Errata Sheet for Stratix V Devices

ES-01034-1.9 Errata Sheet

This errata sheet provides information about known device issues affecting Stratix® V production devices.

Production Device Issues for Stratix V Devices

Table 1 lists the issues and the affected Stratix V production devices.

Table 1. Stratix V Production Device Issues (Part 1 of 2)

Issue	Affected Devices	Planned Fix
"JTAG Programming of 28-nm Devices"	All Stratix V production devices	None
"PCIe Gen2 Link Training Error When Using Hard Reset Controller"	All Stratix V production devices	Software will default to Soft Reset Controller in Quartus II version 13.1.
"LVDS Soft-CDR and DPA Modes"	All Stratix V GX/GS/GT production devices	None
"Receiver Detect Issue in the PCIe Hard IP"	5SGXA7, 5SGXA5, 5SGXA4, 5SGXA3, 5SGSD5, 5SGSD4, 5SGSD3, 5SGTC7, 5SGTC5	5SGXB5, 5SGXB6, 5SGSD6, 5SGSD8, 5SGXA9, 5SGXAB, 5SGXB9, 5SGXBB, 5SEE9, 5SEEB
"Partial Reconfiguration (PR) with Compression Not Supported in Configuration via Procotol (CvP) when Encryption Disabled"	All Stratix V production devices	None
"False Configuration Failure in Active Serial Multi-Device Configuration x1 Mode"	All Stratix V production devices	None
"CMU PLL Range"	All Stratix V GX and GS production devices	None
"Production Device Supply Voltage Requirements"	All Stratix V GX and GS production devices	None
"ATX PLL Range"	All Stratix V GX/GS/GT production devices	For faster operation, contact mySupport.
"Unused or Idle Clock Performance Degradation"	All Stratix V GX/GS/GT production devices	None
"RREF Calibration Resistor Value Changed from 2kΩ to 1.8kΩ"	All Stratix V GX/GS/GT production devices	None

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Table 1. Stratix V Production Device Issues (Part 2 of 2)

Issue	Affected Devices	Planned Fix
"M20K Initialization in Partial Reconfiguration"	5SGXA7, 5SGXA5, 5SGXA4, 5SGXA3, 5SGSD5, 5SGSD4, 5SGSD3, 5SGTC7, 5SGTC5	5SGXB5, 5SGXB6, 5SGSD6, 5SGSD8, 5SGXA9, 5SGXAB, 5SGXB9, 5SGXBB, 5SEE9, 5SEEB
"PCIe Configure Write Operation with Configure Retry Status (CRS) in CvP Mode"	All Stratix V GX/GS/GT production devices	None

JTAG Programming of 28-nm Devices

JTAG configuration of 28-nm devices does not operate correctly when you initiate a `PAUSE_DR` instruction during configuration. In this scenario, JTAG configuration fails when pausing configuration in the middle of the bit stream by entering into the PAUSE-DR state and continuing to clock the TCK input. The failure is indicated by `CONF_DONE` staying low after all of the data has been clocked into the FPGA while `nSTATUS` remains high.

The PAUSE-DR feature works correctly with normal IEEE 1149.1 JTAG test operations.

Workaround

If you require pausing in the middle of the bit stream during JTAG configuration, halt the TCK and do not enter the PAUSE-DR state. Restart the TCK when you resume the configuration.

PCIe Gen2 Link Training Error When Using Hard Reset Controller

An intermittent PCIe Gen2 Hard IP link-up issue may occur in Quartus II version 13.0SP1 and earlier.

When using the hard reset controller in a Gen2 native configuration, the Stratix V Hard IP for PCI Express MegaCore function may incorrectly transmit at 5 Gbps instead of the 2.5 Gbps data rate during link training.

Workaround

For Gen2 configurations that do not use Configuration via Protocol (CvP), follow the instructions in the Knowledge Base Solution for a workaround. For CvP Gen2 configurations, contact mySupport.

LVDS Soft-CDR and DPA Modes

LVDS receivers in Soft-CDR or DPA mode operating between 650 Mbps to 1.25 Gbps include usage restrictions.

For additional information, contact mySupport.

Receiver Detect Issue in the PCIe Hard IP

The Link Training and Status State Machine (LTSSM) in the PCIe Hard IP may become stuck in the Detect.Active state after sending the `TXDetectRX` pulse. This issue may impact your system only if one of the following PCIe Gen1/Gen2 modes is used:

- Autonomous Hard IP
- Configuration via Protocol using PCIe (CvP) **Init mode** only

The CvP update mode is not affected. Other PCIe modes are not impacted by this issue. Contact mySupport if you are using an affected device.

Partial Reconfiguration (PR) with Compression Not Supported in Configuration via Procotol (CvP) when Encryption Disabled

Table 2 shows the PR support with CvP in different combinations of compression and encryption features.

Table 2. Partial Reconfiguration Support

Compression with PR	Encryption with PR	CvP mode	Supported
OFF	OFF	ON	YES
OFF	ON	ON	YES
ON	OFF	ON	NO
ON	ON	ON	NO

There is no restriction when CvP is **Disabled**. For additional inquiries, contact mySupport.

False Configuration Failure in Active Serial Multi-Device Configuration x1 Mode

In Active Serial (AS) multi-device configuration x1 mode, you may experience a false configuration error. The failure is indicated by CONF_DONE going high followed by nSTATUS going low and reconfiguration is initiated repeatedly.

Workaround

To overcome this issue, perform both of the following:

1. Disable the CONF_DONE error checking in AS multi-device configuration mode:
   a. If you are using Quartus® II version 12.0 or older, check the "Disable AS mode CONF_DONE error check" option. This option can be found in the "Advanced" button under the Convert Programming File window.
   b. If you are using Quartus II version 12.0 SP1 or later, the error checking is disabled automatically for AS multi-device configuration POF file generation.

2. Enable the INIT_DONE pin option:
   a. To ensure successful configuration, Altera recommends you enable the INIT_DONE optional pin for devices in the configuration chain. On the board, do not tie INIT_DONE pins together between master and slave devices. Monitor the INIT_DONE status for each device to ensure successful transition into user-mode.

☞ Other configuration modes (JTAG, Fast Passive Parallel (FPP), Passive Serial (PS) single and multi device configuration, and AS single device configuration) are not affected.

CMU PLL Range

The CMU PLL operating range for a -1 transceiver speed grade has changed and is specified in the *Stratix V Device Datasheet*.

Production Device Supply Voltage Requirements

C2 and I2 Speed Grade Core Voltage (VCC) Change

The VCC supply voltage for the C2 and I2 speed grades has changed from 0.85 V to 0.9 V. The voltage change is reflected in the Quartus II version 12.0 software, and the *Stratix V Device Datasheet*. The change applies to VCC, VCCHIP and VCCHSSI, which all must be tied to the same regulator when used.

Transceiver Voltage Changes

The *Stratix V Device Handbook* and *Stratix V Devices Family Pin Connection Guidelines* have been updated to reflect the transceiver voltage changes for VCCR_GXB and VCCT_GXB.

Partial Reconfiguration (PR) Power Supply Requirement

Applications using the PR feature must set the device VCC core voltage supply to 0.9 V. Table 3 summarizes the ordering code and VCC core voltage supply requirements when using PR.

Table 3. Ordering Code and VCC Core Voltage Supply Requirements for PR Applications

Core Speed Grade	For PR Applications, Use Core Speed Grade and VCC Core Voltage Supply
C1	PR is not supported
C2	C2L @ 0.9 V
C2L	C2L @ 0.9 V
C3	C3 @ 0.9 V
C4	C4 @ 0.9 V
I2	Contact mySupport for further assistance
I2L	Contact mySupport for further assistance
I3	I3 @ 0.9 V

Table 3. Ordering Code and VCC Core Voltage Supply Requirements for PR Applications

Core Speed Grade	For PR Applications, Use Core Speed Grade and VCC Core Voltage Supply
I3L	I3L @ 0.9 V
I4	I4 @ 0.9 V

ATX PLL Range

The ATX PLL range is limited for Stratix V production devices. Table 4 through Table 8 list the specifications for these devices.

You must ensure that the correct ATX PLL location is assigned, based on the data rate desired and the specifications listed in Table 4 through Table 8.

Table 4. Specifications for Stratix V GX/GS -1 Transceiver PMA Speed Grade

Range	Dividers *(1)*	Top ATX PLL in Transceiver Bank		Bottom ATX PLL *(2)* in Transceiver Bank		Units
		Min Data Rate	Max Data Rate	Min Data Rate	Max Data Rate	
Native	L = 2	8,000	14,100	8,000	13,200	Mbps
/2	L = 4	4,000	7,050	4,000	6,600	Mbps
/4	L = 8	2,000	3,525	2,000	3,300	Mbps
/8	L = 8, Local/Central Clock Divider = 2	1,000	1,762.5	1,000	1,650	Mbps

Note to Table 4:

(1) "L" is the post VCO Divider within the ATX PLL. The Local/Central Clock Divider is located within the channel.

(2) For faster operation, contact mySupport.

To determine the output frequency of the ATX PLL, divide the data rate by 2. For example, an ATX PLL used for a 12.5 Gbps link will have an output frequency of 6.25 GHz. If local clock dividers are used, then the divide factor must be taken into account. For example, an ATX PLL used for 3.125 and 6.25 Gbps data rate links within the same bank would use a common frequency of 3.125 GHz. That clock would directly feed the 6.25 Gbps links as well as feeding a local data divider set to 2 to generate 1.5625 GHz for the 3.125 Gbps link.

Table 5. Specifications for Stratix V GX/GS -2 Transceiver PMA Speed Grade (Part 1 of 2)

Range	Dividers *(1)*	Top ATX PLL in Transceiver Bank		Bottom ATX PLL in Transceiver Bank		Units
		Min Data Rate	Max Data Rate	Min Data Rate	Max Data Rate	
Native	L = 2	8,000	12,500	8,000	12,500	Mbps
/2	L = 4	4,000	6,600	4,000	6,600	Mbps
/4	L = 8	2,000	3,300	2,000	3,300	Mbps

Table 5. Specifications for Stratix V GX/GS -2 Transceiver PMA Speed Grade (Part 2 of 2)

Range	Dividers *(1)*	Top ATX PLL in Transceiver Bank		Bottom ATX PLL in Transceiver Bank		Units
		Min Data Rate	Max Data Rate	Min Data Rate	Max Data Rate	
/8	L = 8, Local/Central Clock Divider = 2	1,000	1,650	1,000	1,650	Mbps

Note to Table 5:

(1) "L" is the post VCO Divider within the ATX PLL. The Local/Central Clock Divider is located within the channel.

Table 6. Specifications for Stratix V GX/GS -3 Transceiver PMA Speed Grade

Range	Dividers *(1)*	Top ATX PLL in Transceiver Bank		Bottom ATX PLL in Transceiver Bank		Units
		Min Data Rate	Max Data Rate	Min Data Rate	Max Data Rate	
Native	L = 2	8,000	10312.5	8,000	10312.5	Mbps
/2	L = 4	4,000	6,600	4,000	5,500	Mbps
/4	L = 8	2,000	3,300	2,000	2,750	Mbps
/8	L = 8, Local/Central Clock Divider = 2	1,000	1,650	1,000	1,375	Mbps

Note to Table 6:

(1) "L" is the post VCO Divider within the ATX PLL. The Local/Central Clock Divider is located within the channel.

Table 7. Specifications for Stratix V GT -2 Transceiver PMA Speed Grade for GX Channels

Range	Dividers *(1)*	Top ATX PLL in Transceiver Bank		Bottom ATX PLL Left Side in Transceiver Bank *(2)*		Bottom ATX PLL Right Side in Transceiver Bank *(2)*		Units
		Min Data Rate	Max Data Rate	Min Data Rate	Max Data Rate	Min Data Rate	Max Data Rate	
Native	L = 2	8,000	12,500	8,000	12,500	8,000	12,500	Mbps
/2	L = 4	4,000	6,600	4,000	6,600	4,000	7,050	Mbps
/4	L = 8	2,000	3,300	2,000	3,300	2,000	3,525	Mbps
/8	L = 8, Local/Central Clock Divider = 2	1,000	1,650	1,000	1,650	1,000	1,762.5	Mbps

Note to Table 7:

(1) "L" is the post VCO Divider within the ATX PLL. The Local/Central Clock Divider is located within the channel.

(2) Refer to Figure 1 for the Left side and Right side positions.

Table 8. Specifications for Stratix V GT -3 Transceiver PMA Speed Grade for GX Channels

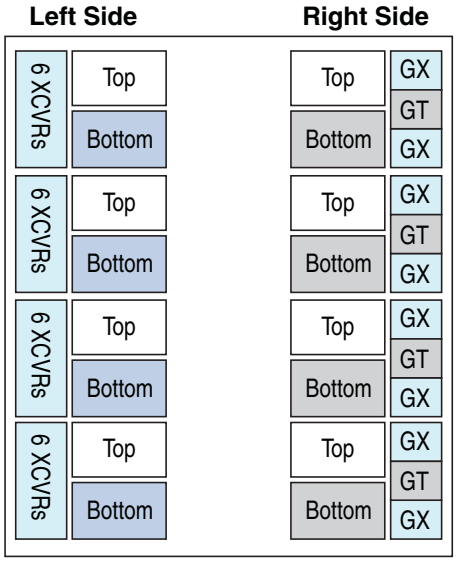
Range	Dividers *(1)*	Top ATX PLL in Transceiver Bank		Bottom ATX PLL Left Side in Transceiver Bank *(2)*		Bottom ATX PLL Right Side in Transceiver Bank *(2)*		Units
		Min Data Rate	Max Data Rate	Min Data Rate	Max Data Rate	Min Data Rate	Max Data Rate	
Native	L = 2	8,000	12,500	8,000	12,500	8,000	12,500	Mbps
/2	L = 4	4,000	6,600	4,000	6,600	4,000	6,600	Mbps
/4	L = 8	2,000	3,300	2,000	3,300	2,000	3,300	Mbps
/8	L = 8, Local/Central Clock Divider = 2	1,000	1,650	1,000	1,650	1,000	1,650	Mbps

Note to Table 8:

(1) "L" is the post VCO Divider within the ATX PLL. The Local/Central Clock Divider is located within the channel.

(2) Refer to Figure 1 for the Left side and Right side positions.

Figure 1. ATX PLL Left and Right Sides



Unused or Idle Clock Performance Degradation

Unused or idle clock dividers of the transceiver can degrade if the devices are powered up to normal operating conditions. This can result in a clock performance degradation of 10% over a period of 5 years. This issue affects designs that will enable unused clock dividers through a new configuration file at a later date. Active clock dividers are not impacted. Non-transceiver circuits are not impacted by this performance degradation.

Guidelines for Eliminating Performance Degradation

1. For unused channels, apply one of the following:
   a. Recompile with Quartus II software, version 12.1 or later to power down the unused clock dividers. This guideline applies to GX channels.
   b. For GX channels designed with Quartus II versions before 12.1, and for GT channels designed with any version of the Quartus II software, instantiate currently unused transceiver channels that may be enabled with a future programming file. This will create activity on currently unused channels. This guideline applies to both GX and GT channels.
2. For used (configured) channels, apply the following:

   For any version of the Quartus II software, do not assert the PLL and analog reset signals indefinitely. This guideline applies to both GX and GT channels.

RREF Calibration Resistor Value Changed from 2kΩ to 1.8kΩ

The R_{REF} calibration resistor value specification has changed from 2kΩ to 1.8kΩ with a maximum tolerance of +/– 1%.

M20K Initialization in Partial Reconfiguration

M20Ks cannot be configured as ROMs or initialized RAMs using partial reconfiguration (PR). Use MLABs as a workaround.

PCIe Configure Write Operation with Configure Retry Status (CRS) in CvP Mode

After a reset (fundamental or FLR), the core will respond to Configuration (CFG) requests with a CRS until the soft logic is ready for normal operation. In the case of Configuration Writes (CFGWR), the core will respond with a CRS, but it will still execute the register write. Therefore, after a reset, Configuration Reads (CFGRD) must be issued until a non-CRS response is received from the PCIe core before issuing any CFGWR. This issue only affects CvP mode.

Document Revision History

Table 9 lists the revision history for this errata sheet.

Table 9. Document Revision History

Date	Version	Changes
March 2018	1.9	■ Added the "Partial Reconfiguration (PR) Power Supply Requirement" section.
January 2017	1.8	■ Changed the support value when compression with PR, Encryption with PR, and CvP mode are all ON in the "Partial Reconfiguration Support" table.
September 2015	1.7	■ Added the "JTAG Programming of 28-nm Devices" section. ■ Updated the maximum data rate in the "Specifications for Stratix V GX/GS -3 Transceiver PMA Speed Grade" table.
September 2013	1.6	■ Added the "PCIe Gen2 Link Training Error When Using Hard Reset Controller" section. ■ Updated the "C2 and I2 Speed Grade Core Voltage (VCC) Change"section. Renamed "-2 Speed Grade" to "C2 and I2 Speed Grade." ■ Updated the "ATX PLL Range"section.
July 2013	1.5	■ Added the "LVDS Soft-CDR and DPA Modes" section. ■ Added the "Receiver Detect Issue in the PCIe Hard IP"section. ■ Added the "Partial Reconfiguration (PR) with Compression Not Supported in Configuration via Procotol (CvP) when Encryption Disabled" section. ■ Updated the "CMU PLL Range"section. ■ Updated the "Production Device Supply Voltage Requirements" section. ■ Added the "Partial Reconfiguration (PR) Power Supply Requirement" section. ■ Updated the "Unused or Idle Clock Performance Degradation" section. ■ Updated the "PCIe Configure Write Operation with Configure Retry Status (CRS) in CvP Mode" section.
September 2012	1.4	Added Note 2 to Table 8 to close FB #53141.
July 2012	1.3	■ Added the "False Configuration Failure in Active Serial Multi-Device Configuration x1 Mode" section. ■ Updated Table 1 and Table 8. ■ Added Table 6 and Table 7. ■ Added Figure 1.
June 2012	1.2	■ Added the "False Configuration Failure in Active Serial Multi-Device Configuration x1 Mode" section. ■ Updated the "CMU PLL Range" section. ■ Updated the "Production Device Supply Voltage Requirements" section. ■ Updated the "Transceiver Voltage Changes" section. ■ Updated the "ATX PLL Range" section. ■ Removed CMU PLL at Channel 01 Driving Channel 0 in Non-Bonded Mode section.
May 2012	1.1	■ Added the "CMU PLL Range" section. ■ Updated the "ATX PLL Range" section. ■ Updated the "Transceiver Voltage Changes" section. ■ Added the "RREF Calibration Resistor Value Changed from 2k W to 1.8k W" section.
March 2012	1.0	Initial release.