# Link Replicator for Fibre Channel, Gigabit Ethernet, and HDTV Data Rates

**Check for Samples: SN65LVCP15**

## FEATURES

- **Replicates Serial Links Such as Fibre Channel, Gigabit Ethernet, and HDTV Links**
- **T11 Fibre Channel Compliant at 1.0634 Gb/s**
- **IEEE802.3-2005 Gigabit Ethernet Compliant at 1.25 Gb/s (1000Base-X)**
- **Support for SMPTE-292M Data Rate at 1.485 Gb/s**
- **Compatible With VSC7132-01**
- **No External Components Required**

- **0.455 W Maximum Power Dissipation**
- **3.3 V Power Supply**
- **28-Pin, 4,4 mm × 9,7 mm TSSOP Package**
- **Footprint Compatible with VSC7132**

## APPLICATIONS

- **Test Equipment**
- **Gigabit Ethernet and Fibre Channel Switches/Repeaters**

## DESCRIPTION

The SN65LVCP15 is a high performance serial link mux for use in Fibre Channel (1.0625 Gb/s), Gigabit Ethernet (1.25 Gb/s), and other high speed interface applications. A common application involves a serializer/deserializer (SerDes), such as the TLK2201B, which would normally be connected to the IN± and OUT± ports in order to provide duplicate set of links on the IN0/OUT0 and IN1/OUT1 ports. This type of application is often used to implement high speed test ports that can be monitored without affecting the serial data stream of the application. A popular application is in Line Cards, that use serial links from a SerDes like TLK2201B (SLLS585), where the SN65LVCP15 provides redundant, hot-swappable links to redundant Switch Fabric Cards.

During normal operation, IN is sent to both OUT0 and OUT1 whose buffers are enabled when OE0 and OE1 are HIGH. OUT0 can select between IN and IN1. OUT1 can select between IN and IN0. OUT can select between IN0 and IN1.

In Link Replicator applications, such as the Line Card to Switch Card links, IN is transmitted to both OUT0 and OUT1 which either IN0 or IN1 is selected at OUT. In host Adapter applications, IN goes to OUT0 (an internal connector) which returns data and IN0. IN0 is looped to OUT1 (an external connector) which returns data on IN1 and then back to the SerDes on OUT.

⚠️ These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ORDERING INFORMATION

| ORDERABLE PART NUMBER | DESCRIPTION |
|---|---|
| SN65LVCP15PW[1] | 28-Pin TSSOP, 4,4 mm x 9,7 mm Body |

(1)  For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS[1]

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{DD}$ | Power supply voltage, TTL | 0.5 to 4.0 | V |
| $V_{IN(P)}$ | DC input voltage, PECL | −0.5 to $V_{DD}$ +0.5 | V |
| $V_{IN(T)}$ | DC input voltage, TTL | −0.5 to +5.5 | V |
| $V_{IN(TTL)}$ | DC voltage applied to outputs for high output state | −0.5 to $V_{DD}$ +0.5 | V |
| ESD | Electrostatic discharge voltage (human body model) | 2 | kV |
| $T_{JA}$ | Junction to Ambient Thermal Resistance (Assumes High K Board) | 61.7 | °C/W |

(1)  Stresses listed under absolute maximum ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to theses values for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Power supply voltage | 3.14 | 3.47 | V |
| | Operating temperature range | −40 | 85 | °C |

## AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

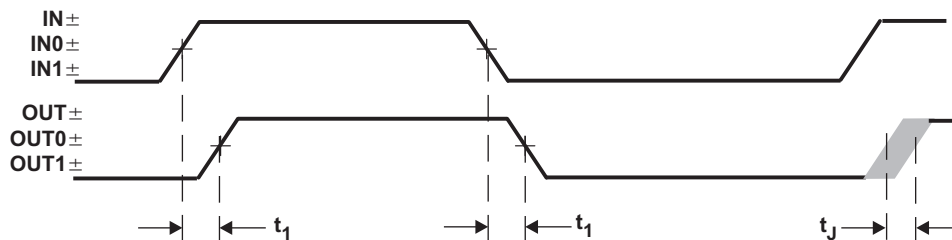| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| f | Operating frequency range | | 1 | | 1.5 | Gb/s |
| $t_1$ | Flow-through propagation delay | Delay from any input to any output | | | 1 | ns |
| $t_r$, $t_f$ | Serial data rise and fall time | 20% to 80% | | | 300 | ps |
| $t_{DJ}$ | Deterministic jitter added to serial input | 1 Gb/s to 1.25 Gb/s. Measured on K28.5+, K28.5− pattern | | | 35 | ps pp |
| | | 1.25 Gb/s to 1.5 Gb/s. Measured on K28.5+, K28.5− pattern | | | 45 | |



**Figure 1.  Timing Waveforms**

## DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH(TTL)}$ | Input HIGH voltage | | 2 | | 5.5 | V |
| $V_{IL(TTL)}$ | Input LOWS voltage | | 0 | | 0.8 | V |
| $I_{IH(TTL)}$ | Input HIGH current | $V_{IN}$ = 2.4 V | -100 | | 100 | µA |
| $I_{IL(TTL)}$ | Input HIGH current | $V_{IN}$ = 0.5 V | −100 | | 100 | µA |
| $V_{DD}$ | Supply voltage | $V_{DD}$ = 3.30 V ±5% | 3.14 | | 3.47 | V |
| $I_{DD}$ | Supply current | Outputs open, $V_{DD}$ = $V_{DD}$ max | | | 131 | mA |
| $P_D$ | Power dissipation | Outputs open, $V_{DD}$ = $V_{DD}$ max | | | 455 | mW |
| $\Delta V_{IN}$ | Receiver differential peak-to-peak input sensitivity (IN, IN0, IN1) | AC coupled, Internally biased at $V_{DD}$/2 | 300 | | 2600 | $mV_{PP}$ |
| $\Delta V_{OUT50}$ | Output differential peak-to-peak voltage swing (OUT, OUT0, OUT1) | 50 Ω to $V_{DD}$ − 2 V | 1000 | | 2200 | $mV_{PP}$ |
| $\Delta V_{OUT75}$ | | 75 Ω to $V_{DD}$ − 2 V | 1200 | | 2200 | $mV_{PP}$ |

## APPLICATION EXAMPLE

Signal Re-Driver Example
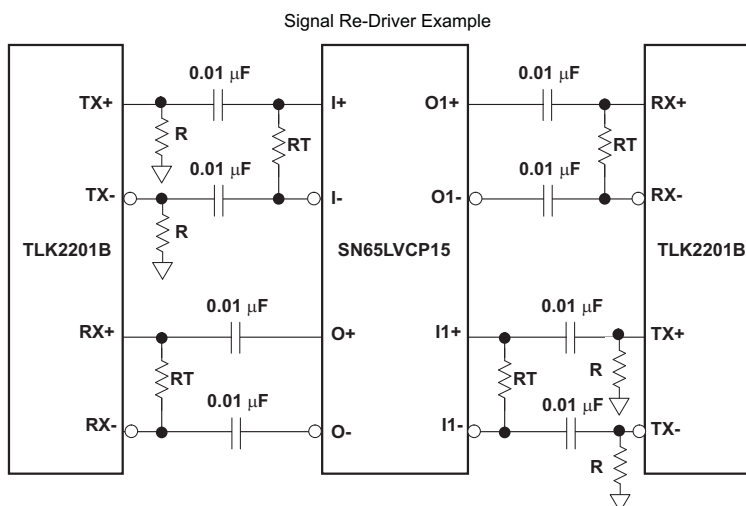


R is 150 Ω for both 100 Ω differential or 150 Ω differential traces.

RT matches the differential impedance of the link.

For optimal signal integrity performance, A/C coupling is recommended.

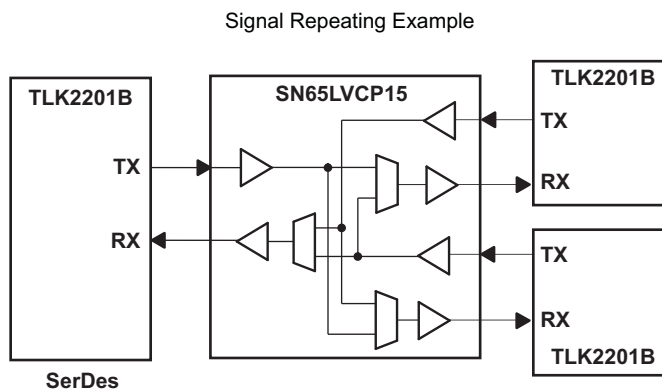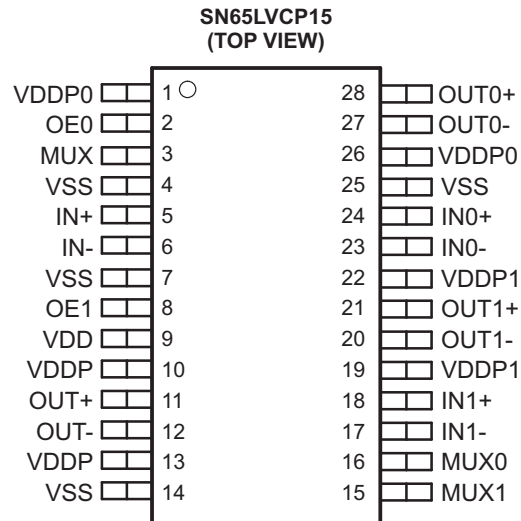**Figure 2.  TLK2201B and SN65LVCP15 Interconnect**

Signal Repeating Example



**Figure 3.**

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Product Folder Links: *SN65LVCP15*

## PACKAGE INFORMATION – PIN DIAGRAM

**SN65LVCP15**
**(TOP VIEW)**

| | | | | |
|---|---|---|---|---|
| VDDP0 | 1 | | 28 | OUT0+ |
| OE0 | 2 | | 27 | OUT0- |
| MUX | 3 | | 26 | VDDP0 |
| VSS | 4 | | 25 | VSS |
| IN+ | 5 | | 24 | IN0+ |
| IN- | 6 | | 23 | IN0- |
| VSS | 7 | | 22 | VDDP1 |
| OE1 | 8 | | 21 | OUT1+ |
| VDD | 9 | | 20 | OUT1- |
| VDDP | 10 | | 19 | VDDP1 |
| OUT+ | 11 | | 18 | IN1+ |
| OUT- | 12 | | 17 | IN1- |
| VDDP | 13 | | 16 | MUX0 |
| VSS | 14 | | 15 | MUX1 |

### PIN FUNCTIONS

| PIN NO. | NAME | TYPE | LEVEL | DESCRIPTION |
|---|---|---|---|---|
| 5, 6<br>24, 23<br>18, 17 | IN+, IN–<br>IN0+, IN0–<br>IN1+, IN1– | I | PECL | Differential (biased to $V_{DD}/2$) High-speed serial inputs |
| 11, 12<br>28, 27<br>21, 20 | OUT+, OUT–<br>OUT0+, OUT0–<br>OUT1+, OUT1– | O | PECL | Differential high-speed serial outputs |
| 2<br>8 | OE0<br>OE1 | I | TTL | OE0/OE1 enables OUT0/OUT1 when HIGH. When LOW, OUTx is powered down and both OUTx+ and OUTx– float HIGH. |
| 3 | MUX | I | TTL | Determines source of OUT. Selects either IN0 (LOW) or IN1 (HIGH). |
| 15 | MUX1 | I | TTL | Determines source of OUT1. Selects either IN (HIGH) or IN0 (LOW). |
| 16 | MUX0 | I | TTL | Determines source of OUT0. Selects either IN (LOW) or IN1 (HIGH). |
| 9 | VDD | Pwr | | 3.3 V power supply for digital logic |
| 10, 13<br>1, 26<br>19, 22 | VDDP<br>VDDP0<br>VDDP1 | Pwr | | High-speed output power supply: 3.3 V supply for PECL drivers. VDDP0 is for OUT0, VDDP is for OUT, and VDDP1 is for OUT1. |
| 4, 7<br>14, 25 | VSS | Pwr | | Ground |

## MOISTURE SENSITIVITY LEVEL

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standards.

## REVISION HISTORY

| **Changes from Original (October 2008) to Revision A** | **Page** |
|---|---|

- Deleted $I_O$ - DC output HIGH current, PECL from the ABSOLUTE MAXIMUM RATINGS table ......................................... 2

| **Changes from Revision A (November 2008) to Revision B** | **Page** |
|---|---|

- Changed Case operating temperature To: Operating temperature range and the range From: 0 to 85°C To: –40 to 85°C ...................................................................................................................................................................... 2

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVCP15PW | ACTIVE | TSSOP | PW | 28 | 50 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCP15 | Samples |
| SN65LVCP15PWR | ACTIVE | TSSOP | PW | 28 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LVCP15 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



Reel Diameter

Reel Width (W1)

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVCP15PWR | TSSOP | PW | 28 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------|--------------|-----------------|------|-----|-------------|-----------|-------------|
| SN65LVCP15PWR | TSSOP | PW | 28 | 2000 | 853.0 | 449.0 | 35.0 |

## TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|--------|--------------|--------------|------|-----|--------|--------|--------|--------|
| SN65LVCP15PW | PW | TSSOP | 28 | 50 | 530 | 10.2 | 3600 | 3.5 |

PW (R−PDSO−G28)                    PLASTIC SMALL OUTLINE



0,65

0,30
0,19

⊕ 0,10 Ⓜ

28                               15

D  4,50
   4,30      6,60
             6,20

1                                14

9,80
9,60

C

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,10

4040064-7/G  02/11

NOTES:   A.  All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.  This drawing is subject to change without notice.
         C.  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
             not exceed 0,15 each side.
         D.  Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.  Falls within JEDEC MO−153

PW (R−PDSO−G28)                                    PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

26x0,65

28x0,25                    1,55

5,60

5,60

26x0,65

Example
Non Soldermask Defined Pad

0,3

Example
Solder Mask Opening
(See Note E)

1,6

Pad Geometry

0,07 All Around

4211284−6/G   08/15

NOTES:   A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Publication IPC−7351 is recommended for alternate design.
         D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
         E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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