TS5A3159-Q1 1-Ω SPDT Analog Switch

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Specified Break-Before-Make Switching
- Low ON-State Resistance (1 Ω)
- Control Inputs are 5-V Tolerant
- Low Charge Injection
- Excellent ON-Resistance Matching
- Low Total Harmonic Distortion
- 1.65-V to 5.5-V Single-Supply Operation

2 Applications

- Automotive Infotainment and Cluster
- Body Electronics and Lighting

3 Description

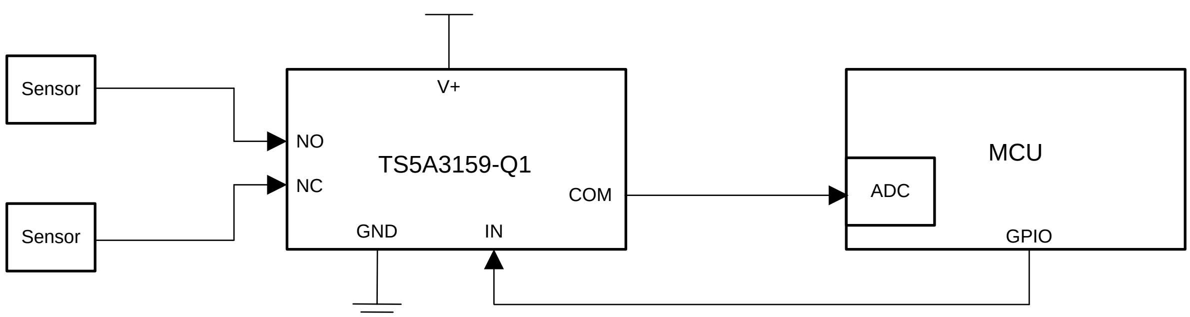
The TS5A3159-Q1 is a single-pole double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance and an excellent ON-resistance, matching with the break-before-make feature to prevent signal distortion during the transferring of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A3159-Q1	SOT-23 (6)	2.90 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Selector Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (October 2015) to Revision C	Page
• Changed I/O for V_+ from I to —	4
• Added V_{NC} to Analog voltage, Analog port diode current, and ON−state switch current	4
• Added Junction temperature, T_J to *Absolute Maximum Ratings*	4
• Changed MIN value for V+ from 1.8 to 1.65 and MAX value from 5 to 5.5	5
• Changed MAX value for IN from 5 to 5.5	5
• Changed MAX value for NO, NC, COM from 5 to V+	5
• Added V_{IL} MAX value 0.6 and deleted TYP value 0.6	7
• Added *Receiving Notification of Documentation Updates* section	20

Changes from Revision A (December 2012) to Revision B	Page
• Added ESD Ratings table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	4

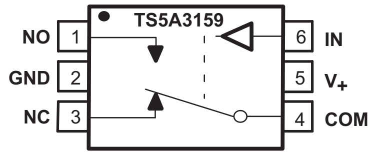
Changes from Original (November, 2012) to Revision A	Page
• Device going from Preview to Production	1
• Changed r_{on} max values from 1.1 to 1.3	5
• Changed $I_{NC(OFF)}$, $I_{NO(OFF)}$ min and max values for 25°C from –2 and 2 to –6 and 6, respectively. Changed min and max values for Full from –20 and 20 to –150 and 150, respectively	5
• Changed $I_{NC(ON)}$, $I_{NO(ON)}$ min and max values for 25°C from –4 and 4 to –6 and 6, respectively. Changed min and max values for Full from –40 and 40 to –150 and 150, respectively	5
• Changed $I_{COM(ON)}$ min and max values for 25°C from –4 and 4 to –8 and 8, respectively. Changed min and max values for Full from –40 and 40 to –150 and 150, respectively.	5
• Inserted 25°C above Full in T_A column and inserted 0.5 µA max value for I_+	6

Copyright © 2012–2016, Texas Instruments Incorporated

Copyright © 2012–2016, Texas Instruments Incorporated

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	NO	I/O	Normally-open terminal
2	GND	—	Digital ground
3	NC	I/O	Normally-closed terminal
4	COM	I/O	Common terminal
5	V_+	—	Power supply
6	IN	I	Digital control pin to connect COM terminal to NO or NC terminals

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_+	Supply voltage (2)		–0.5	6.5	V
V_{NO}, V_{NC}, V_{COM}	Analog voltage (2)(3)(4)		–0.5	V_+ + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NO}, V_{NC}, V_{COM} < 0 or V_{NO}, V_{NC}, V_{COM} > V_+		±50	mA
I_{NO}, I_{NC}, I_{COM}	ON−state switch current	V_{NO}, V_{NC}, V_{COM} = 0 to V_+		±200	mA
	ON−state peak switch current (5)			±400	mA
V_{IN}	Digital input voltage range (2)(3)		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_{IN} < 0		−50	mA
	Continuous current through V_+ or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) Pulse at 1 ms duration < 10% duty cycle.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (NO, NC, IN, and COM)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

Copyright © 2012–2016, Texas Instruments Incorporated

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V+	1.65	5.5	V
IN	0	5.5	V
NO, NC, COM	0	V+	V

6.4 Thermal Information

THERMAL METRIC[1]		TS5A3159-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	192.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	133.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	38.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V and T_A = −40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP[1]	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –30 mA	Switch ON, See Figure 11	25°C	4.5 V		1	1.5	Ω
				Full				1.5	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –30 mA	Switch ON, See Figure 10	25°C	4.5 V		0.75	1.3	Ω
				Full				1.3	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2.5 V, I_{COM} = –30 mA	Switch ON, See Figure 10	25°C	4.5 V		0.1		Ω
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO}$ or $V_{NC} \le V_+$, I_{COM} = –30 mA	Switch ON, See Figure 10	25°C	4.5 V		0.233		Ω
		V_{NO} or V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –30 mA		25°C			0.15		
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 4.5 V, V_{COM} = 0	Switch OFF, See Figure 12	25°C	5.5 V	−6	0.2	6	nA
				Full		−150		150	
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 4.5 V, VCOM = Open	Switch ON, See Figure 13	25°C	5.5 V	−6	2.8	6	nA
				Full		−150		150	
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = 4.5 V or Open, V_{COM} = 4.5 V	Switch ON, See Figure 13	25°C	5.5 V	–8	0.47	8	nA
				Full		−150		150	
DIGITAL INPUTS (IN)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		Full	5.5 V	−1		1	μA

(1) T_A = 25°C

Copyright © 2012–2016, Texas Instruments Incorporated

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V and T_A = −40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
DYNAMIC									
t_{ON}	Turn-on time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	4.5 V to 5.5 V		20	35	ns
				Full				40	
t_{OFF}	Turn-off time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	4.5 V to 5.5 V		15	20	ns
				Full				35	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+ / 2, R_L = 50 Ω,	C_L = 35 pF, See Figure 16	25°C	4.5 V to 5.5 V	1	12	14.5	ns
				Full		1			
Q_C	Charge injection	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 19	25°C	5 V		36		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 13	25°C	5 V		23		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 13	25°C	5 V		84		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 13	25°C	5 V		84		pF
C_{IN}	Digital input capacitance	V_{IN} = V_+ or GND,	See Figure 13	25°C	5 V		2.1		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	5 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 17	25°C	5 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 18	25°C	5 V		–65		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 19	25°C	5 V		0.01%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	5.5 V			0.1	µA
				Full				0.5	

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V and T_A = −40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V+, I_{COM} = –24 mA,	Switch ON, See Figure 10	25°C	3 V		1.35	2.2	Ω
				Full				2.2	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 2 V, I_{COM} = –24 mA,	Switch ON, See Figure 10	25°C	3 V		1.15	1.8	Ω
				Full				1.8	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –24 mA,	Switch ON, See Figure 10	25°C	3 V		0.11		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V+, I_{COM} = –24 mA,	Switch ON, See Figure 10	25°C	3 V		0.225		Ω
		V_{NO} or V_{NC} = 2 V, 0.8 V, I_{COM} = –24 mA,		25°C			0.25		
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO OFF leakage current	V_{NC} or V_{NO} = 3 V, V_{COM} = 0,	Switch OFF, See Figure 11	25°C	3.6 V		0.2		nA
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO ON leakage current	V_{NC} or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 12	25°C	3.6 V		2.8		nA
$I_{COM(ON)}$	COM ON leakage current	V_{NC} or V_{NO} = 3 V or Open, V_{COM} = 3 V,	Switch ON, See Figure 12	25°C	3.6 V		0.47		nA

(1) T_A = 25°C

Copyright © 2012–2016, Texas Instruments Incorporated

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V and T_A = −40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP[(1)]	MAX	UNIT
DIGITAL INPUTS (IN)									
V_{IH}	Input logic high			Full		2		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		Full	3.6 V	–1		1	µA
DYNAMIC									
t_{ON}	Turn-on time	$V_{COM} = V_+$, R_L = 50 Ω	C_L = 35 pF, See Figure 15	25°C	3 V to 3.6 V		30	40	ns
				Full				55	
t_{OFF}	Turn-off time	$V_{COM} = V_+$, R_L = 50 Ω	C_L = 35 pF, See Figure 15	25°C	3 V to 3.6 V		20	25	ns
				Full				40	
t_{BBM}	Break-before-make time	$V_{NC} = V_{NO} = V_+ / 2$, R_L = 50 Ω	C_L = 35 pF, See Figure 16	25°C	3 V to 3.6 V	1	21	29	ns
				Full		1			
Q_C	Charge injection	C_L = 1 nF, V_{GEN} = 0 V	See Figure 19	25°C	3.3 V		20		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch OFF	See Figure 13	25°C	3.3 V		23		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch ON	See Figure 13	25°C	3.3 V		84		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON	See Figure 13	25°C	3.3 V		84		pF
C_{IN}	Digital input capacitance	V_{IN} = V_+ or GND	See Figure 13	25°C	3.3 V		2.1		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON	See Figure 16	25°C	3.3 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz	Switch OFF, See Figure 17	25°C	3.3 V		–65		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz	Switch ON, See Figure 18	25°C	3.3 V		–65		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF	f = 600 Hz to 20 kHz, See Figure 19	25°C	3.3 V		0.015%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND	Switch ON or OFF	25°C	3.6 V			0.1	µA
				Full				0.5	

6.7 Electrical Characteristics For 2.5-V Supply

V_+ = 2.3 V to 2.7 V and T_A = −40°C to +125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP[(1)]	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –8 mA	Switch ON, See Figure 10	25°C	2.5 V		1.7	2.9	Ω
				Full				2.9	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.8 V, I_{COM} = –8 mA	Switch ON, See Figure 10	25°C	2.5 V		1.45	2.3	Ω
				Full				2.3	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA	Switch ON, See Figure 10	25°C	2.5 V		0.7		Ω
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = –8 mA	Switch ON, See Figure 10	25°C	2.5 V		0.5		Ω
		V_{NO} or V_{NC} = 0.8 V, 1.8 V, I_{COM} = –8 mA		25°C			0.45		
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO Off leakage current	V_{NC} or V_{NO} = 2.3 V, V_{COM} = 0	Switch OFF, See Figure 11	25°C	2.7 V		0.2		nA
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO On leakage current	V_{NC} or V_{NO} = 2.3 V, V_{COM} = Open	Switch ON, See Figure 12	25°C	2.7 V		2.8		nA
$I_{COM(ON)}$	COM On leakage current	V_{NC} or V_{NO} = 2.3 V or Open, V_{COM} = 2.3 V	Switch ON, See Figure 12	25°C	2.7 V		0.47		nA
DIGITAL INPUTS (IN)									
V_{IH}	Input logic high			Full		1.8		5.5	V
V_{IL}	Input logic low			Full		0	0.6		V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		Full	2.7 V	−1		1	μA
DYNAMIC									
t_{ON}	Turn-on time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	2.3 V to 2.7 V		40	55	ns
				Full				70	
t_{OFF}	Turn-off time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	2.3 V to 2.7 V		30	40	ns
				Full				55	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+ / 2, R_L = 50 Ω,	C_L = 35 pF, See Figure 16	25°C	2.3 V to 2.7 V	1	33	39	ns
				Full		1			
Q_C	Charge injection	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 19	25°C	2.5 V		13		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	2.5 V		23		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	2.5 V		84		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	2.5 V		84		pF
C_{IN}	Digital input capacitance	V_{IN} = V_+ or GND,	See Figure 14	25°C	2.5 V		2.1		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	2.5 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 17	25°C	2.5 V		–64		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 18	25°C	2.5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 600 Hz to 20 kHz, See Figure 19	25°C	2.5 V		0.025%		
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	2.7 V			0.1	μA
				Full				0.5	

(1) T_A = 25°C

Copyright © 2012–2016, Texas Instruments Incorporated

6.8 Electrical Characteristics For 1.8-V Supply

V_+ = 1.65 V to 1.95 V and T_A = −40°C to +125°C (unless otherwise noted

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP(1)	MAX	UNIT
ANALOG SWITCH									
V_{COM}, V_{NO}, V_{NC}	Analog signal range					0		V_+	V
r_{peak}	Peak ON-state resistance	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = −2 mA	Switch ON, See Figure 10	25°C	1.8 V		4	5.2	Ω
				Full				5.2	
r_{on}	ON-state resistance	V_{NO} or V_{NC} = 1.5 V, I_{COM} = −2 mA	Switch ON, See Figure 10	25°C	1.8 V		1.7	3.5	Ω
				Full				3.5	
Δr_{on}	ON-state resistance match between channels	V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = −2 mA	Switch ON, See Figure 10	25°C	1.8 V		0.7		Ω
				Full			0.7		
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} or V_{NC} ≤ V_+, I_{COM} = −2 mA	Switch ON, See Figure 11	25°C	1.8 V		1.85		Ω
				Full			1.85		
		V_{NO} or V_{NC} = 0.6 V, 1.5 V, I_{COM} = −2 mA		25°C			0.9		
				Full			0.9		
$I_{NC(OFF)}$, $I_{NO(OFF)}$	NC, NO Off leakage current	V_{NC} or V_{NO} = 1.65 V, V_{COM} = 0	Switch OFF, See Figure 11	25°C	1.95 V		0.2		nA
$I_{NC(ON)}$, $I_{NO(ON)}$	NC, NO On leakage current	V_{NC} or V_{NO} = 1.65 V, V_{COM} = Open	Switch ON, See Figure 12	25°C	1.95 V		2.8		nA
$I_{COM(ON)}$	COM On leakage current	V_{NC} or V_{NO} = 1.65 V or Open, V_{COM} = 1.65 V	Switch ON, See Figure 12	25°C	1.95 V		0.47		nA
DIGITAL INPUTS (IN)									
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_{IN} = 5.5 V or 0		Full	1.95 V	−1		1	µA
DYNAMIC									
t_{ON}	Turn-on time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	1.65 V to 1.95 V		65	70	ns
				Full				95	
t_{OFF}	Turn-off time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	1.65 V to 1.95 V		40	55	ns
				Full				70	
t_{BBM}	Break-before-make time	V_{NC} = V_{NO} = V_+ / 2, R_L = 50 Ω,	C_L = 35 pF, See Figure 15	25°C	1.65 V to 1.95 V	1	60	72	ns
				Full		0.5			
Q_C	Charge injection	C_L = 1 nF, V_{GEN} = 0 V,	See Figure 19	25°C	1.8 V		13		pC
$C_{NC(OFF)}$, $C_{NO(OFF)}$	NC, NO OFF capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch OFF,	See Figure 14	25°C	1.8 V		23		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NC, NO ON capacitance	V_{NC} or V_{NO} = V_+ or GND, Switch ON,	See Figure 14	25°C	1.8 V		84		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See Figure 14	25°C	1.8 V		84		pF
C_{IN}	Digital input capacitance	V_{IN} = V_+ or GND,	See Figure 14	25°C	1.8 V		2.1		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 16	25°C	1.8 V		100		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 17	25°C	1.8 V		–63		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 18	25°C	1.8 V		–63		dB
SUPPLY									
I_+	Positive supply current	V_{IN} = V_+ or GND,	Switch ON or OFF	25°C	1.95 V			0.1	µA
				Full				0.5	

(1) T_A = 25°C

6.9 Typical Characteristics

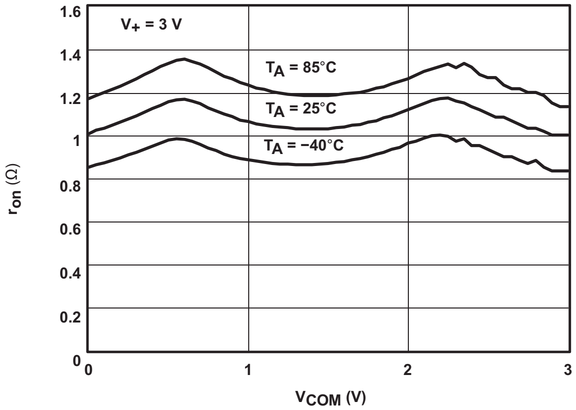


Figure 1. r_{on} vs V_{COM}

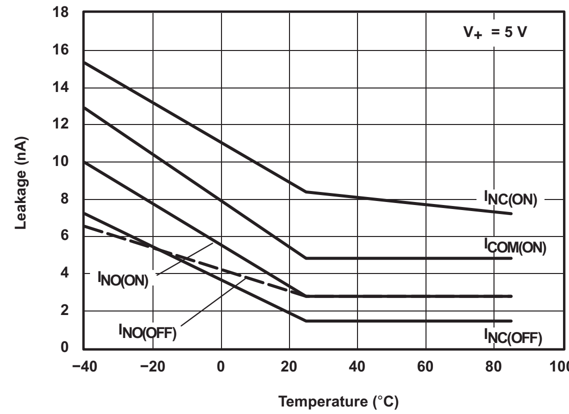


Figure 2. Leakage Current vs Temperature

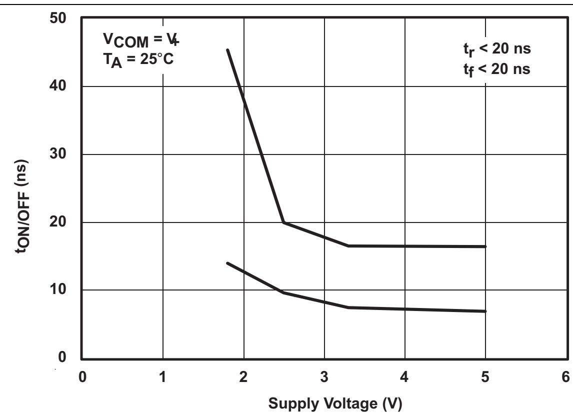


Figure 3. $t_{ON/OFF}$ vs V+

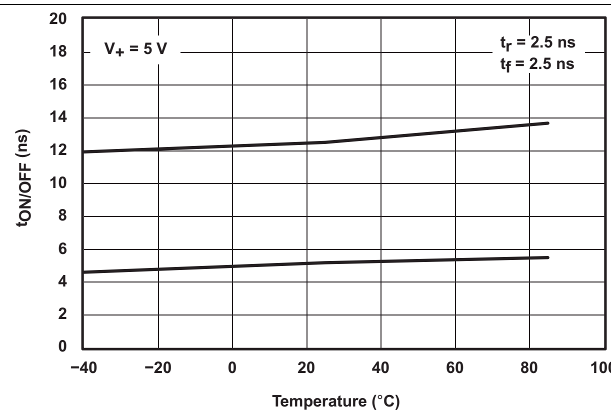


Figure 4. $t_{ON/OFF}$ vs Temperature

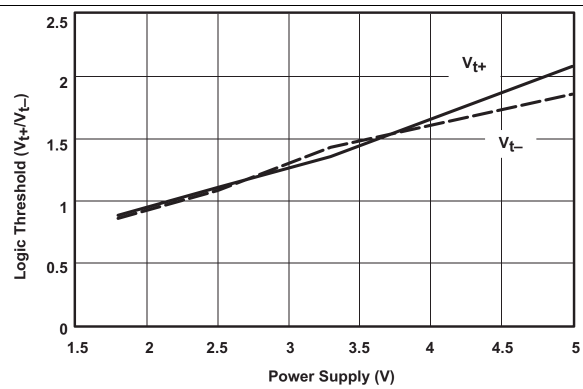


Figure 5. Logic Threshold vs Power Supply

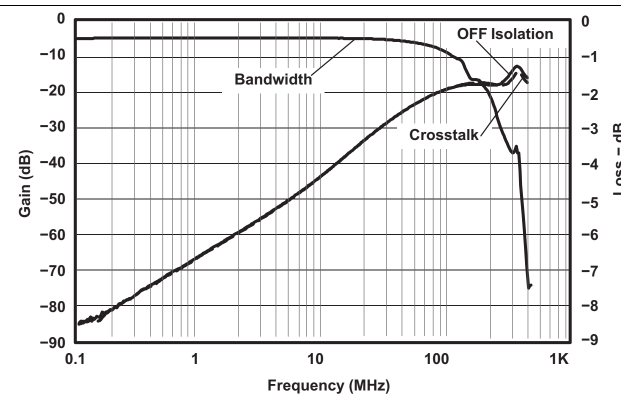


Figure 6. Frequency Response

Copyright © 2012–2016, Texas Instruments Incorporated

Typical Characteristics (continued)

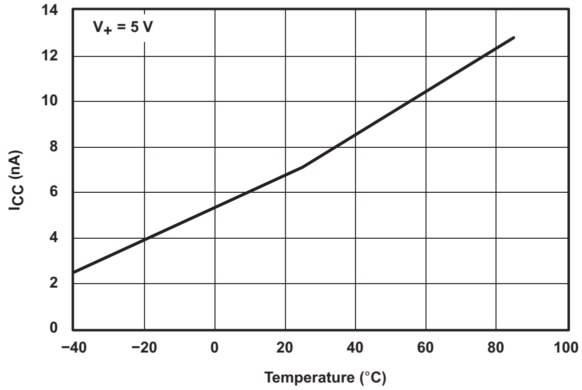


Figure 7. Power-Supply Current vs Temperature

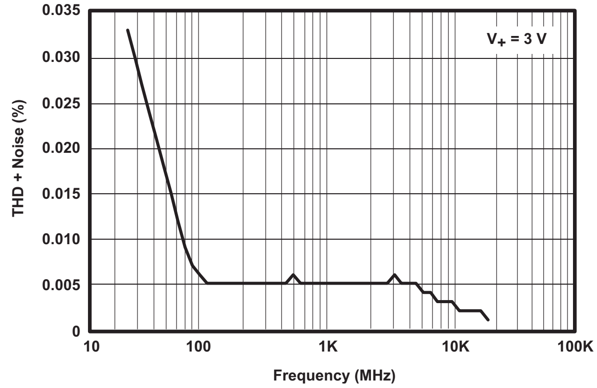


Figure 8. Total Harmonic Distortion (THD) vs Frequency

7 Parameter Measurement Information

Table 1. Parameter Description

SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NC}	Voltage at NC
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NC or COM and NO ports, when the channel is ON
r_{peak}	Peak ON-state resistance over a specified voltage range
Δr_{on}	Difference of r_{on} between channels
ron(flat)	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NC(OFF)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the OFF state under worst-case input and output conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state under worst-case input and output conditions
$I_{NC(ON)}$	Leakage current measured at the NC port, with the corresponding channel (NC to COM) in the ON state and the output (COM) being open
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) being open
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO or COM to NC) in the ON state and the output (NC or NO) being open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Minimum input voltage for logic low for the control input (IN)
V_{IN}	Voltage at IN
I_{IH}, I_{IL}	Leakage current measured at IN
t_{ON}	Turn-on time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal, when the switch is turning ON.
t_{OFF}	Turn-off time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog outputs (COM, NC, or NO) signal, when the switch is turning OFF.
t_{BBM}	Break-before-make time. This parameter is measured under the specified range of conditions and by the propagation delay between the output of two adjacent analog channels (NC and NO), when the control signal changes state.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NC, NO, or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_O$, C_L is the load capacitance, and ΔV_O is the change in analog output voltage.
$C_{NC(OFF)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is OFF
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NC(ON)}$	Capacitance at the NC port when the corresponding channel (NC to COM) is ON
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NC or COM to NO) is ON
C_{IN}	Capacitance of IN
O_{ISO}	OFF isolation of the switch is a measurement OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NC to COM or NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NC to NO or NO to NC). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is −3 dB below the DC gain.
I_+	Static power-supply current with the control (IN) pin at V_+ or GND
ΔI_+	This is the increase in I_+ for each control (IN) input that is at the specified voltage, rather than at V_+ or GND.

Copyright © 2012–2016, Texas Instruments Incorporated

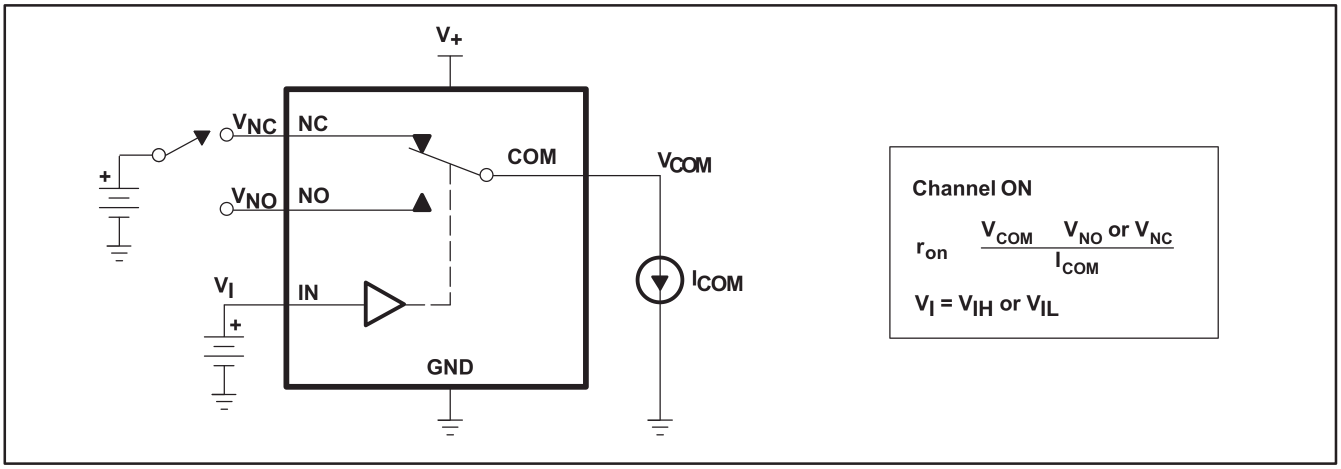


Figure 9. On-State Resistance (r_{on})

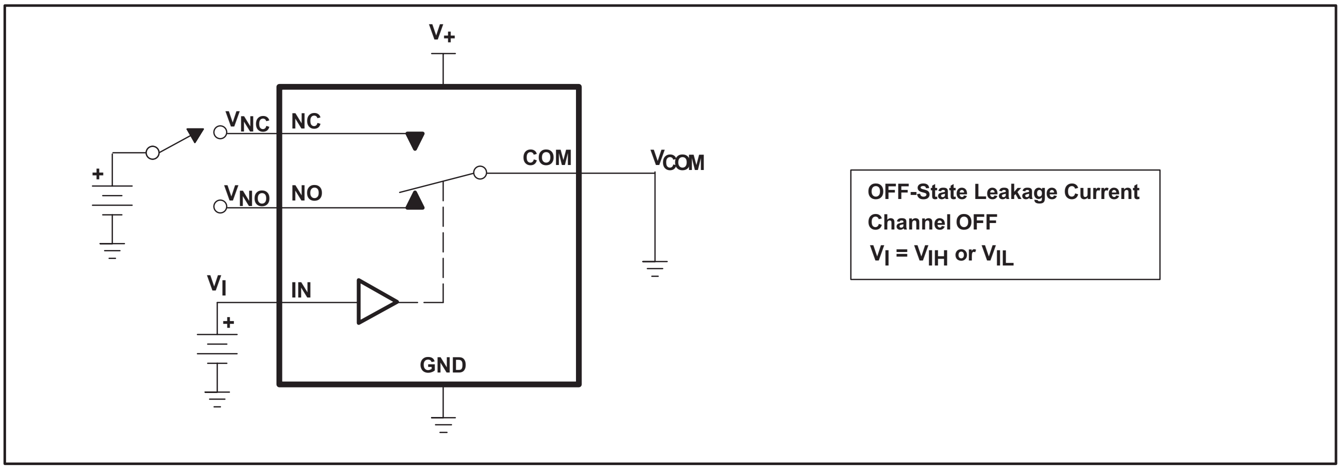


Figure 10. Off-State Leakage Current ($I_{NC(OFF)}$, $I_{NO(OFF)}$)

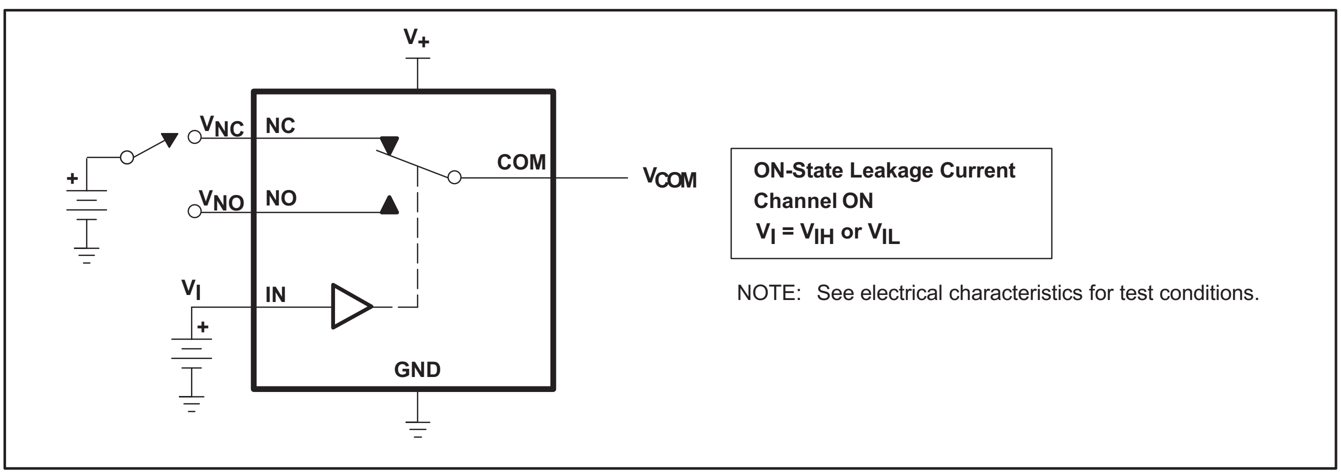


Figure 11. On-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$, $I_{NO(ON)}$)

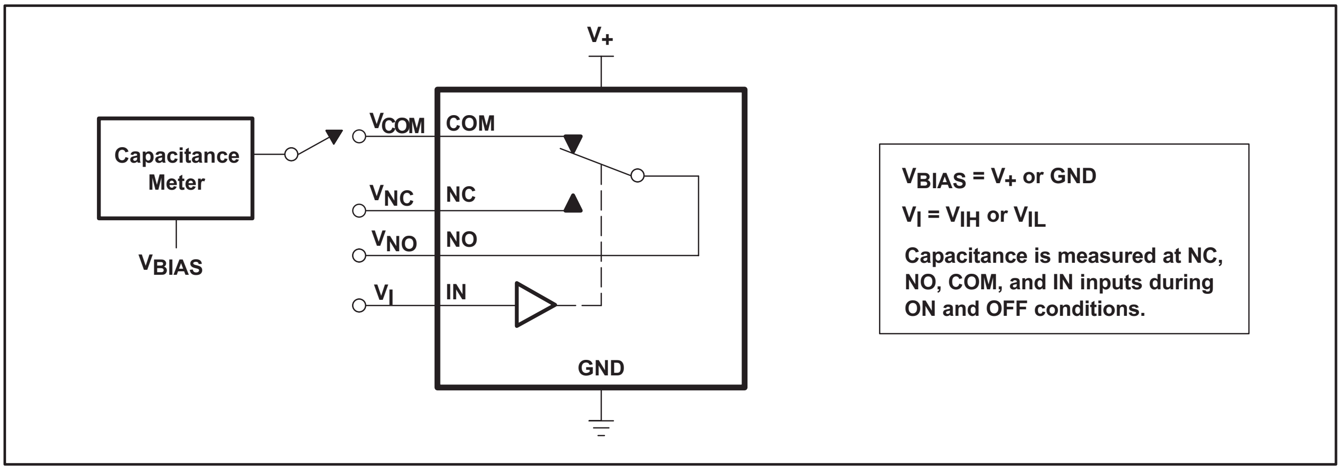
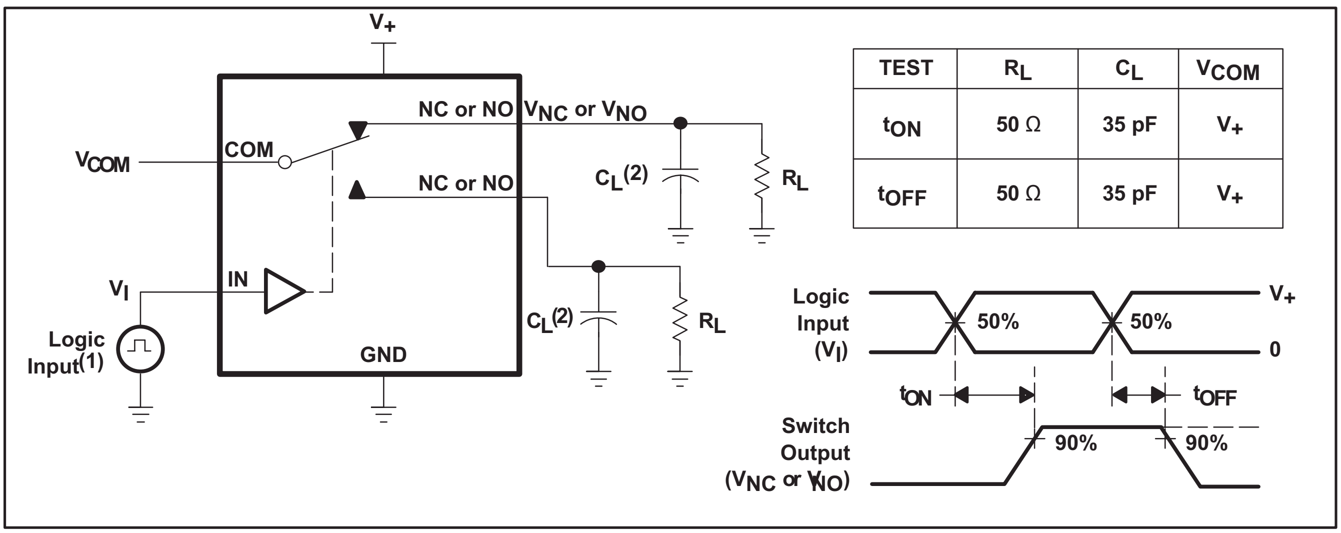


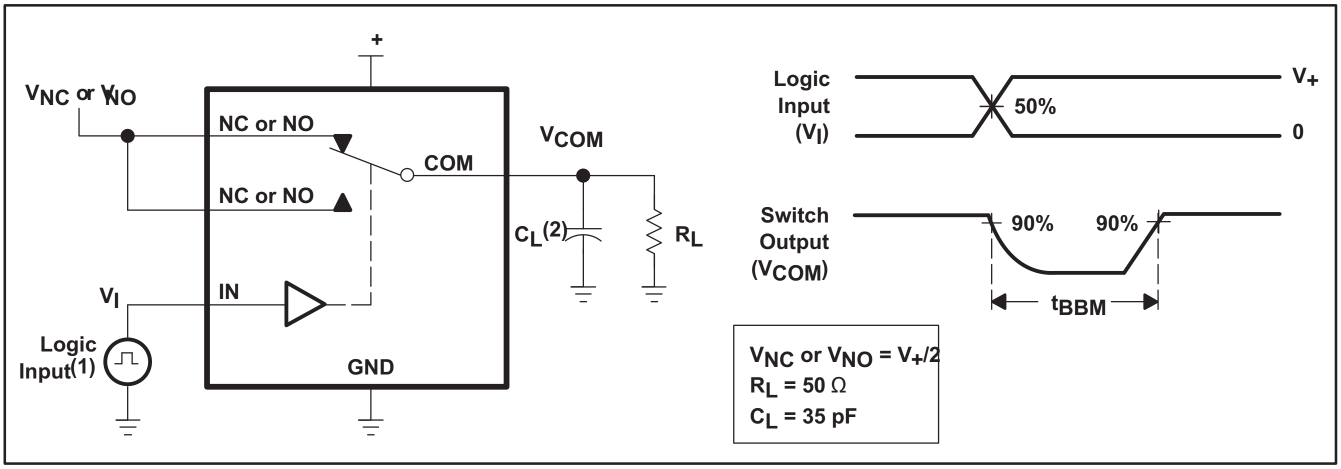
Figure 12. Capacitance (C_I, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NO(OFF)}$, $C_{NC(ON)}$, $C_{NO(ON)}$)



(1) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 13. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

Copyright © 2012–2016, Texas Instruments Incorporated



(1) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 14. Break-Before-Make Time (t_{BBM})

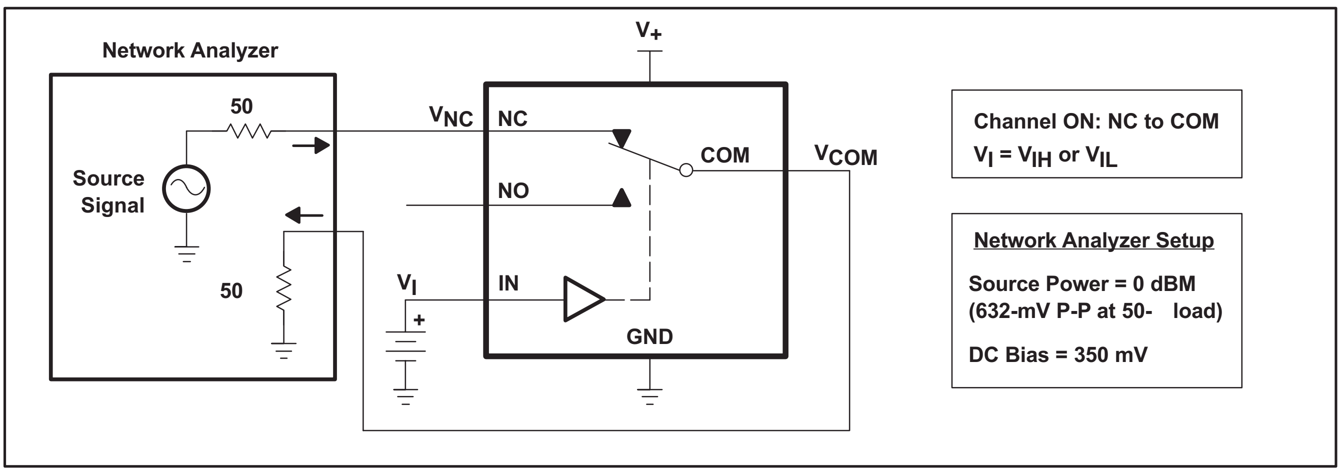


Figure 15. Bandwidth (BW)

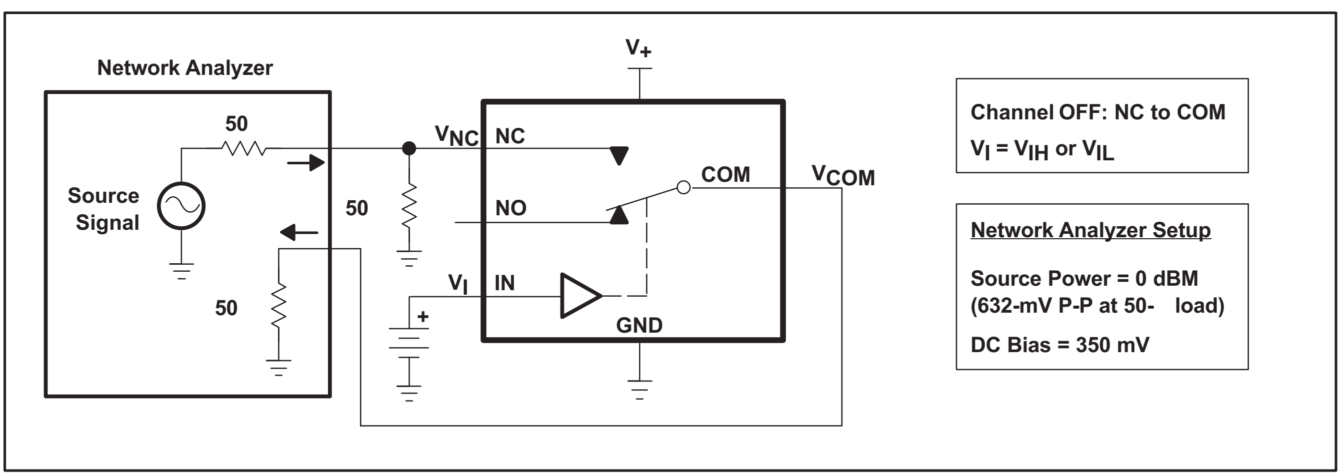


Figure 16. OFF Isolation (O_{ISO})

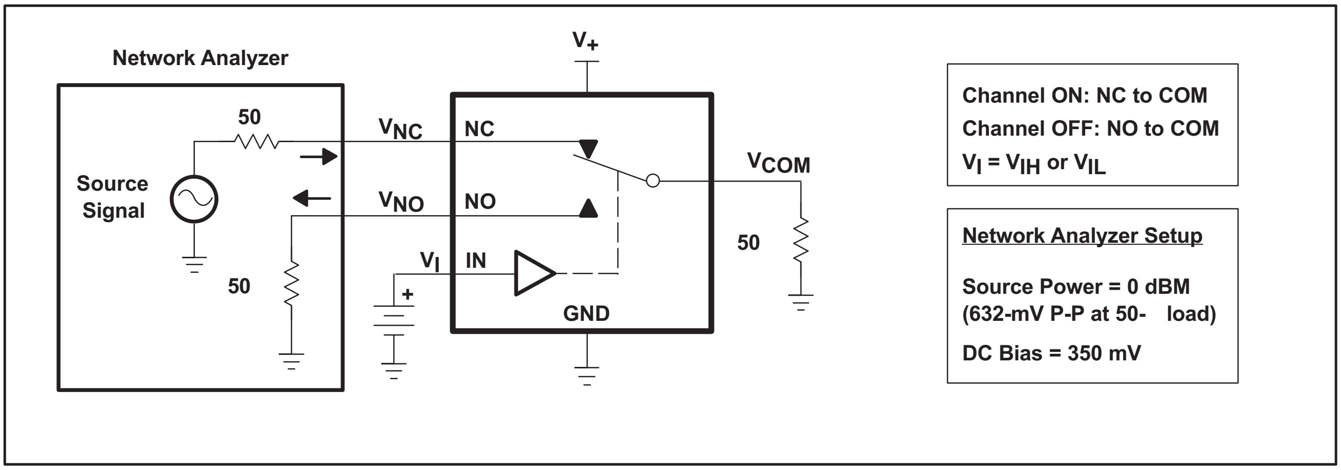
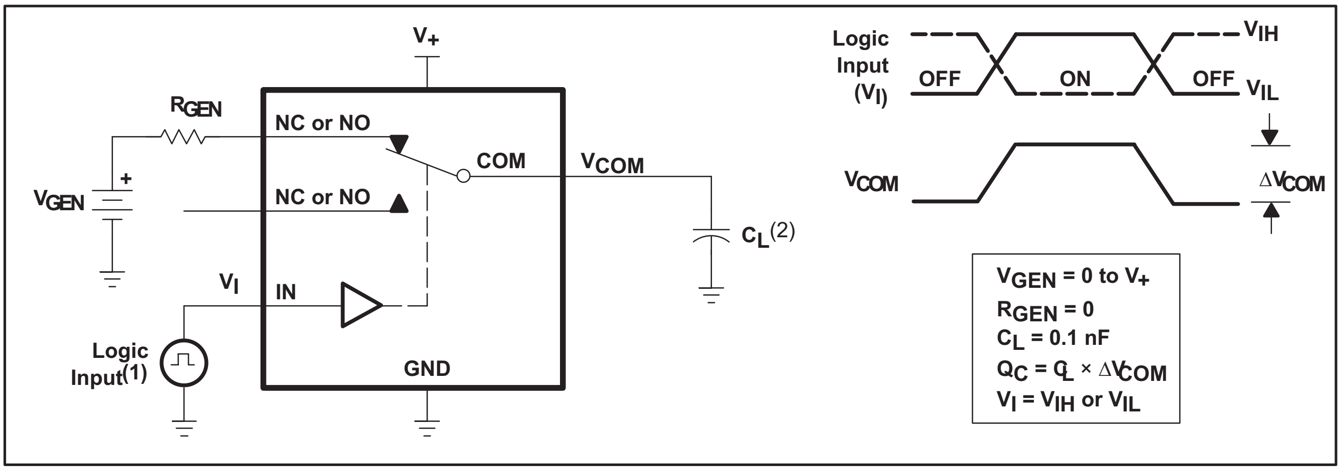
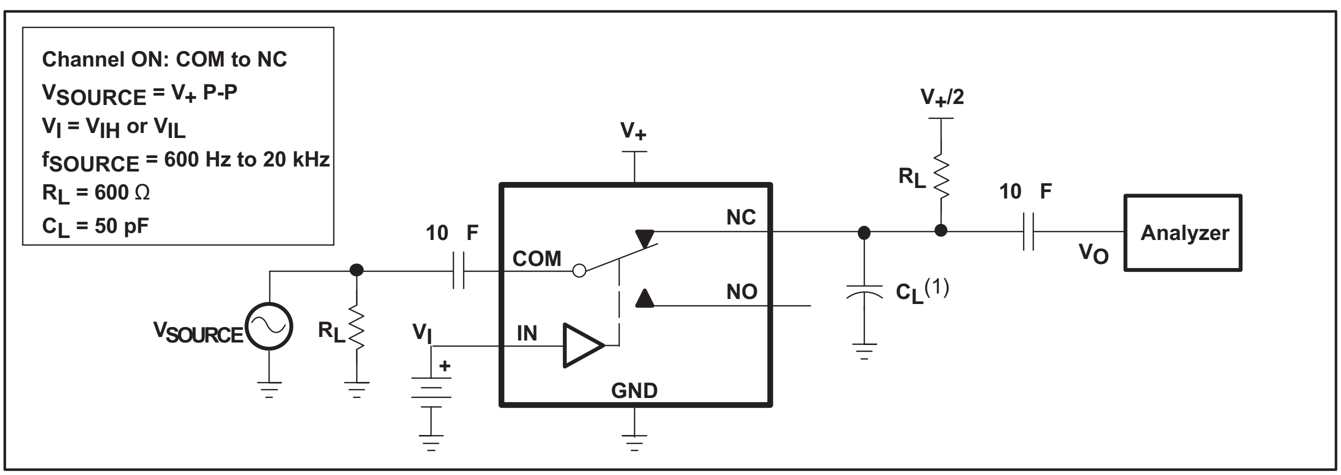


Figure 17. Crosstalk (X_{TALK})



(1) All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.
(2) C_L includes probe and jig capacitance.

Figure 18. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

Figure 19. Total Harmonic Distortion (THD)

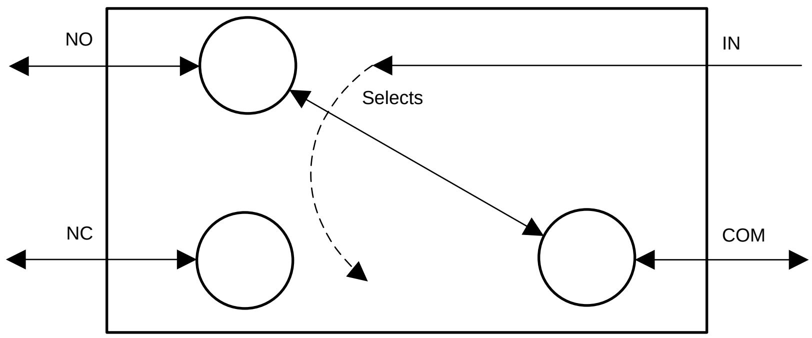
Copyright © 2012–2016, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The TS5A3159-Q1 is a single-pole double-throw (SPDT) analog switch designed to operate from 1.65 V to 5.5 V. Either the NO or the NC pin is shorted to the COM pin, depending on the logic level input to the IN pin.

8.2 Functional Block Diagram



8.3 Feature Description

The main feature of this device is the excellent total harmonic distortion performance and low power consumption. Additionally, the NO, NC, and COM pins can be used as either inputs or outputs.

Table 2. Summary Of Characteristics(1)

CONFIGURATION	2:1 MULTIPLEXER / DEMULTIPLEXER (1 × SPDT)
Number of channels	1
ON-state resistance (r_{on})	1.3 Ω
ON-state resistance match (Δr_{on})	0.1 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.15 Ω
Turn on/turn off time (t_{ON} / t_{OFF})	20 ns / 15 ns
Break-before-make time (t_{BBM})	12 ns
Charge injection (Q_C)	36 pC
Bandwidth (BW)	100 MHz
OFF isolation (O_{ISO})	–65 dB at 1 MHz
Crosstalk (X_{TALK})	–65 dB at 1 MHz
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{NO(OFF)}$ / $I_{NC(OFF)}$)	±6 nA
Package option	6-pin DBV

(1) V_+ = 5 V and T_A = 25°C

8.4 Device Functional Modes

Table 3 lists the functions for the TS5A3159-Q1 device.

Table 3. Function Table

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Analog switches are commonly used in battery powered applications to route audio signals. A typical use case is highlighted in Figure 20. The analog switch is supplied with 5 V and the control input is from a 5-V processor GPIO. In this case, there are no concerns related to excess power consumption.

9.2 Typical Application

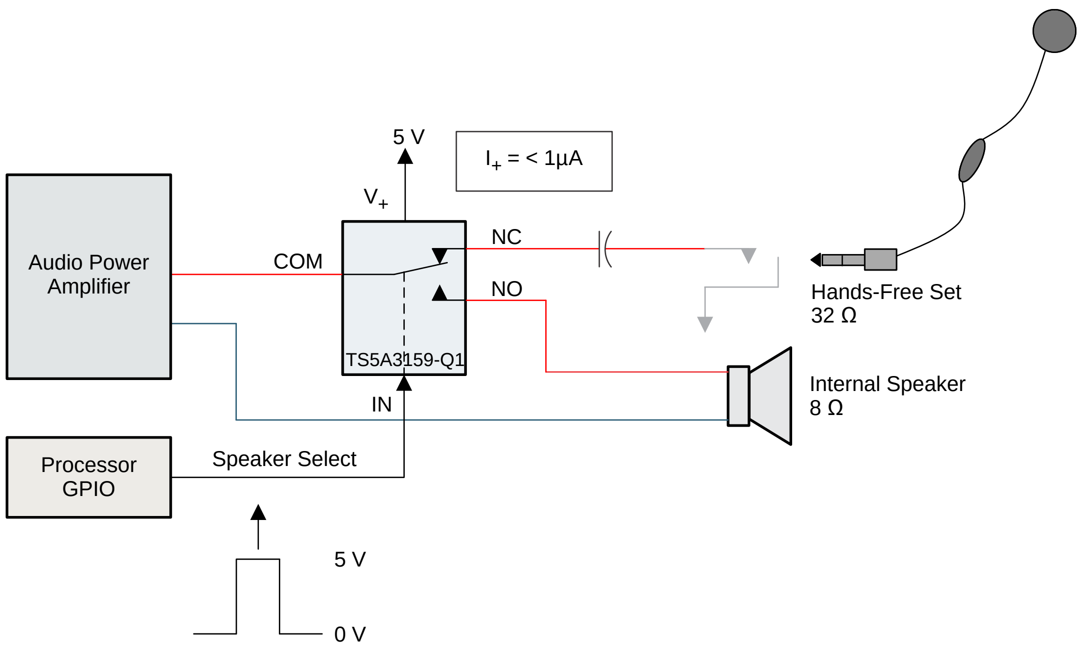


Figure 20. Typical Application Schematic

9.2.1 Design Requirements

In this application example, the device receives the control signal from a 5-V GPIO and common input from an Audio Power amplifier. The input is routed to either the Hands free set or the internal speaker depending upon the control signal.

9.2.2 Detailed Design Procedure

Since the control signal varies from 0 to 5 V (Vdd), there's no excess current consumption. However, if the control signal comes from lower voltage GPIOs while the V+ of TS5A3159 is connected to the battery whose voltage varies, it can lead to an excess current draw from the V+ suppl pin. Such a scenario requires the use of an external voltage level translator such as the SN74LVC1T45. For more information see *Preventing Excess Current Consumption on Analog Switches*, SCDA011.

Copyright © 2012–2016, Texas Instruments Incorporated

Typical Application (continued)

9.2.3 Application Curve

The ON state resistance of the switch is a critical parameter to measure since it helps select the right switch for the application. The on state resistance versus the common voltage can be seen in Figure 21.

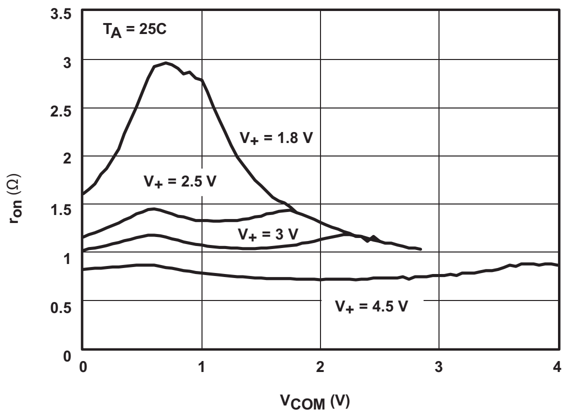


Figure 21. r_{on} vs V_{COM}

10 Power Supply Recommendations

Most systems have a common 3.3 V or 5 V rail that can supply the V+ pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) can supply this device from a higher voltage rail. Proper decouping of the supply rail is a must to avoid any spikes that may exceed the absolute ratings of the V+ pin of the device.

11 Layout

11.1 Layout Guidelines

TI recommends to keep signal lines as short as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω, as required by the application. Do not place this device too close to high voltage switching components, as they may cause interference.

11.2 Layout Example

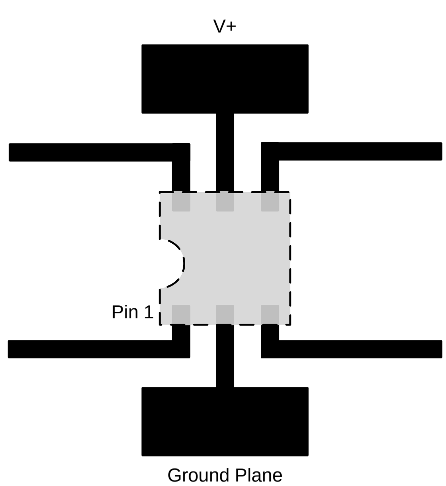


Figure 22. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Preventing Excess Current Consumption on Analog Switches, SCDA011

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2012–2016, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3159QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	UAAQ	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TS5A3159-Q1 :

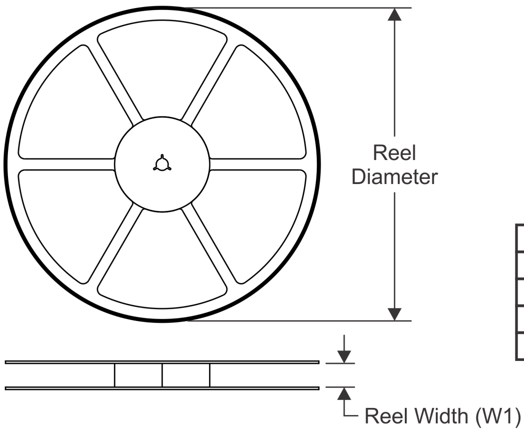
- Catalog: TS5A3159
- Enhanced Product: TS5A3159-EP

NOTE: Qualified Version Definitions:

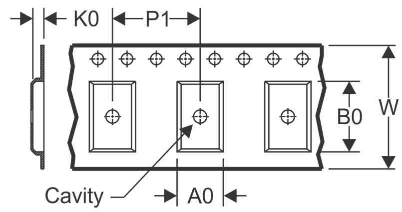
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

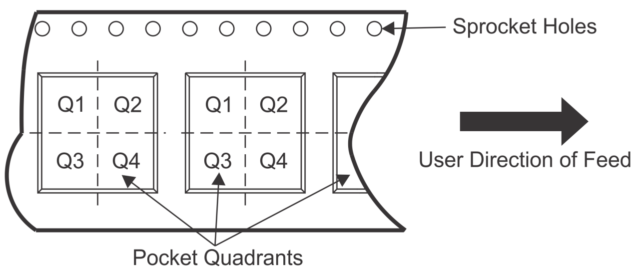


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

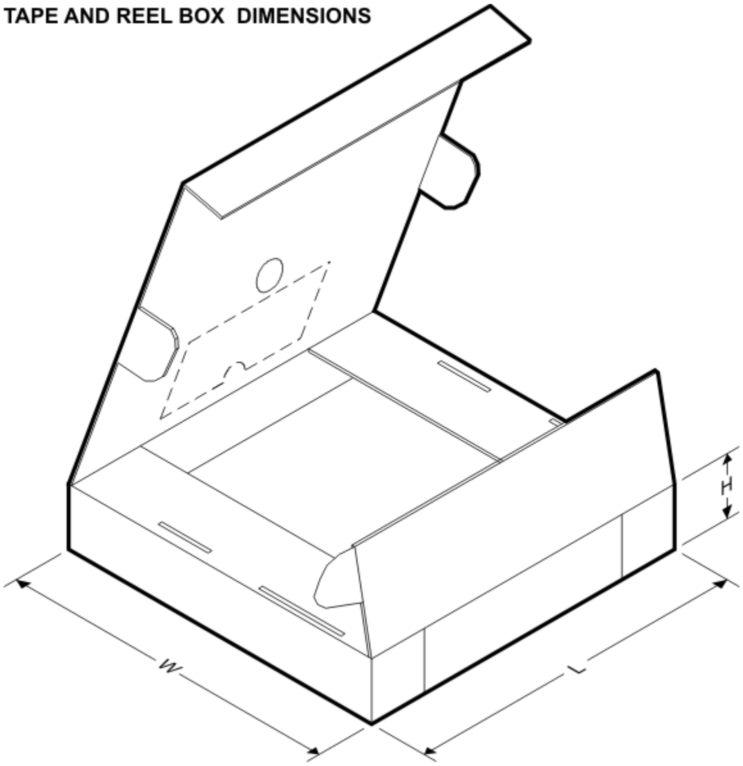
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3159QDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

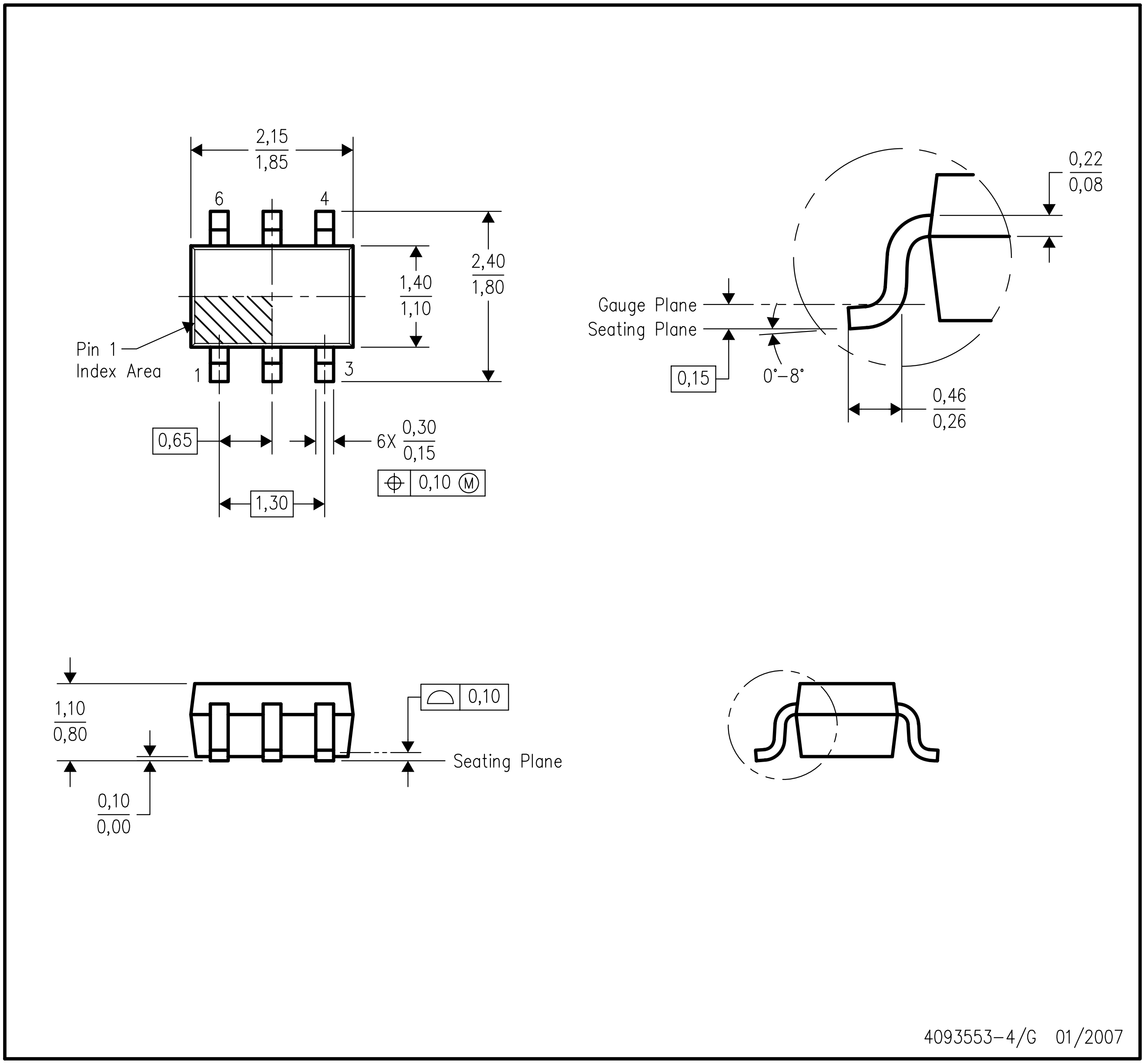
TAPE AND REEL BOX DIMENSIONS



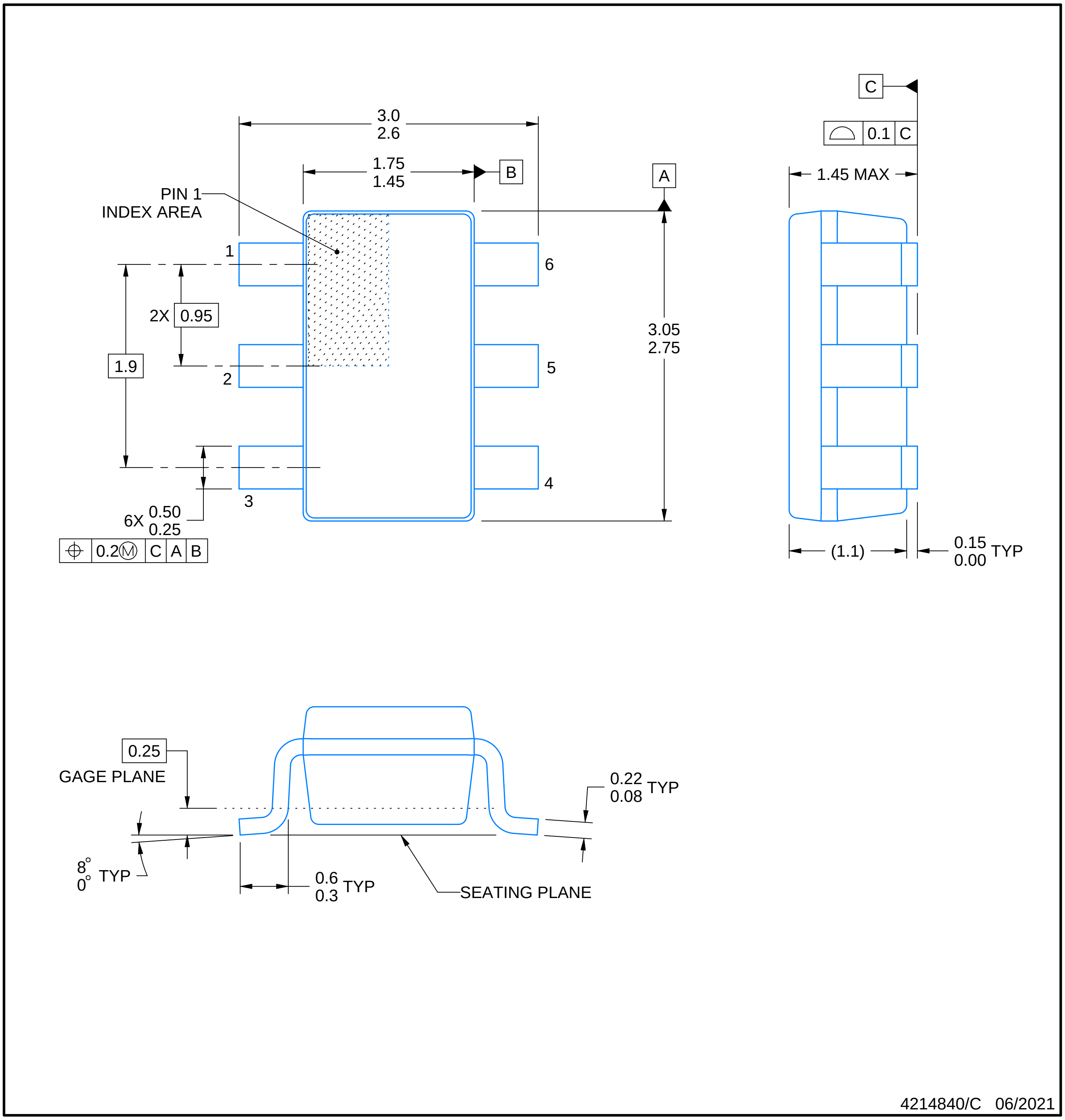
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3159QDBVRQ1	SOT-23	DBV	6	3000	202.0	201.0	28.0

DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE

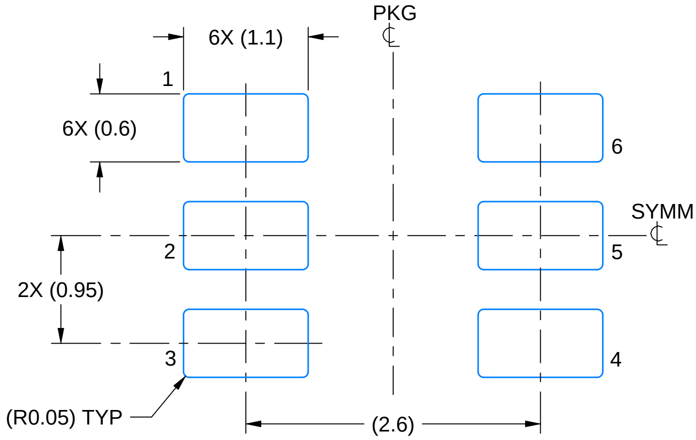


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

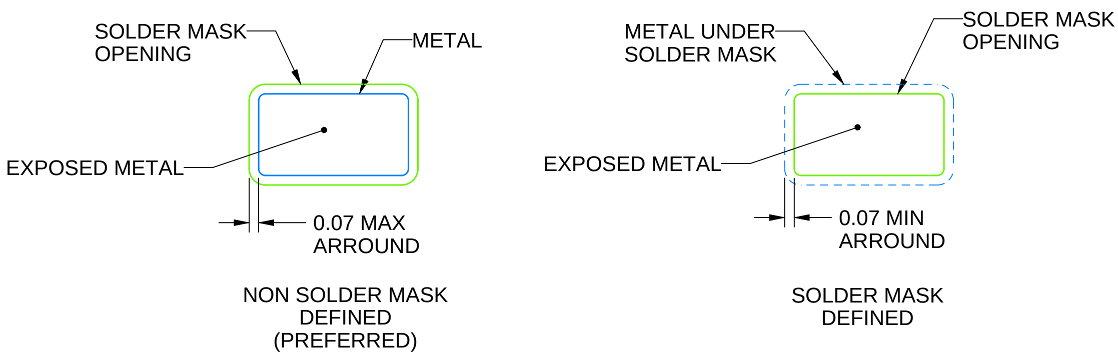


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

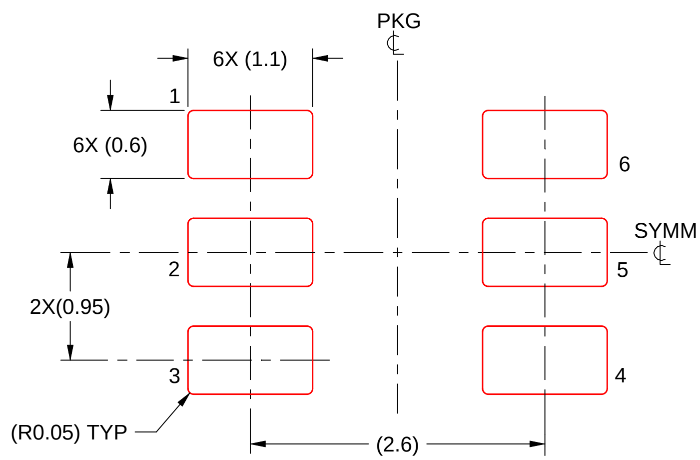


SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated