WM8958

Multi-Channel Audio Hub CODEC for Smartphones

DESCRIPTION

The WM8958[1] is a highly integrated ultra-low power hi-fi CODEC designed for smartphones and other portable devices rich in multimedia features.

An integrated stereo class D/AB speaker driver and class W headphone driver minimize power consumption during audio playback.

The device requires only two voltage supplies, with all other internal supply rails generated from integrated LDOs.

Stereo full duplex asynchronous sample rate conversion and multi-channel digital mixing combined with powerful analogue mixing allow the device to support a huge range of different architectures and use cases.

A multiband compressor and programmable parametric EQ provide volume maximisation and speaker compensation in the digital playback paths. The dynamic range controller can be used in record or playback paths for maintaining a constant signal level, maximizing loudness and protecting speakers against overloading and clipping.

A smart digital microphone interface provides power regulation, a low jitter clock output and decimation filters for up to four digital microphones. Microphone activity detection with interrupt is available. Impedance sensing and measurement is provided for external accessory / push-button detection.

Fully differential internal architecture and on-chip RF noise filters ensure a very high degree of noise immunity. Active ground loop noise rejection and DC offset correction help prevent pop noise and suppress ground noise on the headphone outputs.

FEATURES

- 24-bit 4-channel hi-fi DAC and 2-channel hi-fi ADC
- 100dB SNR during DAC playback ('A' weighted)
- Smart MIC interface
  - Power, clocking and data input for up to four digital MICs
  - High performance analogue MIC interface
  - MIC activity detect & interrupt allows processor to sleep
- 2W stereo (2 x 2W) class D/AB speaker driver
- Capless Class W headphone drivers
  - Integrated charge pump
  - 5.3mW total power for DAC playback to headphones
- 4 Line outputs (single-ended or differential)
- BTL Earpiece driver
- Digital audio interfaces for multi-processor architecture
  - Asynchronous stereo duplex sample rate conversion
  - Powerful mixing and digital loopback functions
- ReTune™ Mobile 5-band, 6-channel parametric EQ
- Multiband compressor and dynamic range controller
- Dual FLL provides all necessary clocks
  - Self-clocking modes allow processor to sleep
  - All standard sample rates from 8kHz to 96kHz
- Active noise reduction circuits
  - DC offset correction removes pops and clicks
  - Ground loop noise cancellation
- Integrated LDO regulators
- 72-ball W-CSP package (4.516 x 4.258 x 0.698mm)

APPLICATIONS

- Smartphones and music phones
- Portable navigation
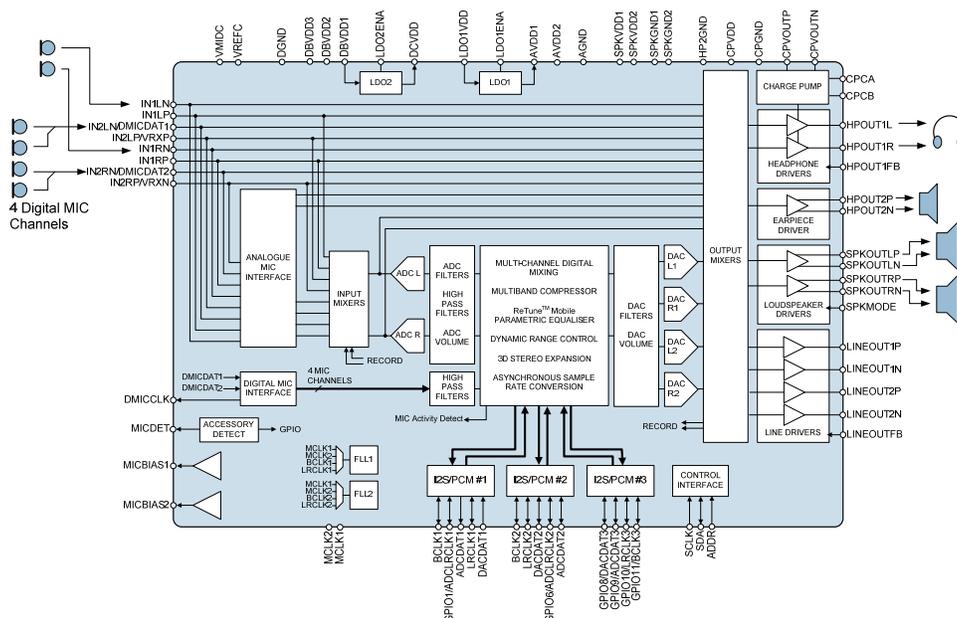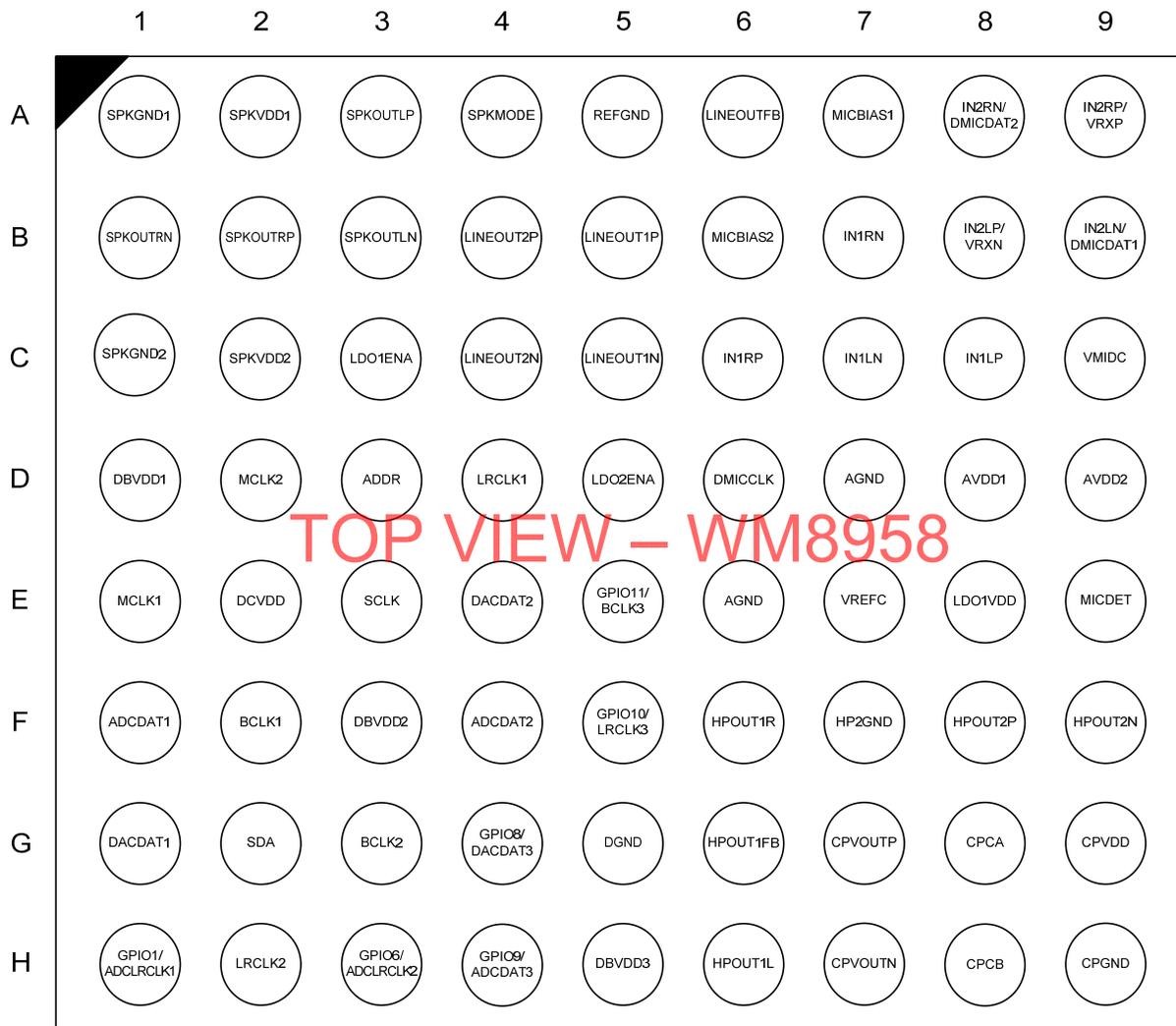- Tablets
- eBooks
- Portable Media Players

[1] This product is protected by Patents US 7,622,984, US 7,626,445,US 7,765,019 and GB 2,432,765

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PIN CONFIGURATION

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A	SPKGND1	SPKVDD1	SPKOUTLP	SPKMODE	REFGND	LINEOUTFB	MICBIAS1	IN2RN/ DMICDAT2	IN2RP/ VRXP
B	SPKOUTRN	SPKOUTRP	SPKOUTLN	LINEOUT2P	LINEOUT1P	MICBIAS2	IN1RN	IN2LP/ VRXN	IN2LN/ DMICDAT1
C	SPKGND2	SPKVDD2	LDO1ENA	LINEOUT2N	LINEOUT1N	IN1RP	IN1LN	IN1LP	VMIDC
D	DBVDD1	MCLK2	ADDR	LRCLK1	LDO2ENA	DMICCLK	AGND	AVDD1	AVDD2
E	MCLK1	DCVDD	SCLK	DACDAT2	GPIO11/ BCLK3	AGND	VREFC	LDO1VDD	MICDET
F	ADCDAT1	BCLK1	DBVDD2	ADCDAT2	GPIO10/ LRCLK3	HPOUT1R	HP2GND	HPOUT2P	HPOUT2N
G	DACDAT1	SDA	BCLK2	GPIO8/ DACDAT3	DGND	HPOUT1FB	CPVOUTP	CPCA	CPVDD
H	GPIO1/ ADCLRCLK1	LRCLK2	GPIO6/ ADCLRCLK2	GPIO9/ ADCDAT3	DBVDD3	HPOUT1L	CPVOUTN	CPCB	CPGND

TOP VIEW – WM8958

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8958ECS/R	-40°C to +85°C	72-ball W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:

Reel quantity = 5000

PIN DESCRIPTION

A description of each pin on the WM8958 is provided below.

Note that a table detailing the associated power domain for every input and output pin is provided on the following page.

Note that, where multiple pins share a common name, these pins should be tied together on the PCB.

PIN NO	NAME	TYPE	DESCRIPTION
F1	ADCDAT1	Digital Output	Audio interface 1 ADC digital audio data
F4	ADCDAT2	Digital Output	Audio interface 2 ADC digital audio data
D3	ADDR	Digital Input	2-wire (I2C) address select
D7, E6	AGND	Supply	Analogue ground (Return path for AVDD1, AVDD2 and LDO1VDD)
D8	AVDD1	Supply / Analogue Output	Analogue core supply / LDO1 Output
D9	AVDD2	Supply	Bandgap reference, analogue class D and FLL supply
F2	BCLK1	Digital Input / Output	Audio interface 1 bit clock
G3	BCLK2	Digital Input / Output	Audio interface 2 bit clock
G8	CPCA	Analogue Output	Charge pump fly-back capacitor pin
H8	CPCB	Analogue Output	Charge pump fly-back capacitor pin
H9	CPGND	Supply	Charge pump ground (Return path for CPVDD)
G9	CPVDD	Supply	Charge pump supply
H7	CPVOUTN	Analogue Output	Charge pump negative supply decoupling pin (HPOUT1L, HPOUT1R)
G7	CPVOUTP	Analogue Output	Charge pump positive supply decoupling pin (HPOUT1L, HPOUT1R)
G1	DACDAT1	Digital Input	Audio interface 1 DAC digital audio data
E4	DACDAT2	Digital Input / Output	Audio interface 2 DAC digital audio data
D1	DBVDD1	Supply	Digital buffer (I/O) supply (core functions and Audio Interface 1)
F3	DBVDD2	Supply	Digital buffer (I/O) supply (for Audio Interface 2)
H5	DBVDD3	Supply	Digital buffer (I/O) supply (for Audio Interface 3)
E2	DCVDD	Supply / Analogue Output	Digital core supply / LDO2 output
G5	DGND	Supply	Digital ground (Return path for DCVDD, DBVDD1, DBVDD2, DBVDD3)
D6	DMICCLK	Digital Output	Digital MIC clock output
H1	GPIO1/ ADCLRCLK1	Digital Input / Output	General Purpose pin GPIO 1 / Audio interface 1 ADC left / right clock
F5	GPIO10/ LRCLK3	Digital Input / Output	General Purpose pin GPIO 10 / Audio interface 3 left / right clock
E5	GPIO11/ BCLK3	Digital Input / Output	General Purpose pin GPIO 11 / Audio interface 3 bit clock
H3	GPIO6/ ADCLRCLK2	Digital Input / Output	General Purpose pin GPIO 6 / Audio interface 2 ADC left / right clock
G4	GPIO8/ DACDAT3	Digital Input / Output	General Purpose pin GPIO 8 / Audio interface 3 DAC digital audio data
H4	GPIO9/ ADCDAT3	Digital Input / Output	General Purpose pin GPIO 9 / Audio interface 3 ADC digital audio data
F7	HP2GND	Supply	Analogue ground
G6	HPOUT1FB	Analogue Input	HPOUT1L and HPOUT1R ground loop noise rejection feedback
H6	HPOUT1L	Analogue Output	Left headphone output
F6	HPOUT1R	Analogue Output	Right headphone output
F9	HPOUT2N	Analogue Output	Earpiece speaker inverted output
F8	HPOUT2P	Analogue Output	Earpiece speaker non-inverted output
C7	IN1LN	Analogue Input	Left channel single-ended MIC input / Left channel negative differential MIC input
C8	IN1LP	Analogue Input	Left channel line input / Left channel positive differential MIC input
B7	IN1RN	Analogue Input	Right channel single-ended MIC input / Right channel negative differential MIC input

PIN NO	NAME	TYPE	DESCRIPTION
C6	IN1RP	Analogue Input	Right channel line input / Right channel positive differential MIC input
B9	IN2LN/ DMICDAT1	Analogue Input / Digital Input	Left channel line input / Left channel negative differential MIC input / Digital MIC data input 1
B8	IN2LP/VRXN	Analogue Input	Left channel line input / Left channel positive differential MIC input / Mono differential negative input (RXVOICE -)
A8	IN2RN/ DMICDAT2	Analogue Input / Digital Input	Right channel line input / Right channel negative differential MIC input / Digital MIC data input 2
A9	IN2RP/VRXP	Analogue Input	Left channel line input / Left channel positive differential MIC input / Mono differential positive input (RXVOICE +)
C3	LDO1ENA	Digital Input	Enable pin for LDO1
E8	LDO1VDD	Supply	Supply for LDO1
D5	LDO2ENA	Digital Input	Enable pin for LDO2
C5	LINEOUT1N	Analogue Output	Negative mono line output / Positive left or right line output
B5	LINEOUT1P	Analogue Output	Positive mono line output / Positive left line output
C4	LINEOUT2N	Analogue Output	Negative mono line output / Positive left or right line output
B4	LINEOUT2P	Analogue Output	Positive mono line output / Positive left line output
A6	LINEOUTFB	Analogue Input	Line output ground loop noise rejection feedback
D4	LRCLK1	Digital Input / Output	Audio interface 1 left / right clock
H2	LRCLK2	Digital Input / Output	Audio interface 2 left / right clock
E1	MCLK1	Digital Input	Master clock 1
D2	MCLK2	Digital Input	Master clock 2
A7	MICBIAS1	Analogue Output	Microphone bias 1
B6	MICBIAS2	Analogue Output	Microphone bias 2
E9	MICDET	Analogue Input	Microphone & accessory sense input
A5	REFGND	Supply	Analogue ground
E3	SCLK	Digital Input	Control interface clock input
G2	SDA	Digital Input / Output	Control interface data input and output / acknowledge output
A1	SPKGND1	Supply	Ground for speaker driver (Return path for SPKVDD1)
C1	SPKGND2	Supply	Ground for speaker driver (Return path for SPKVDD2)
A4	SPKMODE	Digital Input	Mono / Stereo speaker mode select
B3	SPKOUTLN	Analogue Output	Left speaker negative output
A3	SPKOUTLP	Analogue Output	Left speaker positive output
B1	SPKOUTRN	Analogue Output	Right speaker negative output
B2	SPKOUTRP	Analogue Output	Right speaker positive output
A2	SPKVDD1	Supply	Supply for speaker driver 1 (Left channel)
C2	SPKVDD2	Supply	Supply for speaker driver 2 (Right channel)
C9	VMIDC	Analogue Output	Midrail voltage decoupling capacitor
E7	VREFC	Analogue Output	Bandgap reference decoupling capacitor

The following table identifies the power domain and ground reference associated with each of the input / output pins.

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
F1	ADCDAT1	DBVDD1	DGND
F4	ADCDAT2	DBVDD2	DGND
D3	ADDR	DBVDD1	DGND
F2	BCLK1	DBVDD1	DGND
G3	BCLK2	DBVDD2	DGND
G1	DACDAT1	DBVDD1	DGND
E4	DACDAT2	DBVDD2	DGND
D6	DMICCLK	MICBIAS1	AGND
H1	GPIO1/ADCLRCLK1	DBVDD1	DGND
H3	GPIO6/ADCLRCLK2	DBVDD2	DGND
G4	GPIO8/DACDAT3	DBVDD3	DGND
H4	GPIO9/ADCDAT3	DBVDD3	DGND
F5	GPIO10/LRCLK3	DBVDD3	DGND
E5	GPIO11/BCLK3	DBVDD3	DGND
H6	HPOUT1L	CPVOUTP, CPVOUTN	CPGND
F6	HPOUT1R	CPVOUTP, CPVOUTN	CPGND
F9	HPOUT2N	AVDD1	HP2GND
F8	HPOUT2P	AVDD1	HP2GND
C7	IN1LN	AVDD1	AGND
C8	IN1LP	AVDD1	AGND
B7	IN1RN	AVDD1	AGND
C6	IN1RP	AVDD1	AGND
B9	IN2LN/DMICDAT1	AVDD1 (IN2LN) or MICBIAS1 (DMICDAT1)	AGND
B8	IN2LP/VRXN	AVDD1	AGND
A8	IN2RN/DMICDAT2	AVDD1 (IN2RN) or MICBIAS1 (DMICDAT2)	AGND (IN2RN) or DGND (DMICDAT2)
A9	IN2RP/VRXP	AVDD1	AGND
C3	LDO1ENA	DBVDD1	DGND
D5	LDO2ENA	DBVDD1	DGND
C5	LINEOUT1N	AVDD1	AGND
B5	LINEOUT1P	AVDD1	AGND
C4	LINEOUT2N	AVDD1	AGND
B4	LINEOUT2P	AVDD1	AGND
D4	LRCLK1	DBVDD1	DGND
H2	LRCLK2	DBVDD2	DGND
E1	MCLK1	DBVDD1	DGND
D2	MCLK2	DBVDD1	DGND
E9	MICDET	MICBIAS2	AGND
E3	SCLK	DBVDD1	DGND
G2	SDA	DBVDD1	DGND
A4	SPKMODE	DBVDD1	DGND
B3	SPKOUTLN	SPKVDD1	SPKGND1
A3	SPKOUTLP	SPKVDD1	SPKGND1
B1	SPKOUTRN	SPKVDD2	SPKGND2
B2	SPKOUTRP	SPKVDD2	SPKGND2

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (AVDD1, DBVDD2, DBVDD3)	-0.3V	+4.5V
Supply voltages (AVDD2, DCVDD, DBVDD1)	-0.3V	+2.5V
Supply voltages (CPVDD)	-0.3V	+2.2V
Supply voltages (SPKVDD1, SPKVDD2, LDO1VDD)	-0.3V	+7.0V
Voltage range digital inputs (DBVDD1 domain)	AGND -0.3V	DBVDD1 +0.3V
Voltage range digital inputs (DBVDD2 domain)	AGND -0.3V	DBVDD2 +0.3V
Voltage range digital inputs (DBVDD3 domain)	AGND -0.3V	DBVDD3 +0.3V
Voltage range digital inputs (DMICDATn)	AGND - 0.3V	AVDD1 + 0.3V
Voltage range analogue inputs (AVDD1 domain)	AGND -0.3V	AVDD1 +0.3V
Voltage range analogue inputs (MICDET, LINEOUTFB)	AGND - 0.3V	AVDD1 + 0.3V
Voltage range analogue inputs (HPOUT1FB)	AGND - 0.3V	AGND + 0.3V
Ground (DGND, CPGND, SPKGND1, SPKGND2, REFGND, HP2GND)	AGND - 0.3V	AGND + 0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core) See notes 7,8	DCVDD	1.08	1.2	2.0	V
Digital supply range (I/O)	DBVDD1	1.62	1.8	2.0	V
Digital supply range (I/O)	DBVDD2, DBVDD3	1.62	1.8	3.6	V
Analogue supply 1 range See notes 3,4,5,6	AVDD1	2.4	3.0	3.3	V
Analogue supply 2 range	AVDD2	1.71	1.8	2.0	V
Charge Pump supply range	CPVDD	1.71	1.8	2.0	V
Speaker supply range	SPKVDD1, SPKVDD2	2.7	5.0	5.5	V
LDO1 supply range	LDO1VDD	2.7	5.0	5.5	V
Ground	DGND, AGND, CPGND, SPKGND1, SPKGND2, REFGND, HP2GND		0		V
Power supply rise time (notes 6, 7 and 8)	All supplies	1			µs
Operating temperature range	T_A	-40		85	°C

Notes:

1. Analogue, digital and speaker grounds must always be within 0.3V of AGND..

2. There is no power sequencing requirement; the supplies may be enabled in any order.

3. AVDD1 must be less than or equal to SPKVDD1 and SPKVDD2.

4. An internal LDO (powered by LDO1VDD) can be used to provide the AVDD1 supply.

5. When AVDD1 is supplied externally (not from LDO1), the LDO1VDD voltage must be greater than or equal to AVDD1.

6. The WM8958 can operate with AVDD1 tied to 0V; power consumption may be reduced, but the analogue audio functions will not be supported.

7. An internal LDO (powered by DBVDD1) can be used to provide the DCVDD supply.

8. When DCVDD is supplied externally (not from LDO2), the DBVDD1 voltage must be greater than or equal to DCVDD.

9. DCVDD and AVDD1 minimum rise times do not apply when these domains are powered using the internal LDOs.

10. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Wolfson strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed (see "Applications Information" section).

11. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

DEVICE DESCRIPTION

The WM8958 is a low power, high quality audio codec designed to interface with a wide range of processors and analogue components. A high level of mixed-signal integration in a very small footprint makes it ideal for portable applications such as mobile phones. Fully differential internal architecture and on-chip RF noise filters ensure a very high degree of noise immunity.

Three sets of audio interface pins are available in order to provide independent and fully asynchronous connections to multiple processors, typically an application processor, baseband processor and wireless transceiver. Any two of these interfaces can operate totally independently and asynchronously while the third interface can be synchronised to either of the other two and can also provide ultra low power loopback modes to support, for example, wireless headset voice calls.

Four digital microphone input channels are available to support advanced multi-microphone applications such as noise cancellation. An integrated microphone activity monitor is available to enable the processor to sleep during periods of microphone inactivity, saving power.

Four DAC channels are available to support use cases requiring up to four simultaneous digital audio streams to the output drivers.

Eight highly flexible analogue inputs allow interfacing to up to four microphone inputs (single-ended or differential), plus multiple stereo or mono line inputs. Connections to an external voice CODEC, FM radio, line input, handset MIC and headset MIC are all fully supported. Signal routing to the output mixers and within the CODEC has been designed for maximum flexibility to support a wide variety of usage modes. A 'Direct Voice' path from a voice CODEC directly to the Speaker or Earpiece output drivers is included.

Nine analogue output drivers are integrated, including a stereo pair of high power, high quality Class D/AB switchable speaker drivers; these can support 2W each in stereo mode. It is also possible to configure the speaker drivers as a mono output, giving enhanced performance. A mono earpiece driver is provided, providing output from the output mixers or from the low-power differential 'Direct Voice' path.

One pair of ground-referenced headphone outputs is provided; these are powered from an integrated Charge Pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. A DC Servo circuit is available for DC offset correction, thereby suppressing pops and reducing power consumption. Four line outputs are provided, with multiple configuration options including 4 x single-ended output or 2 x differential outputs. The line outputs are suitable for output to a voice CODEC, an external speaker driver or line output connector. Ground loop feedback is available on the headphone outputs and the line outputs, providing rejection of noise on the ground connections. All outputs have integrated pop and click suppression features.

Internal differential signal routing and amplifier configurations have been optimised to provide the highest performance and lowest possible power consumption for a wide range of usage scenarios, including voice calls and music playback. The speaker drivers offer low leakage and high PSRR; this enables direct connection to a Lithium battery. The speaker drivers provide eight levels of AC and DC gain to allow output signal levels to be maximised for many commonly-used SPKVDD/AVDD1 combinations.

The ADCs and DACs are of hi-fi quality, using a 24-bit low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports mixed sample rates, whilst integrated ultra-low power dual FLLs provide additional flexibility. A high pass filter is available in all ADC and digital MIC paths for removing DC offsets and suppressing low frequency noise such as mechanical vibration and wind noise. A digital mixing path from the ADC or digital MICs to the DAC provides a sidetone of enhanced quality during voice calls. DAC soft mute and un-mute is available for pop-free music playback.

The integrated Multiband Compressors (MBC), Dynamic Range Controllers (DRC) and ReTune[TM] Mobile 5-band parametric equaliser (EQ) provide further processing capability of the digital audio paths. The MBC enables the loudness of the digital playback path to be maximised without overdriving the loudspeakers. The RMS Limiter within the MBC function enables the maximum signal level to be matched to the application requirements and/or power rating of the loudspeaker. The DRC provides compression and signal level control to improve the handling of unpredictable signal levels. 'Anti-clip' and 'quick release' algorithms improve intelligibility in the presence of transients and impulsive noises. The EQ provides the capability to tailor the audio path according to the frequency characteristics of an earpiece or loudspeaker, and/or according to user preferences.

The WM8958 has highly flexible digital audio interfaces, supporting a number of protocols, including I^2S, DSP, MSB-first left/right justified, and can operate in master or slave modes. PCM operation is supported in the DSP mode. A-law and μ-law companding are also supported. Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power. The four digital MIC and ADC channels and four DAC channels are available via four TDM channels on Digital Audio Interface 1 (AIF1).

A powerful digital mixing core allows data from each TDM channel of each audio interface and from the ADCs and digital MICs to be mixed and re-routed back to a different audio interface and to the 4 DAC output channels. The digital mixing core can operate synchronously with either Audio Interface 1 or Audio Interface 2, with asynchronous stereo full duplex sample rate conversion performed on the other audio interface as required.

The system clock (SYSCLK) provides clocking for the ADCs, DACs, DSP core, digital audio interface and other circuits. SYSCLK can be derived directly from one of the MCLK1 or MCLK2 pins or via one of two integrated FLLs, providing flexibility to support a wide range of clocking schemes, including self-clocking FLL modes. Typical portable system MCLK frequencies, and sample rates from 8kHz to 96kHz are all supported. A low frequency (eg. 32.768kHz) clock can be used as the input reference to the FLLs, providing further flexibility. Automatic configuration of the clocking circuits is available, derived from the sample rate and from the MCLK / SYSCLK ratio.

The WM8958 uses a standard 2-wire control interface, providing full software control of all features, together with device register readback. An integrated Control Write Sequencer enables automatic scheduling of control sequences; commonly-used signal configurations may be selected using ready-programmed sequences, including time-optimised control of the WM8958 pop suppression features. It is an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications.

Versatile GPIO functionality is provided, with support for button/accessory detect inputs, or for clock, system status, or programmable logic level output for control of additional external circuitry. Interrupt logic, status readback and de-bouncing options are supported within this functionality.
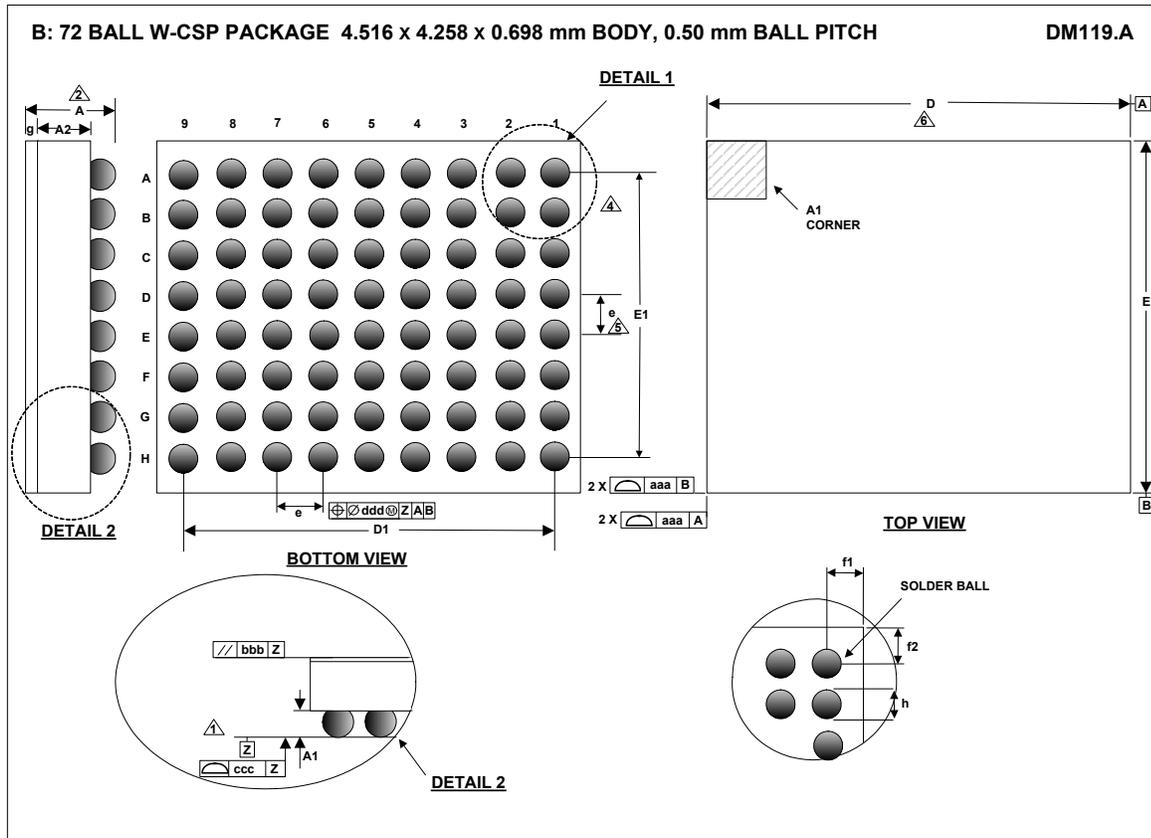
RECOMMENDED EXTERNAL COMPONENTS
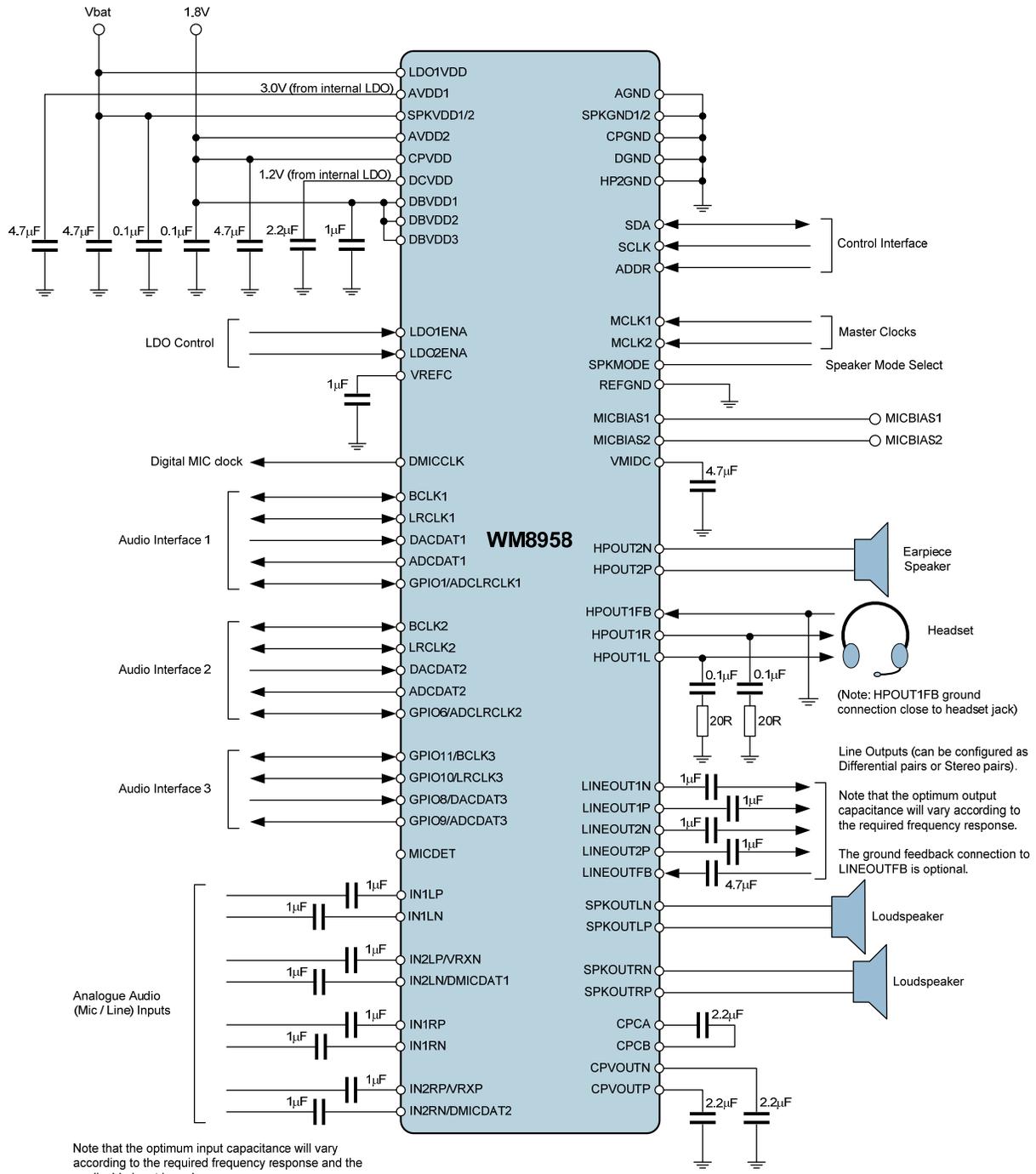
Note that the optimum input capacitance will vary according to the required frequency response and the applicable input impedance.

Note that input capacitors are not required for connection to Digital Microphone (DMIC) components.

PACKAGE DIMENSIONS

B: 72 BALL W-CSP PACKAGE 4.516 x 4.258 x 0.698 mm BODY, 0.50 mm BALL PITCH   **DM119.A**

Symbols	Dimensions (mm)			NOTE
	MIN	**NOM**	**MAX**	
A	0.658	0.698	0.738	
A1	0.206	0.242	0.278	
A2	0.418	0.434	0.450	
D	4.491	4.516	4.541	
D1		4.00 BSC		
E	4.233	4.258	4.283	
E1		3.50 BSC		
e		0.50 BSC		5
f1	0.246			8
f2	0.367			9
g		0.022		
h	0.264	0.314	0.364	
aaa		0.025		
bbb		0.060		
ccc		0.030		
ddd		0.015		

NOTES:
1. PRIMARY DATUM -Z- AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
2. THIS DIMENSION INCLUDES STAND-OFF HEIGHT 'A1' AND BACKSIDE COATING.
3. A1 CORNER IS IDENTIFIED BY INK/LASER MARK ON TOP PACKAGE.
4. BILATERAL TOLERANCE ZONE IS APPLIED TO EACH SIDE OF THE PACKAGE BODY.
5. 'e' REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
6. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
7. FOLLOWS JEDEC DESIGN GUIDE MO-211-C.
8. f1 = NOMINAL DISTANCE OF BALL CENTRE TO DIE EDGE X AXIS (AS PER POD) – APPLICABLE TO ALL CORNERS OF DIE.
9. f2 = NOMINAL DISTANCE OF DIE CENTRE TO DIE EDGE IN Y AXIS (AS PER POD) – APPLICABLE TO ALL CORNERS OF DIE.

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Testing and other quality control techniques are utilised to the extent Wolfson deems necessary to support its warranty. Specific testing of all parameters of each device is not necessarily performed unless required by law or regulation.

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REVISION HISTORY

DATE	REV	DESCRIPTION OF CHANGES
27/09/10	2.0	Initial version
14/10/10	2.1	Tablets, EBooks and PMP added to Applications
04/04/11	2.2	2W Stereo (into 4ohms) now specified. Noted RF suppression on analogue inputs. Reel order quantity updated
07/04/11	3.0	Revision updated to reflect datasheet revision / production status change
04/10/11	3.1	Pin Description table re-ordered (by Pin Name), noting that any pins with a common name (eg. AGND) should be tied together on the PCB. Added Table of Contents
25/04/12	3.1	Front page updated
25/04/12	3.1	Power domain table added, p6
25/04/12	3.1	Additional details in Absolute Maximum Ratings.
25/04/12	3.1	Recommended Operating Conditions updated
25/04/12	3.1	Device Description, 10th para updated.
09/08/12	3.2	Package Diagram changed to DM119.A