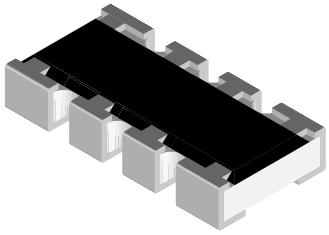
Professional Thin Film Chip Resistor Array



FEATURES

- Advanced thin film technology
- Two pairs or four equal resistor values
- TCR down to ± 25 ppm/K
- Tolerance down to ± 0.5 %
- Pure Sn termination on Ni barrier layer
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

APPLICATIONS

- Voltage divider
- Feedback circuits
- Signal conditioning

The ACAS 0612 thin film chip resistor arrays combine the proven reliability of professional thin film chip resistor products with the advantages of chip resistor arrays. A small package enables the design of high density circuits in combination with reduction of assembly costs. Four equal resistor values or two pairs are available.

TECHNICAL SPECIFICATIONS

DESCRIPTION	ACAS 0612
EIA size	0612
Metric size	RR1632M
Configuration, isolated	4 x 0603
Design:	
All equal	AE
Two pairs	TP
Resistance values	47 Ω to 221 kΩ (1)
Absolute tolerance (2)	± 1 %; ± 0.5 %
Absolute temperature coefficient (2)	± 50 ppm/K; ± 25 ppm/K
Max. resistance ratio $R_{min.}/R_{max.}$	1:10
Rated dissipation: P_{70}	
Element	0.1 W
Package, 4 x 0603	0.3 W
Operating voltage	75 V
Permissible film temperature	125 °C
Operating temperature range	- 55 °C to 125 °C
Insulation voltage (U_{ins}) against ambient and between isolated resistors, continuous	75 V

Notes

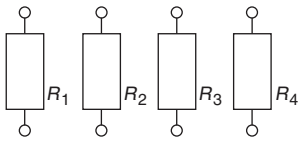
(1) Resistance values to be selected from E24; E192.

(2) For specified TCR tracking, tolerance matching and even tighter absolute tolerance and TCR please refer to data sheet ACAS 0612 - Precision available on our web site at www.vishay.com/doc?28751.

APPLICATION INFORMATION

The power dissipation on the resistor generates a temperature rise against the local ambient, depending on the heat flow support of the printed-circuit board (thermal resistance). The rated dissipation applies only if the permitted film temperature is not exceeded. These resistors do not feature a limited lifetime when operated within the permissible limits.

CIRCUITS



ACAS 0612

DESIGN

	ACAS 0612
AE	$R_1 = R_2 = R_3 = R_4$
TP	$R_1 = R_4 < R_2 = R_3$

PART NUMBER AND PRODUCT DESCRIPTION

Part Number: ACASA110012200P500

A	C	A	S	A	1	1	0	0	1	2	2	0	0	P	5	0	0

MODEL/ SIZE	TERMINAL	SIZE	RESISTANCE (1)	ACCURACY GRADE (2)	RESISTANCE (1)	PACKAGING	SPECIAL
ACA	**S** = Convex square	**A** = 0612	**3 digit resistance value R_1, R_4 1 digit multiplier** MULTIPLIER **9** = $*10^{-1}$ **0** = $*10^{0}$ **1** = $*10^{1}$ **2** = $*10^{2}$ **3** = $*10^{3}$	TCR and tolerance **1** **2** **3**	**3 digit resistance value R_2, R_3 1 digit multiplier** MULTIPLIER **9** = $*10^{-1}$ **0** = $*10^{0}$ **1** = $*10^{1}$ **2** = $*10^{2}$ **3** = $*10^{3}$	**P1** **P5**	**00** = Standard

Product Description: ACAS 0612 110R 1 220R P5

ACA	S	0612	110R	1	220R	P5
MODEL/SIZE	TERMINATION	SIZE	RESISTANCE R_1, R_4 (1)	ACCURACY GRADE (2)	RESISTANCE R_2, R_3 (1)	PACKAGING
ACA = Chip Array	**S** = Convex square	**0612**	**110R** = 110 Ω **1K1** = 1.1 kΩ **22K1** = 22.1 kΩ	TCR and tolerance **1** **2** **3**	**220R** = 220 Ω **1K1** = 1.1 kΩ **22K1** = 22.1 kΩ	**P1** **P5**

Notes

- Products can be ordered using either the PART NUMBER or the PRODUCT DESCRIPTION.

(1) $R_1 = R_4 \leq R_2 = R_3$.

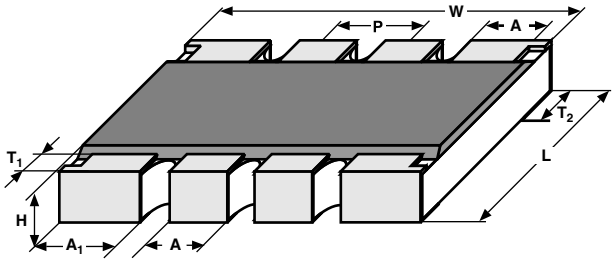
(2) Please refer to the table TEMPERATURE COEFFICIENT AND RESISTANCE RANGE, see next page.

(3) Please refer to the table PACKAGING, see next page.

TEMPERATURE COEFFICIENT AND RESISTANCE RANGE						
TYPE	ACCURACY GRADE	ABSOLUTE		RELATIVE		RESISTANCE VALUE
		TCR	TOLERANCE	TCR	TOLERANCE	
ACAS 0612	1	± 25 ppm/K	± 0.5 %	-	-	47 Ω to 221 kΩ
	2	± 50 ppm/K	± 0.5 %	-	-	47 Ω to 221 kΩ
	3	± 50 ppm/K	± 1 %	-	-	47 Ω to 221 kΩ

PACKAGING						
TYPE	CODE	QUANTITY	PACKAGING STYLE	WIDTH	PITCH	REEL DIAMETER
ACAS 0612	P1	1000	Tape and reel cardboard tape acc. IEC 60286-3 Type I	8 mm	4 mm	180 mm/7"
	P5	5000				

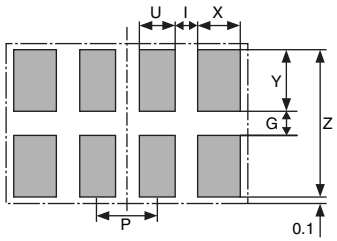
DIMENSIONS



DIMENSIONS - Chip resistor array, mass and relevant physical dimensions									
TYPE	L (mm)	W (mm)	H (mm)	P (mm)	A_1 (mm)	A (mm)	T_1 (mm)	T_2 (mm)	MASS (mg)
ACAS 0612	1.5 ± 0.15	3.2 ± 0.15	0.45 ± 0.1	0.8 ± 0.1	0.6 ± 0.1	0.4 ± 0.1	0.3 ± 0.15	0.4 ± 0.15	6.6

PATTERN STYLES FOR CHIP RESISTOR ARRAY

ACAS 0612



Dimensions in mm
limits for solder resist

RECOMMENDED SOLDER PAD DIMENSIONS FOR CHIP RESISTOR ARRAYS							
TYPE	G (mm)	Y (mm)	X (mm)	U (mm)	Z (mm)	I (mm)	P (mm)
ACAS 0612	0.7	0.7	0.64	0.5	2.1	0.3	0.8

DESCRIPTION

The production of the components is strictly controlled and follows an extensive set of instructions established for reproducibility. A homogeneous film of metal alloy is deposited on a high grade (Al_2O_3) ceramic substrate using a mask to separate the adjacent resistors and conditioned to achieve the desired temperature coefficient. Specially designed inner contacts are realized on both sides. A special laser is used to achieve the target value by smoothly cutting a meander groove in the resistive layer without damaging the ceramics.

The resistor elements are covered by a protective coating designed for electrical, mechanical and climatic protection. The terminations receive a final pure tin on nickel plating.

The result of the determined production is verified by an extensive testing procedure and optical inspection performed on 100 % of the individual chip resistors. Only accepted products are laid directly into the paper tape in accordance with **IEC 60286-3** [3].

ASSEMBLY

The resistors are suitable for processing on automatic SMD assembly systems. They are suitable for automatic soldering using reflow or vapour phase as shown in **IEC 61760-1** [3]. The encapsulation is resistant to all cleaning solvents commonly used in the electronics industry, including alcohols, esters and aqueous solutions. The suitability of conformal coatings, if applied, shall be qualified by appropriate means to ensure the long-term stability of the whole system. The resistors are RoHS compliant; the pure tin plating provides compatibility with lead (Pb)-free and lead-containing soldering processes. The permitted storage time is 20 years, whereas the solderability is specified for 2 years after production or requalification. The immunity of the plating against tin whisker growth has been proven under extensive testing.

All products comply with the **GADSL** [1] and the **CEFIC-EECA-EICTA** [2] list of legal restrictions on hazardous substances. This includes full compliance with the following directives:

- 2000/53/EC End of Vehicle life Directive (ELV) and Annex II (ELV II)
- 2011/65/EC Restriction of the use of Hazardous Substances directive (RoHS)
- 2002/96/EC Waste Electrical and Electronic Equipment Directive (WEEE)

TESTS

Where applicable, the resistors are tested in accordance with **EN 140401-801** which refers to **EN 60115-1** and **EN 140400**.

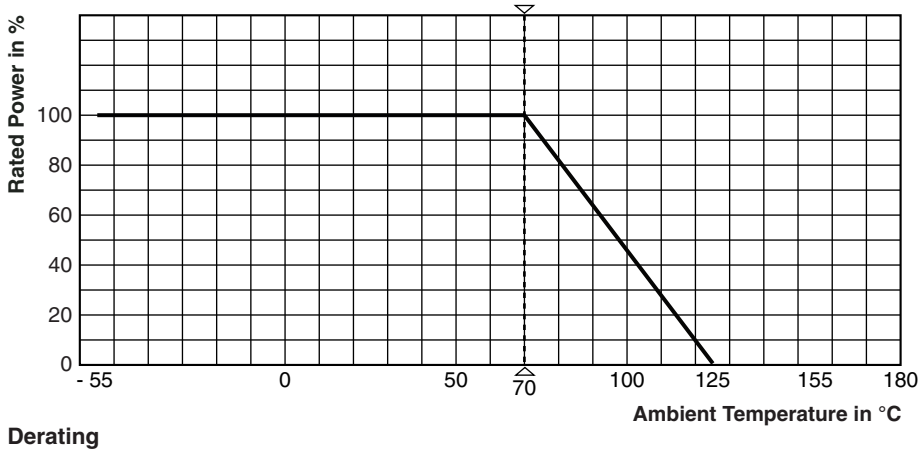
Notes

(1) Global Automotive Declarable Substance List, see www.gadsl.org.

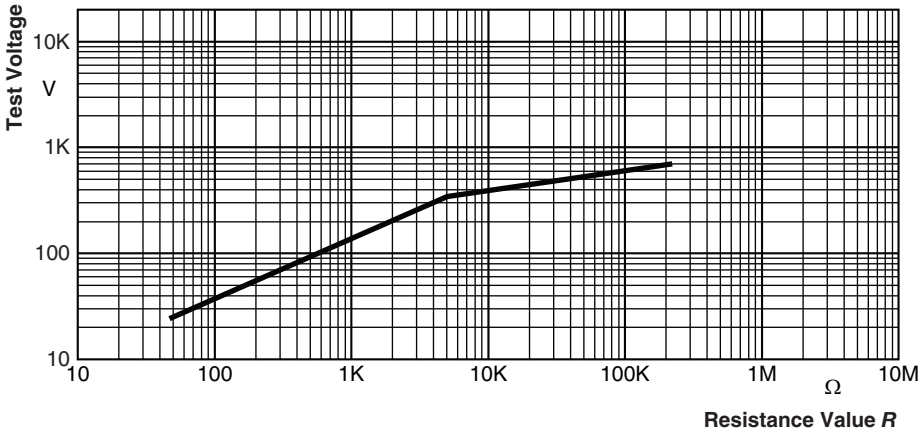
(2) CEFIC (European Chemical Industry Council), EECA (European Electronic Component Manufacturers Association), EICTA (European trade organisation representing the information and communications technology and consumer electronics), see www.eicta.org → policy → environmental policy group → chemicals → jig → Joint Industry Guide (JIG-101 Ed 2.0).

(3) The quoted IEC standards are also released as EN standards with the same number and identical contents.

FUNCTIONAL PERFORMANCE

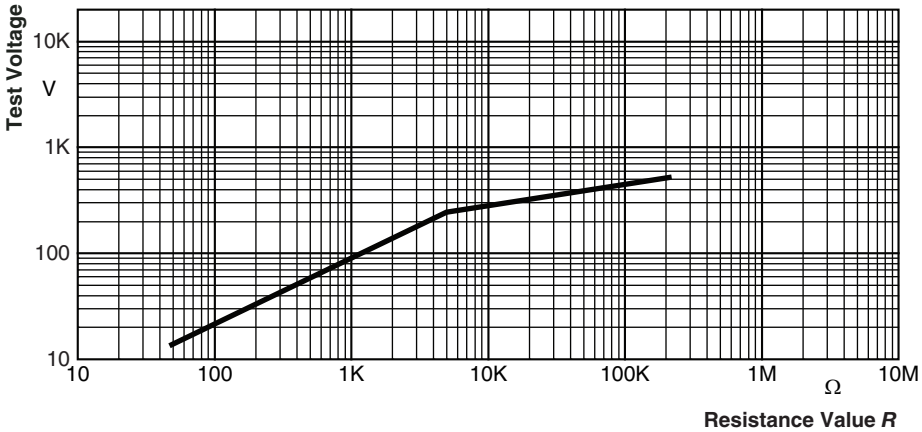


Derating



Pulse load rating for arrays with equal values, design type AE, in accordance with
EN 60115-1 clause 4.27; 1.2 µs/50 µs; 5 pulses at 12 s interval; for permissible resistance change (0.5 % R + 0.05 Ω)

1.2/50 Pulse



Pulse load rating rating for arrays with equal values, design type AE in accordance with
EN 60115-1 clause 4.27; 10 µs/700 µs; 10 pulses at 1 min intervals; for permissible resistance change (0.5 % R + 0.05 Ω)

10/700 Pulse

TESTS AND REQUIREMENTS

Essentially all tests are carried out in accordance with the following specifications:

EN 60115-1, generic specification

EN 140400, sectional specification

EN 140401-801, detail specification

The testing also covers most of the requirements specified by EIA/IS-703 and JIS-C-5202.

The tests are carried out in accordance with **IEC 60068** (1) and under standard atmospheric conditions according to **IEC 60068-1** (1), 5.3. Climatic category LCT/UCT/56 (rated temperature range: Lower category temperature, upper category temperature; damp heat, long term, 56 days) is valid (LCT = - 55 °C/UCT = 125 °C).

Unless otherwise specified the following values apply:

Temperature: 15 °C to 35 °C

Relative humidity: 45 % to 75 %

Air pressure: 86 kPa to 106 kPa (860 mbar to 1060 mbar)

The requirements stated in the "Test Procedures and Requirements" table are based on the required tests and permitted limits of EN 140401-801 where applicable.

TEST PROCEDURES AND REQUIREMENTS

EN 60115-1 CLAUSE	IEC 60068-2 (1) TEST METHOD	TEST	PROCEDURE	REQUIREMENTS PERMISSIBLE CHANGE (2) (ΔR)
			Stability for product types:	
			ACAS 0612	**47 Ω to 221 kΩ**
4.5	-	Resistance	-	± 1 %; ± 0.5 %
4.8.4.2	-	Temperature coefficient	At (20/- 55/20) °C and (20/125/20) °C	± 50 ppm/K; ± 25 ppm/K
4.25.1	-	Endurance	$U = \sqrt{P_{70} \times R}$ or $U = U_{max.}$; 1.5 h on; 0.5 h off; whichever is the less severe; 70 °C; 1000 h	± (0.25 % R + 0.05 Ω)
4.25.3	-	Endurance at upper category temperature	125 °C; 1000 h	± (0.25 % R + 0.05 Ω)
4.24	78 (Cab)	Damp heat, steady state	(40 ± 2) °C; 56 days; (93 ± 3) % RH	± (0.5 % R + 0.05 Ω)
4.13	-	Short time overload (3)	$U = 2.5 \times \sqrt{P_{70} \times R}$ or $U = 2 \times U_{max.}$; 5 s	± (0.1 % R + 0.01 Ω) no visible damage
4.19	14 (Na)	Rapid change of temperature	30 min at - 55 °C and 30 min at 125 °C; 5 cycles	± (0.1 % R + 0.01 Ω) no visible damage
4.18.2	58 (Td)	Resistance to soldering heat	Reflow method 2 (IR/forced gas convection); (260 ± 5) °C; (10 ± 1) s	± (0.25 % R + 0.01 Ω) no visible damage
4.17.2	58 (Td)	Solderability	Solder bath method; SnPb; non-activated flux accelerated ageing 4 h/155 °C (215 ± 3) °C; (3 ± 0.3) s	Good tinning (≥ 95 % covered); no visible damage
			Solder bath method; SnAgCu; non-activated flux accelerated ageing 4 h/155 °C (235 ± 3) °C; (2 ± 0.2) s	
4.32	21 (Ue_3)	Shear (adhesion)	45 N	No visible damage
4.33	21 (Ue_1)	Substrate bending	Depth 2 mm, 3 times	± (0.1 % R + 0.01 Ω) no visible damage; no open circuit in bent position
4.7	-	Voltage proof	$U_{RMS} = U_{ins}$ (60 ± 5) s; against ambient, between adjacent resistors	No flashover or breakdown

Notes

(1) The quoted IEC standards are also released as EN standards with the same number and identical contents.

(2) Figures are given for arrays with equal values, design type AE.

(3) For a single element.

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