Adjustable Frequency Current Mode Flyback/ Boost/SEPIC DC/DC Controller

FEATURES

- **V_{IN} and V_{OUT} Limited Only by External Components**
- **4.5V Undervoltage Lockout Threshold**
- **Adjustable Slope Compensation**
- **Adjustable Overcurrent Protection with Automatic Restart**
- **Adjustable Operating Frequency (70kHz to 700kHz) With One External Resistor**
- Synchronizable to an External Clock
- ±1.5% Reference Accuracy
- Only 100mV Current Sense Voltage Drop
- RUN Pin with Precision Threshold and Adjustable Hysteresis
- Programmable Soft-Start with One External Capacitor
- Low Quiescent Current: 360μA
- Small 10-Lead MSOP and 3mm × 3mm DFN

APPLICATIONS

- Automotive Power Supplies
- Telecom Power Supplies
- Isolated Electronic Equipment
- Auxiliary/Housekeeping Power Supplies
- Power over Ethernet

DESCRIPTION

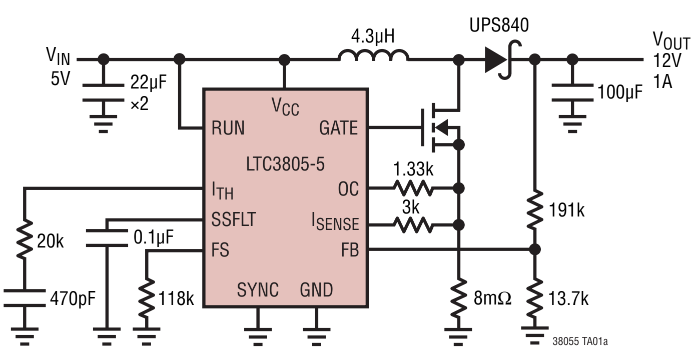
The LTC®3805-5 is a current mode DC/DC controller designed to drive an N-channel MOSFET in flyback, boost and SEPIC converter applications. Operating frequency and slope compensation can be programmed by external resistors. Programmable overcurrent sensing protects the converter from overload and short-circuit conditions. Soft-start can be programmed using an external capacitor and the soft-start capacitor also programs an automatic restart feature.

The LTC3805-5 provides ±1.5% output voltage accuracy and consumes only 360μA of quiescent current during normal operation and only 40μA during micropower start-up. Using a 9.5V internal shunt regulator, the LTC3805-5 can be powered from a high V_{IN} through a resistor or it can be powered directly from a low impedance DC voltage from 4.7V to 8.8V.

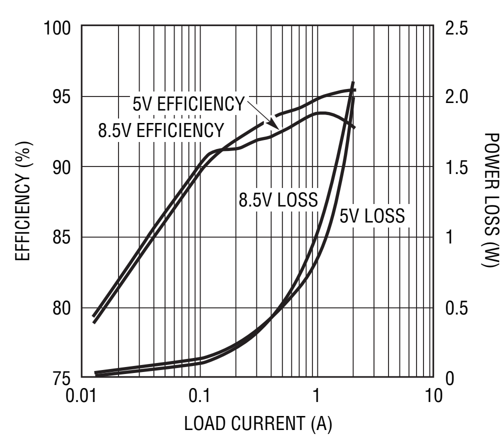
The LTC3805-5 is available in the 10-lead MSOP package and the 3mm × 3mm DFN package.

TYPICAL APPLICATION

5V to 12V/1A Boost Converter



Efficiency and Power Loss vs Load Current



ABSOLUTE MAXIMUM RATINGS (Note 1)

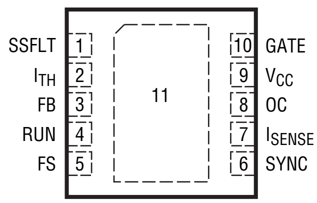
V_{CC} to GND
- Low Impedance Source .... –0.3V to 8.8V
- Current Fed .... 25mA into V_{CC}*

SYNC .... –0.3V to 6V
SSFLT.. –0.3V to 5V
FB, I_{TH}, FS... –0.3V to 3.5V
RUN .... –0.3V to 18V
OC, I_{SENSE} .... –0.3V to 1V
Operating Junction Temperature Range
(Notes 2, 3) .... –55°C to 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
- MSE Package .... 300°C

*LTC3805-5 internal clamp circuit regulates V_{CC} voltage to 9.5V

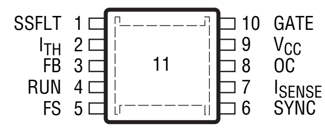
PIN CONFIGURATION

TOP VIEW



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 45°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE CONNECTED TO GND

TOP VIEW



MSE PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 45°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE CONNECTED TO GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3805EMSE-5#PBF	LTC3805EMSE-5#TRPBF	LTDGX	10-Lead Plastic MSOP	–40°C to 85°C
LTC3805IMSE-5#PBF	LTC3805IMSE-5#TRPBF	LTDGX	10-Lead Plastic MSOP	–40°C to 125°C
LTC3805HMSE-5#PBF	LTC3805HMSE-5#TRPBF	LTDGX	10-Lead Plastic MSOP	–40°C to 150°C
LTC3805MPMSE-5#PBF	LTC3805MPMSE-5#TRPBF	LTDGX	10-Lead Plastic MSOP	–55°C to 150°C
LTC3805EDD-5#PBF	LTC3805EDD-5#TRPBF	LDHB	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3805IDD-5#PBF	LTC3805IDD-5#TRPBF	LDHB	10-Lead (3mm × 3mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{CC} = 5V, unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{TURNON}	V_{CC} Turn-On Voltage	V_{CC} Rising	●	4.3	4.5	4.7	V
$V_{TURNOFF}$	V_{CC} Turn-Off Voltage	V_{CC} Falling	●	3.75	3.95	4.15	V
V_{HYST}	V_{CC} Hysteresis				0.55		V
$V_{CLAMP1mA}$	V_{CC} Shunt Regulator Voltage	I_{CC} = 1mA, V_{RUN} = 0	●	8.8	9.25	9.65	V
$V_{CLAMP25mA}$	V_{CC} Shunt Regulator Voltage	I_{CC} = 25mA, V_{RUN} = 0	●	8.9	9.5	9.9	V
I_{CC}	Input DC Supply Current	Normal Operation (f_{OSC} = 200kHz) (Note 4)			360		µA
		V_{RUN} < V_{RUNON} or V_{CC} < V_{TURNON} – 100mV (Micropower Start-Up)	●		40	90	µA
V_{RUNON}	RUN Turn-On Voltage	V_{CC} = V_{TURNON} + 100mV	●	1.122	1.207	1.292	V
V_{RUNOFF}	RUN Turn-Off Voltage	V_{CC} = V_{TURNON} + 100mV	●	1.092	1.170	1.248	V
$I_{RUN(HYST)}$	RUN Hysteresis Current		●	4	5	5.8	µA
V_{FB}	Regulated Feedback Voltage	0°C ≤ T_J ≤ 85°C (E-Grade) (Note 5)		0.788	0.800	0.812	V
		–40°C ≤ T_J ≤ 85°C (E-Grade) (Note 5)	●	0.780	0.800	0.812	V
		–40°C ≤ T_J ≤ 125°C (I-Grade) (Note 5)	●	0.780	0.800	0.812	V
		–40°C ≤ T_J ≤ 150°C (H-Grade) (Note 5)	●	0.770	0.800	0.820	V
		–55°C ≤ TJ ≤ 150°C (MP-Grade)	●	0.770	0.800	0.820	V
I_{FB}	V_{FB} Input Current	V_{ITH} = 1.3V (Note 5)			20		nA
g_m	Error Amplifier Transconductance	I_{TH} Pin Load = ±5µA (Note 5)			333		µA/V
$\Delta V_{O(LINE)}$	Output Voltage Line Regulation	$V_{TURNOFF}$ < V_{CC} < $V_{CLAMP1mA}$ (Note 5)			0.05		mV/V
$\Delta V_{O(LOAD)}$	Output Voltage Load Regulation	I_{TH} Sinking 5µA (Note 5)			3		mV/µA
		I_{TH} Sourcing 5µA (Note 5)			3		mV/µA
f_{OSC}	Oscillator Frequency	R_{FS} = 350k			70		kHz
		R_{FS} = 36k			700		kHz
$DC_{ON(MIN)}$	Minimum Switch-On Duty Cycle	f_{OSC} = 200kHz			6	9	%
$DC_{ON(MAX)}$	Maximum Switch-On Duty Cycle	f_{OSC} = 200kHz		70	80	95	%
f_{SYNC}	As a Function of f_{OSC}	70kHz < f_{OSC} < 700kHz, 70kHz < f_{SYNC} < 700kHz		67		133	%
V_{SYNC}	Minimum SYNC Amplitude					2.9	V
I_{SS}	Soft-Start Current				–6		µA
I_{FTO}	Fault Timeout Current				2		µA
$t_{SS(INT)}$	Internal Soft-Start Time	No External Capacitor on SSFLT			1.8		ms
$t_{FTO(INT)}$	Internal Fault Timeout	No External Capacitor on SSFLT			4.5		ms
t_{RISE}	Gate Drive Rise Time	C_{LOAD} = 3000pF			30		ns
t_{FALL}	Gate Drive Fall Time	C_{LOAD} = 3000pF			30		ns
$V_{I(MAX)}$	Peak Current Sense Voltage	R_{SL} = 0 (Note 6)	●	85	100	115	mV
$I_{SL(MAX)}$	Peak Slope Compensation Output Current	(Note 7)			10		µA
V_{OCT}	Overcurrent Threshold	R_{OC} = 0 (Note 8)	●	85	100	115	mV
I_{OC}	Overcurrent Threshold Adjust Current				10		µA

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3805-5 is tested under pulsed conditions such that $T_J \approx T_A$. The LTC3805E-5 is guaranteed to meet specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3805I-5 is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3805H-5 is guaranteed over the full –40°C to 150°C operating junction temperature range and the LTC3805MP-5 is tested and guaranteed over the full –55°C to 150°C operating temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$T_J = T_A + (P_D \bullet 45°C/W)$

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 5: The LTC3805-5 is tested in a feedback loop that servos V_{FB} to the output of the error amplifier while maintaining I_{TH} at the midpoint of the current limit range.

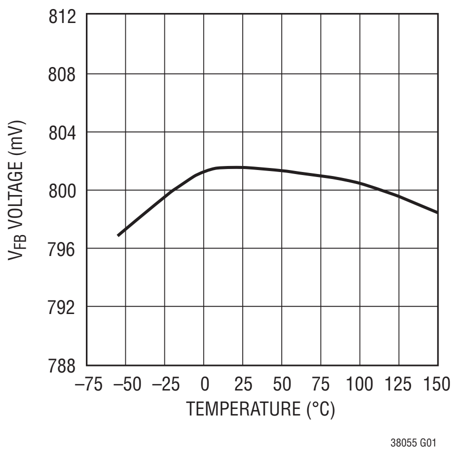
Note 6: Peak current sense voltage is reduced dependent on duty cycle and an optional external resistor in series with the SENSE pin. For details, refer to Programmable Slope Compensation in the Applications Information section.

Note 7: Guaranteed by design.

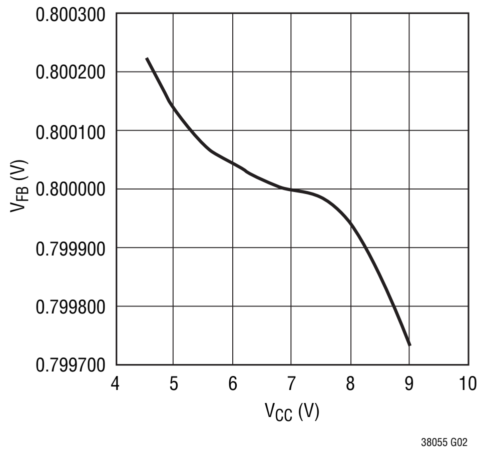
Note 8: Overcurrent threshold voltage is reduced dependent on an optional external resistor in series with the OC pin. For details, refer to Programmable Overcurrent in the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS

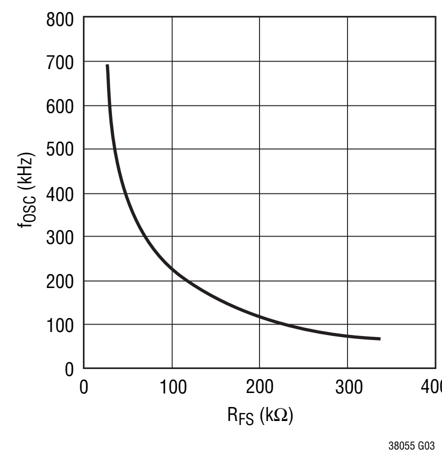
Reference Voltage vs Temperature



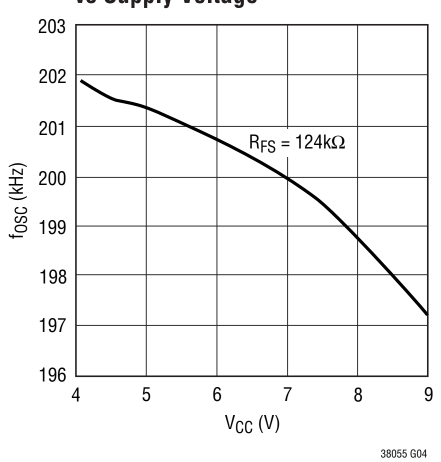
Reference Voltage vs Supply Voltage



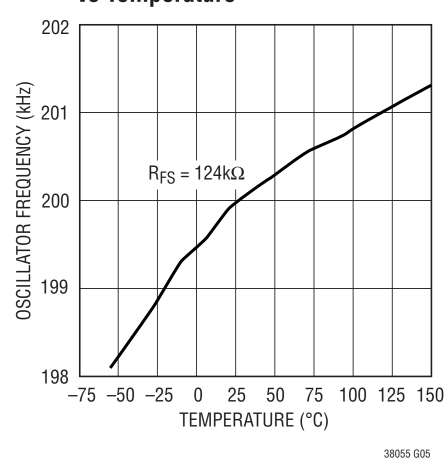
Oscillator Frequency vs R_{FS}



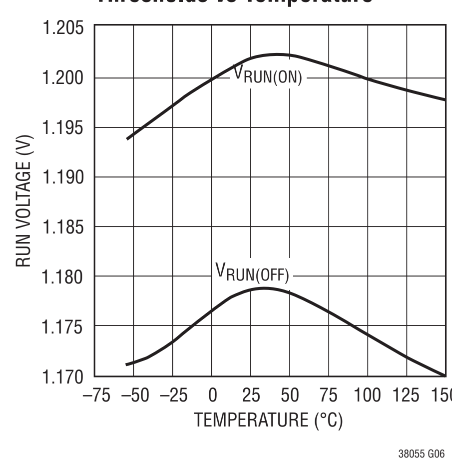
Oscillator Frequency vs Supply Voltage



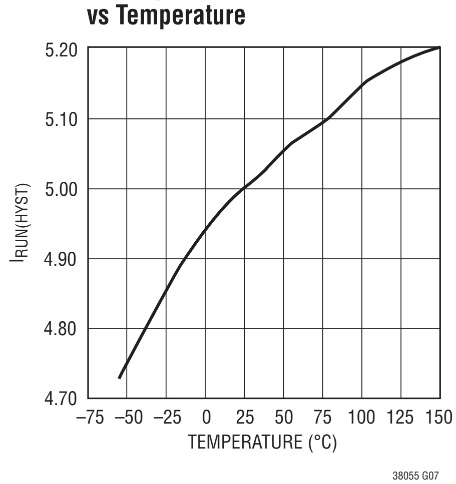
Oscillator Frequency vs Temperature



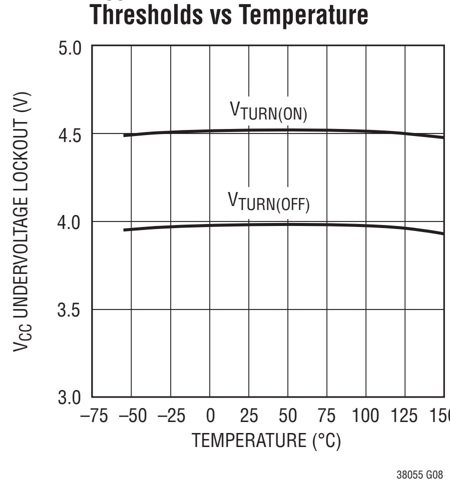
RUN Undervoltage Lockout Thresholds vs Temperature



RUN Hysteresis Current vs Temperature

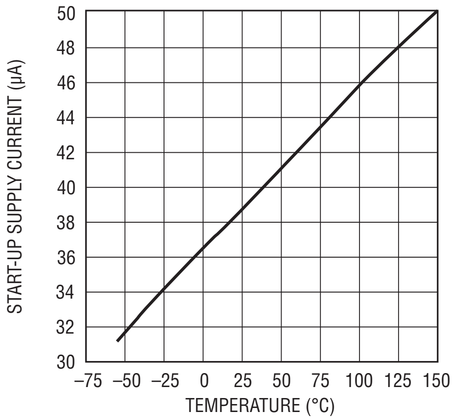


V_{CC} Undervoltage Lockout Thresholds vs Temperature

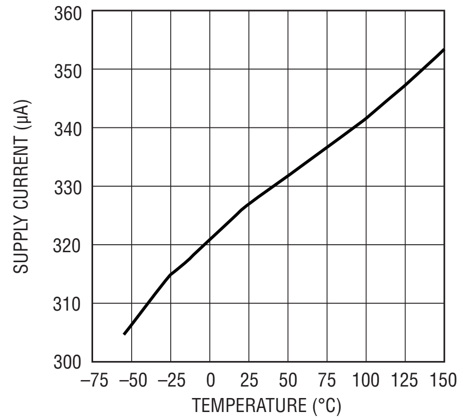


TYPICAL PERFORMANCE CHARACTERISTICS

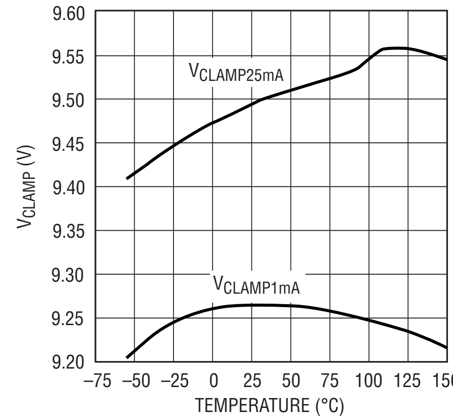
Start-Up I_{CC} Supply Current vs Temperature



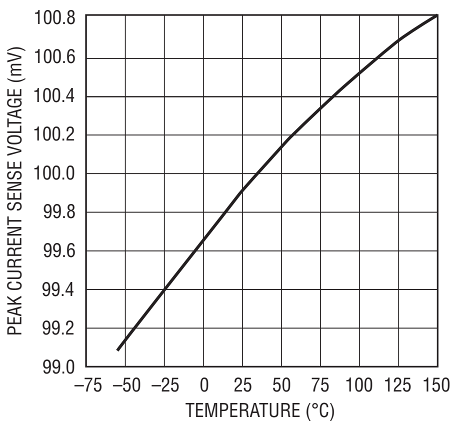
I_{CC} Supply Current vs Temperature



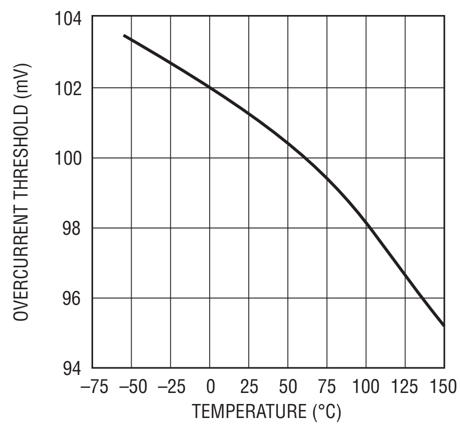
V_{CC} Shunt Regulator Voltage vs Temperature



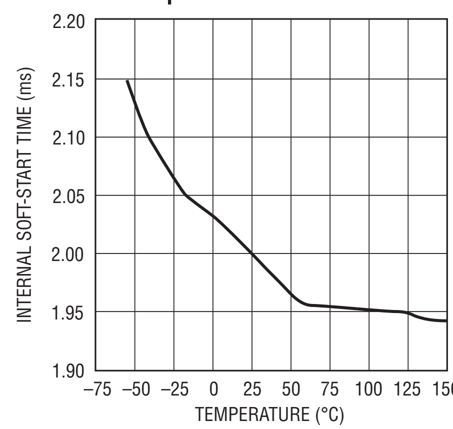
Peak Current Sense Voltage vs Temperature



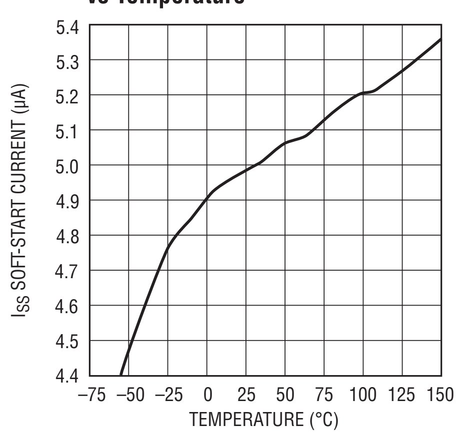
Overcurrent Threshold vs Temperature



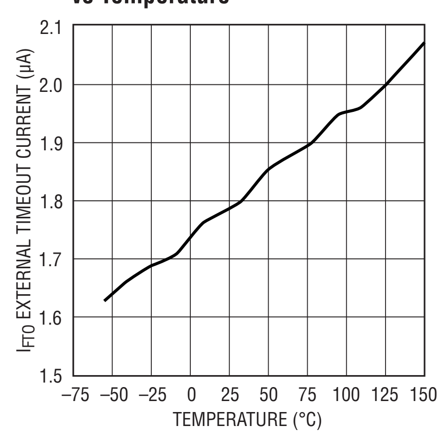
Internal Soft-Start Time vs Temperature



External Soft-Start Current vs Temperature



External Timeout Current vs Temperature



PIN FUNCTIONS

SSFLT (Pin 1): Soft-Start Pin. A capacitor placed from this pin to GND (Exposed Pad) controls the rate of rise of converter output voltage during start-up. This capacitor is also used for time out after a fault prior to restart.

I_{TH} (Pin 2): Error Amplifier Compensation Point. Normal operating voltage range is clamped between 0.7V and 1.9V.

FB (Pin 3): Receives the feedback voltage from an external resistor divider across the output.

RUN (Pin 4): An external resistor divider connects this pin to V_{IN} and sets the thresholds for converter operation.

FS (Pin 5): A resistor connected from this pin to ground sets the frequency of operation.

SYNC (Pin 6): Input to synchronize the oscillator to an external source.

I_{SENSE} (Pin 7): Performs two functions: for current mode control, it monitors the switch current, using the voltage across an external current sense resistor. Pin 7 also injects a current ramp that develops slope compensation voltage across an optional external programming resistor.

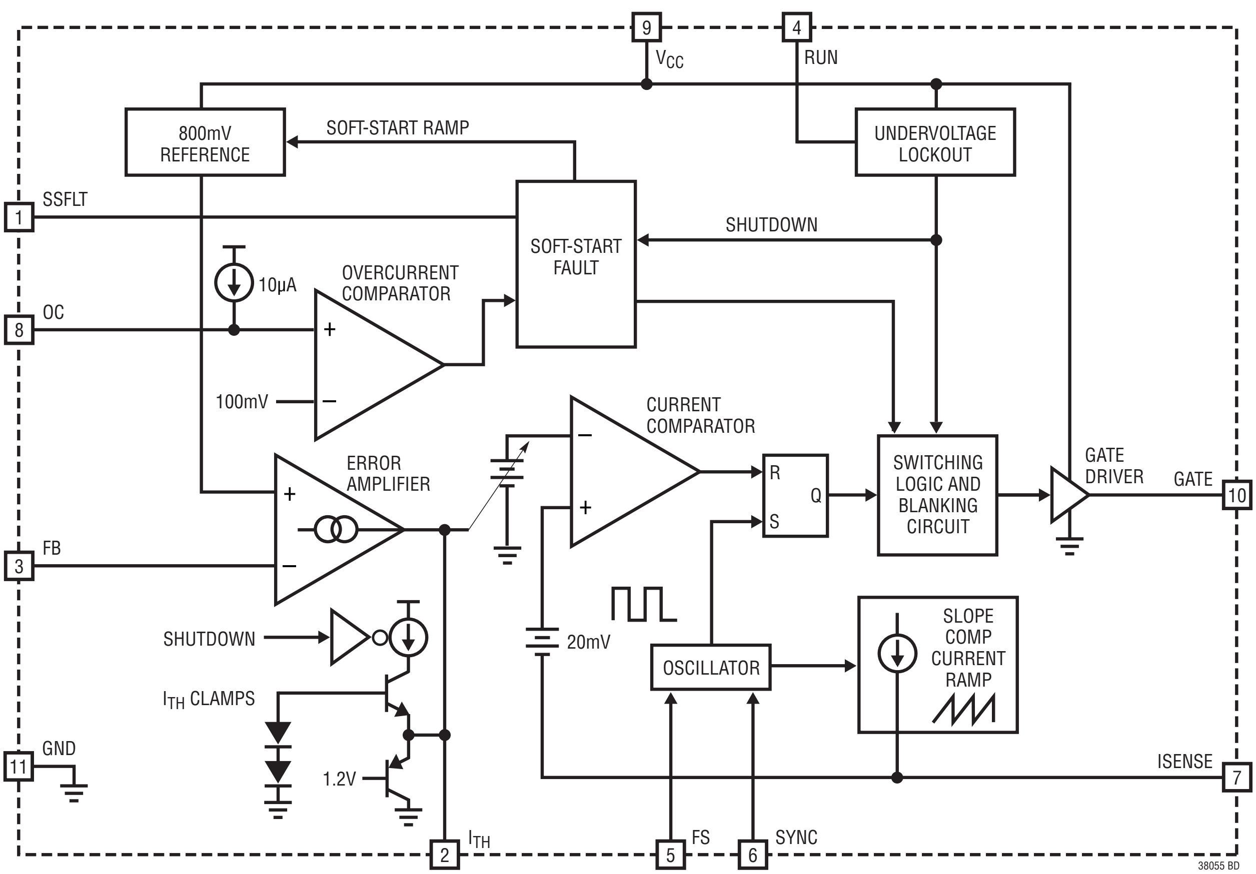
OC (Pin 8): Overcurrent Pin. Connect this pin to the external switch current sense resistor. An additional resistor programs the overcurrent trip level.

V_{CC} (Pin 9): Supply Pin. A capacitor must closely decouple V_{CC} to GND (Exposed Pad).

GATE (Pin 10): Gate Drive for the External N-Channel MOSFET. This pin swings from GND to V_{CC}.

GND (Exposed Pad Pin 11): Ground. A capacitor must closely decouple GND to V_{CC} (Pin 9). The exposed pad must be soldered to electrical ground on PCB for electrical contact and rated thermal performance.

BLOCK DIAGRAM



OPERATION

The LTC3805-5 is a programmable-frequency current mode controller for flyback, boost and SEPIC DC/DC converters. The LTC3805-5 is designed so that none of its pins need to come in contact with the input or output voltages of the power supply circuit of which it is a part, allowing the conversion of voltages well beyond the LTC3805-5's absolute maximum ratings.

Main Control Loop

Please refer to the Block Diagram of this data sheet and the Typical Application shown on the front page. An external resistive voltage divider presents a fraction of the output voltage to the FB pin. The divider is designed so that when the output is at the desired voltage, the FB pin voltage equals the 800mV internal reference voltage. If the load current increases, the output voltage decreases slightly, causing the FB pin voltage to fall below the 800mV reference. The error amplifier responds by feeding current into the I_{TH} pin causing its voltage to rise. Conversely, if the load current decreases, the FB voltage rises above the 800mV reference and the error amplifier sinks current away from the I_{TH} pin causing its voltage to fall.

The voltage at the I_{TH} pin controls the pulse-width modulator formed by the oscillator, current comparator and SR latch. Specifically, the voltage at the I_{TH} pin sets the current comparator's trip threshold. The current comparator's I_{SENSE} input monitors the voltage across an external current sense resistor in series with the source of the external MOSFET. At the start of a cycle, the LTC3805-5's oscillator sets the SR latch and turns on the external power MOSFET. The current through the external power MOSFET rises as does the voltage on the I_{SENSE} pin. The LTC3805-5's current comparator trips when the voltage on the I_{SENSE} pin exceeds a voltage proportional to the voltage on the I_{TH} pin. This resets the SR latch and turns off the external power MOSFET. In this way, the peak current levels through the external MOSFET and the flyback transformer's primary and secondary windings are controlled by the voltage on the I_{TH} pin. If the current comparator does not trip, the LTC3805-5 automatically limits the duty cycle to 80%, resets the SR latch, and turns off the external MOSFET.

The path from the FB pin, through the error amplifier, current comparator and the SR latch implements the closed-loop current mode control required to regulate the output voltage against changes in input voltage or output current. For example, if the load current increases, the output voltage decreases slightly, and sensing this, the error amplifier sources current from the I_{TH} pin, raising the current comparator threshold, thus increasing the peak currents through the transformer primary and secondary. This delivers more current to the load and restores the output voltage to the desired level.

The I_{TH} pin serves as the compensation point for the control loop. Typically, an external series RC network is connected from I_{TH} to ground and is chosen for optimal response to load and line transients. The impedance of this RC network converts the output current of the error amplifier to the I_{TH} voltage which sets the current comparator threshold and commands considerable influence over the dynamics of the voltage regulation loop.

OPERATION

Start-Up/Shutdown

The LTC3805-5 has two shutdown mechanisms to disable and enable operation: an undervoltage lockout on the V_{CC} supply pin voltage, and a precision-threshold RUN pin. The voltage on both pins must exceed the appropriate threshold before operation is enabled. The LTC3805-5 transitions into and out of shutdown according to the state diagram shown in Figure 1. Operation in fault timeout is discussed in a subsequent section. During shutdown the LTC3805-5 draws only a small 40μA current.

The undervoltage lockout (UVLO) mechanism prevents the LTC3805-5 from trying to drive the external MOSFET gate with insufficient voltage on the V_{CC} pin. The voltage at the V_{CC} pin must initially exceed V_{TURNON} = 4.5V to enable LTC3805-5 operation. After operation is enabled, the voltage on the V_{CC} pin may fall as low as $V_{TURNOFF}$ = 4V before undervoltage lockout disables the LTC3805-5. See the Applications Information section for more detail.

The RUN pin is connected to the input voltage using a voltage divider. Converter operation is enabled when the voltage on the RUN pin exceeds V_{RUNON} = 1.207V and disabled when the voltage falls below V_{RUNOFF} = 1.170V. Additional hysteresis is added by a 5μA current source acting on the voltage divider's Thevenin resistance. Setting the input voltage range and hysteresis is further discussed in the Applications Information section.

Setting the Oscillator Frequency

Connect a frequency set resistor R_{FS} from the FS pin to ground to set the oscillator frequency over a range from 70kHz to 700kHz. The oscillator frequency is calculated from:

$$f_{OSC} = \frac{24 \bullet 10^9}{R_{FS} - 1500}$$

The oscillator may be synchronized to an external clock using the SYNC input. The rising edge of the external clock on the SYNC pin triggers the beginning of a switching period, i.e., the GATE pin going high. The pulse width of the external clock is quite flexible.

Overcurrent Protection

With the OC pin connected to the external MOSFET's current sense resistor, the converter is protected in the event of an overload or short-circuit on the output. During normal operation the peak value of current in the external MOSFET, as measured by the current sense resistor (plus any adjustment for slope compensation), is set by the voltage on the I_{TH} pin operating through the current comparator. As the output current increases, so does the voltage on the I_{TH} pin and so does the peak MOSFET current.

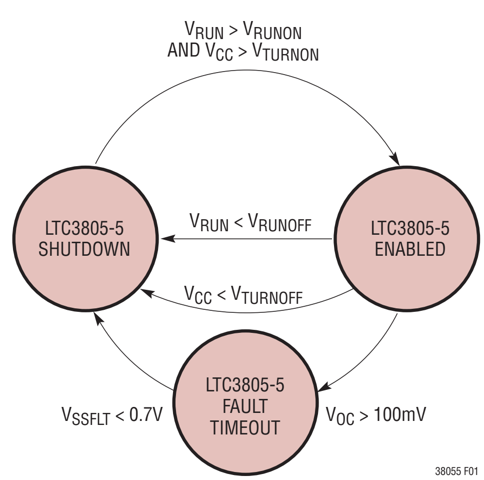


Figure 1. Start-Up/Shutdown State Diagram

OPERATION

First, consider operation without overcurrent protection. For some maximum converter output current, the voltage on the I_{TH} pin rises to and is clamped at approximately 1.9V. This corresponds to a 100mV limit on the voltage at the I_{SENSE} pin. As the output current is further increased, the duty cycle is reduced as the output voltage sags. However, the peak current in the external MOSFET is limited by the 100mV threshold at the I_{SENSE} pin.

As the output current is increased further, eventually, the duty cycle is reduced to the 6% minimum. Since the external MOSFET is always turned on for this minimum amount of time, the current comparator no longer limits the current through the external MOSFET based on the 100mV threshold. If the output current continues to increase, the current through the MOSFET could rise to a level that would damage the converter.

To prevent damage, the overcurrent pin, OC, is also connected to the current sense resistor, and a fault is triggered if the voltage on the OC pin exceeds 100mV. To protect itself, the converter stops operating as described in the next section. External resistors can be used to adjust the overcurrent threshold to voltages higher or lower than 100mV as described in the Applications Information section.

Soft-Start and Fault Timeout Operation

The soft-start and fault timeout of the LTC3805-5 uses either a fixed internal timer or an external timer programmed by a capacitor from the SSFLT pin to GND. The internal soft-start and fault timeout times are minimums and can be increased by placing a capacitor from the SSFLT pin to GND. Operation is shown in Figure 1.

Leave the SSFLT pin open to use the internal soft-start and fault timeout. The internal soft-start is complete in about 1.8ms. In the event of an overcurrent as detected by the OC pin exceeding 100mV, the LTC3805-5 shuts down and an internal timing circuit waits for a fault timeout of about 4.25ms and then restarts the converter.

Add a capacitor C_{SS} from the SSFLT pin to GND to increase both the soft-start time and the time for fault timeout. During soft-start, C_{SS} is charged with a 6µA current. When the LTC3805-5 comes out of shutdown, the LTC3805-5 quickly charges C_{SS} to about 0.7V at which point GATE begins switching. From that point, GATE continues switching with increasing duty cycle until the SSFLT pin reaches about 2.25V at which point soft-start is over and closed-loop regulation begins. The voltage on the SSFLT pin additionally further charges to about 4.75V.

C_{SS} also performs the timeout function in the event of a fault. After a fault, C_{SS} is slowly discharged from about 4.75V to about 0.7V by a 2µA current. When the voltage on the SSFLT pin reaches 0.7V the converter attempts to restart. More detail on programming the external soft-start fault timeout is described in the Applications Information section.

Powering the LTC3805-5

A built-in shunt regulator from the V_{CC} pin to GND limits the voltage on the V_{CC} pin to approximately 9.5V as long as the shunt regulator is not forced to sink more than 25mA. The shunt regulator is always active, even when the LTC3805-5 is in shutdown, since it serves the vital function of protecting the V_{CC} pin from overvoltage. The shunt regulator permits the use of a wide variety of powering schemes for the LTC3805-5 even from high voltage sources that exceed the LTC3805-5's absolute maximum ratings. Further details on powering schemes are described in the Applications Information section.

Adjustable Slope Compensation

The LTC3805-5 injects a 10µA peak current ramp out of its I_{SENSE} pin which can be used, in conjunction with an external resistor, for slope compensation in designs that require it. This current ramp is approximately linear and begins at zero current at 6% duty cycle, reaching peak current at 80% duty cycle. Additional details are provided in the Applications Information section.

Applications Information

Many LTC3805-5 application circuits can be derived from the topologies shown on the first page or in the Typical Applications section of this data sheet.

The LTC3805-5 itself imposes no limits on allowed input voltage V_{IN} or output voltage V_{OUT}. These are all determined by the ratings of the external power components. In Figure 8, the factors are: Q1 maximum drain-source voltage (B_{VDSS}), on-resistance ($R_{DS(ON)}$) and maximum drain current, T1 saturation flux level and winding insulation breakdown voltages, C_{IN} and C_{OUT} maximum working voltage, equivalent series resistance (ESR), and maximum ripple current ratings, and D1 and R_{SENSE} power ratings.

V_{CC} Bias Power

The V_{CC} pin must be bypassed to the GND pin with a minimum 1µF ceramic or tantalum capacitor located immediately adjacent to the two pins. Proper supply bypassing is necessary to supply the high transient currents required by the MOSFET gate driver.

For maximum flexibility, the LTC3805-5 is designed so that it can be operated from voltages well beyond the LTC3805-5's absolute maximum ratings. Figure 2 shows the simplest case, in which the LTC3805-5 is powered with a resistor R_{VCC} connected between the input voltage and V_{CC}. The built-in shunt regulator limits the voltage on the V_{CC} pin to around 9.5V as long as the internal shunt regulator is not forced to sink more than 25mA. This powering scheme has the drawback that the power loss in the resistor reduces converter efficiency and the 25mA shunt regulator maximum may limit the maximum-to-minimum range of input voltage.

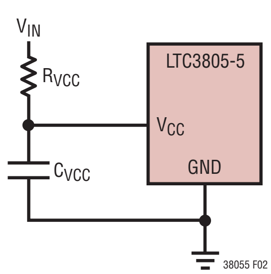


Figure 2. Powering the LTC3805-5 via the Internal Shunt Regulator

The typical application circuit in Figure 9 shows a different flyback converter bias power strategy for a case in which neither the input or output voltage is suitable for providing bias power to the LTC3805-5. A small NPN preregulator transistor and a Zener diode are used to accelerate the rise of V_{CC} and reduce the value of the V_{CC} bias capacitor. The flyback transformer has an additional bias winding to provide bias power. Note that this topology is very powerful because, by appropriate choice of transformer turns ratio, the output voltage can be chosen without regard to the value of the input voltage or the V_{CC} bias power for the LTC3805-5. The number of turns in the bias winding is chosen according to

$$N_{BIAS} = N_{SEC}\frac{V_{CC} + V_{D2}}{V_{OUT} + V_{D1}}$$

where N_{BIAS} is the number of turns in the bias winding, N_{SEC} is the number of turns in the secondary winding, V_{CC} is the desired voltage to power the LTC3805-5, V_{OUT} is the converter output voltage, V_{D1} is the forward voltage drop of D1 and V_{D2} is the forward voltage drop of D2. Note that since V_{OUT} is regulated by the converter control loop, V_{CC} is also regulated although not as precisely. If an "off-the-shelf" transformer with excessive bias windings is used, the resistor, R_{BIAS} in Figure 9, can be added to limit the current.

Transformer Design Considerations

Transformer specification and design is perhaps the most critical part of applying the LTC3805-5 successfully. In addition to the usual list of caveats dealing with high frequency power transformer design, the following should prove useful.

Turns Ratios

Due to the use of the external feedback resistor divider ratio to set output voltage, the user has relative freedom in selecting transformer turns ratio to suit a given application. Simple ratios of small integers, e.g., 1:1, 2:1, 3:2, etc. can be employed which yield more freedom in setting total turns and transformer inductance. Simple integer turns ratios also facilitate the use of "off-the-shelf" configurable transformers. Turns ratio can be chosen on

APPLICATIONS INFORMATION

the basis of desired duty cycle. However, remember that the input supply voltage plus the secondary-to-primary referred version of the flyback pulse (including leakage spike) must not exceed the allowed external MOSFET breakdown rating.

Leakage Inductance

Transformer leakage inductance (on either the primary or secondary) causes a voltage spike to occur after the turn off of MOSFET (Q1) in Figure 8. This is increasingly prominent at higher load currents, where more stored energy must be dissipated. In some cases an RC "snubber" circuit will be required to avoid overvoltage breakdown at the MOSFET's drain node. Application Note 19 is a good reference on snubber design. A bifilar or similar winding technique is a good way to minimize troublesome leakage inductances. However, remember that this will limit the primary-to-secondary breakdown voltage, so bifilar winding is not always practical.

Setting Undervoltage and Hysteresis on V_{IN}

The RUN pin is connected to a resistive voltage divider connected to V_{IN} as shown in Figure 3. The voltage threshold for the RUN pin is V_{RUNON} rising and V_{RUNOFF} falling. Note that $V_{RUNON} - V_{RUNOFF}$ = 35mV of built-in voltage hysteresis that helps eliminate false trips.

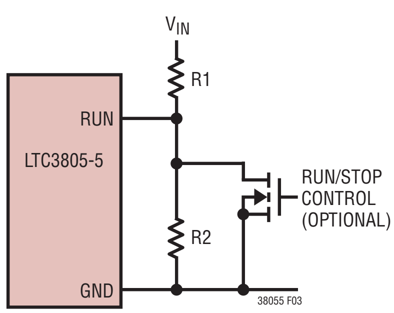


Figure 3. Setting RUN Pin Voltage and Run/Stop Control

To introduce further user-programmable hysteresis, the LTC3805-5 sources 5μA out of the RUN pin when operation of LTC3805-5 is enabled. As a result, the falling threshold for the RUN pin also depends on the value of R1 and can be programmed by the user. The falling threshold for V_{IN} is therefore

$$V_{IN(RUN,FALLING)} = V_{RUNOFF} \bullet \frac{R1+R2}{R2} - R1 \bullet 5\mu A$$

where R1(5μA) is the additional hysteresis introduced by the 5μA current sourced by the RUN pin. When in shutdown, the RUN pin does not source the 5μA current and the rising threshold for V_{IN} is simply

$$V_{IN(RUN,RISING)} = V_{RUNON} \bullet \frac{R1+R2}{R2}$$

Note that for some applications the RUN pin can be connected to V_{CC} in which case the V_{CC} thresholds, V_{TURNON} and $V_{TURNOFF}$, control operation.

External Run/Stop Control

To implement external run control, place a small N-channel MOSFET from the RUN pin to GND as shown in Figure 3. Drive the gate of this MOSFET high to pull the RUN pin to ground and prevent converter operation.

Selecting Feedback Resistor Divider Values

The regulated output voltage is determined by the resistor divider across V_{OUT} (R3 and R4 in Figure 8). The ratio of R4 to R3 needed to produce a desired V_{OUT} can be calculated:

$$R3 = \frac{V_{OUT} - 0.8V}{0.8V} R4$$

Choose resistance values for R3 and R4 to be as large as possible in order to minimize any efficiency loss due to the static current drawn from V_{OUT}, but just small enough so that when V_{OUT} is in regulation the input current to the V_{FB} pin is less than 1% of the current through R3 and R4. A good rule of thumb is to choose R4 to be less than 80k.

APPLICATIONS INFORMATION

Feedback in Isolated Applications

Isolated applications do not use the FB pin and error amplifier but control the I_{TH} pin directly using an opto-isolator driven on the other side of the isolation barrier as shown in Figure 4. For isolated converters, the FB pin is grounded which provides pull-up on the I_{TH} pin. This pull-up is not enough to properly bias the opto-isolator which is typically biased using a resistor to V_{CC}. Since the I_{TH} pin cannot sink the opto-isolator bias current, a diode is required to block it from the I_{TH} pin. A low leakage Schottky diode, or low forward voltage PN junction diode, should be used to ensure that the opto-isolator is able to pull I_{TH} down to its lower clamp.

Oscillator Synchronization

The oscillator may be synchronized to an external clock by connecting the synchronization signal to the SYNC pin. The LTC3805-5 oscillator and turn-on of the switch are synchronized to the rising edge of the external clock. The frequency of the external sync signal must be ±33% with respect to f_{OSC} (as programmed by R_{FS}). Additionally, the value of f_{SYNC} must be between 70kHz and 700kHz.

Current Sense Resistor Considerations

The external current sense resistor (R_{SENSE} in Figure 8) allows the user to optimize the current limit behavior for the particular application. As the current sense resistor is varied from several ohms down to tens of milliohms, peak switch current goes from a fraction of an ampere to several amperes. Care must be taken to ensure proper circuit operation, especially with small current sense resistor values.

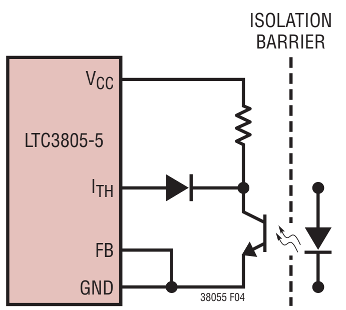


Figure 4. Circuit for Isolated Feedback

For example, with the peak current sense voltage of 100mV on the I_{SENSE} pin, a peak switch current of 5A requires a sense resistor of 0.020Ω. Note that the instantaneous peak power in the sense resistor is 0.5W and it must be rated accordingly. The LTC3805-5 has only a single sense line to this resistor. Therefore, any parasitic resistance in the ground side connection of the sense resistor will increase its apparent value. In the case of a 0.020Ω sense resistor, one milliohm of parasitic resistance will cause a 5% reduction in peak switch current. So the resistance of printed circuit copper traces and vias cannot necessarily be ignored.

Programmable Slope Compensation

The LTC3805-5 injects a ramping current through its I_{SENSE} pin into an external slope compensation resistor R_{SLOPE}. This current ramp starts at zero right after the GATE pin has been high for the LTC3805-5's minimum duty cycle of 6%. The current rises linearly towards a peak of 10µA at the maximum duty cycle of 80%, shutting off once the GATE pin goes low. A series resistor R_{SLOPE} connecting the I_{SENSE} pin to the current sense resistor R_{SENSE} develops a ramping voltage drop. From the perspective of the I_{SENSE} pin, this ramping voltage adds to the voltage across the sense resistor, effectively reducing the current comparator threshold in proportion to duty cycle. This stabilizes the control loop against subharmonic oscillation. The amount of reduction in the current comparator threshold (ΔV_{SENSE}) can be calculated using the following equation:

$$\Delta V_{SENSE} = \frac{\text{Duty Cycle} - 6\%}{80\%} 10\mu A \bullet R_{SLOPE}$$

Note: LTC3805-5 enforces 6% < Duty Cycle < 80%. A good starting value for R_{SLOPE} is 3k, which gives a 30mV drop in current comparator threshold at 80% duty cycle. Designs that do not operate at greater than 50% duty cycle do not need slope compensation and may replace R_{SLOPE} with a direct connection.

APPLICATIONS INFORMATION

Overcurrent Threshold Adjustment

Figure 5 shows the connection of the overcurrent pin, OC, along with the I_{SENSE} pin and the current sense resistor R_{SENSE} located in the source circuit of the power NMOS which is driven by the GATE pin. The internal overcurrent threshold on the OC pin is set at V_{OCT} = 100 mV which is the same as the peak current sense voltage $V_{I(MAX)}$ = 100 mV on the I_{SENSE} pin. The role of the slope compensation adjustment resistor R_{SLOPE} and the slope compensation current I_{SLOPE} is discussed in the prior section. In combination with the overcurrent threshold adjust current I_{OC} = 10µA, an external resistor R_{OC} can be used to lower the overcurrent trip threshold from 100mV. This section describes how to pick R_{OC} to achieve the desired performance. In the discussion that follows be careful to distinguish between "current limit" where the converter continues to run with the I_{SENSE} pin limiting current on a cycle-by-cycle basis while the output voltage falls below the regulation point and "overcurrent protection" where the OC pin senses an overcurrent and shuts down the converter for a timeout period before attempting an automatic restart.

One overcurrent protection strategy is for the converter to never enter current limit but to maintain output voltage regulation up to the point of tripping the overcurrent protection. Operation at minimum input voltage $V_{IN(MIN)}$ hits current limiting for the smallest output current and is the design point for this strategy.

First, for operation at $V_{IN(MIN)}$, calculate the duty cycle Duty Cycle $V_{IN(MIN)}$ using the appropriate formula depending on whether the converter is a boost, flyback or SEPIC. Then use Duty Cycle $V_{IN(MIN)}$ to calculate $\Delta V_{SENSE(VIN(MIN))}$ using the formula in the prior section. For overcurrent protection to trip at exactly the point where current limiting would begin set:

$$R_{OC(CRIT)} = \frac{\Delta V_{SENSE(VIN(MIN))}}{10\mu A}$$

To find the actual output current that trips overcurrent protection, calculate the peak switch current $I_{PK(VIN(MIN))}$ from:

$$I_{PK(VIN(MIN))} = \frac{100mV - \Delta V_{SENSE(VIN(MIN))}}{R_{SENSE}}$$

Then calculate the converter output current that corresponds to $I_{PK(VIN(MIN))}$. Again, the calculation depends both on converter type and the details of converter design including inductor current ripple. For minimum input voltage, $R_{OC(CRIT)}$ produces an overcurrent trip at an output current just before loss of output voltage regulation and the onset of current limiting. Note that the output current that causes an overcurrent trip is higher for higher input voltages but that an overcurrent trip will always occur before loss of output voltage regulation. If desired to meet a specific design target, an increase in R_{OC} above $R_{OC(CRIT)}$ can be used to reduce the trip threshold and make the converter trip for a lower output current.

This calculation is based on steady-state operation. Depending on design, overcurrent protection can also be triggered during a start-up transient, particularly if large output filter capacitors are being charged as output voltage rises. If that is a problem, output capacitor charging can be slowed by using a larger value of SSFLT capacitor. It is also possible to trip overcurrent protection during a load step especially if the trip threshold is lowered by making $R_{OC} > R_{OC(CRIT)}$.

Another overcurrent protection strategy is keep the converter running as current limiting reduces the duty cycle and the output voltage sags. In this case, the goal is often keep the converter in normal operation over as wide a range as possible, including current limiting, and to trigger the

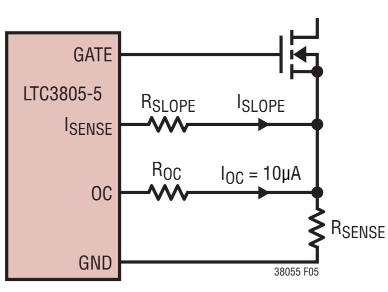


Figure 5. Circuit to Decrease Overcurrent Threshold

APPLICATIONS INFORMATION

overcurrent trip only to prevent damage. To implement this strategy use a value of R_{OC} smaller than $R_{OC(CRIT)}$. This also reduces sensitivity to overcurrent trips caused by transient operation. In the limit, set R_{OC} = 0 and connect the OC pin directly to R_{SENSE}. This causes an overcurrent trip near minimum duty cycle or around 6%.

In some cases it may be desirable to increase the trip threshold even further. In this strategy, the converter is allowed to operate all the way down to minimum duty cycle at which point the cycle-by-cycle current limit of the I_{SENSE} pin is lost and switch current goes up proportionally to the output current. Figures 6 and 7 show two ways to do this. Figure 6 is for relatively low currents with relatively large values of R_{SENSE}. Using this circuit the overcurrent trip threshold is increased from 100mV to:

$$V_{OC} = \frac{R_{SENSE1} + R_{SENSE2}}{R_{SENSE1}} 100mV$$

where it is assumed that the values of R_{SENSE1} and R_{SENSE2} are so small that the I_{OC} = 10µA threshold adjustment current produces a negligible change in V_{OC}.

For larger currents, values of the current sense resistors must be very small and the circuit of Figure 6 becomes impractical. The circuit of Figure 7 can be substituted and the current sense threshold is increased from 100mV to:

$$V_{OC} = \frac{R1 + R2}{R1} 100mV$$

where the values of R1 and R2 should be kept below 10Ω to prevent the I_{OC} = 10µA threshold adjustment current from producing a shift in V_{OC}.

External Soft-Start Fault Timeout

The external soft-start is programmed by a capacitor C_{SS} from the SSFLT pin to GND. At the initiation of soft-start the voltage on the SSFLT pin is quickly charged to 0.7V at which point GATE begins switching. From that point, a 6µA current charges the voltage on the SSFLT pin until the voltage reaches about 2.25V at which point soft-start is over and the converter enters closed-loop regulation. The soft-start time $t_{SS(EXT)}$ as a function of the soft-start capacitor C_{SS} is therefore:

$$t_{SS(EXT)} = C_{SS} \frac{2.25 - 0.7V}{6\mu A}$$

After soft-start is complete, the voltage on the SSFLT pin continues to charge to about a final value of 4.75V. Note that choosing a value of C_{SS} less than 5.8nF has no effect since it would attempt to program an external soft-start time $t_{SS(EXT)}$ less than the mandatory minimum internal soft-start time $t_{SS(IN)}$ = 1.8ms.

If there is an overcurrent fault detected on the OC pin, the LTC3805-5 enters a shutdown mode while a 2µA current discharges the voltage on the SSFLT pin from 4.75V to about 0.7V. The fault timeout $t_{FTO(EXT)}$ is therefore:

$$t_{FTO(EXT)} = C_{SS} \frac{4.75V - 0.7V}{2\mu A}$$

At this point, the LTC3805-5 attempts a restart.

In the event of a persistent fault, such as a short-circuit on the converter output, the converter enters a "hiccup" mode where it continues to try and restart at repetition rate determined by C_{SS}. If the fault is eventually removed the converter successfully restarts.

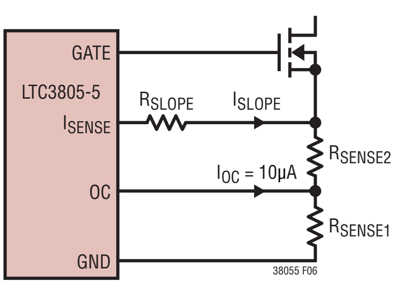


Figure 6. Circuit to Increase the Overcurrent Threshold for Small Switch Currents

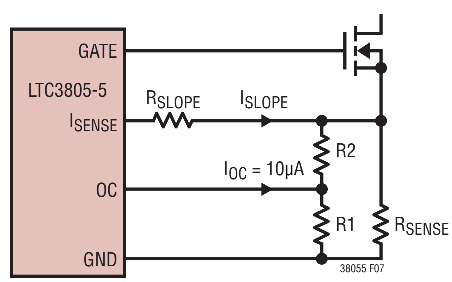


Figure 7. Circuit to Increase the Overcurrent Threshold for Large Switch Currents

TYPICAL APPLICATIONS

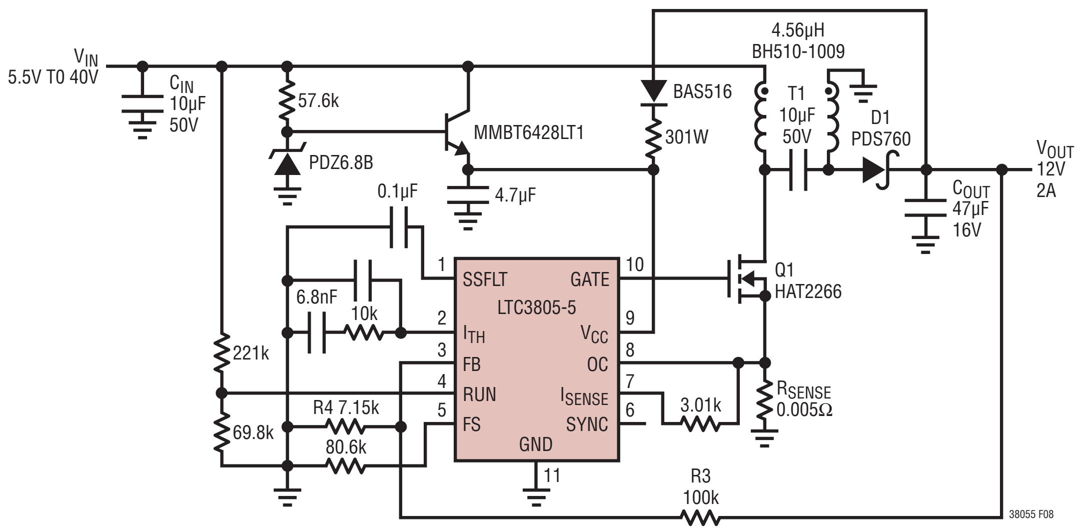
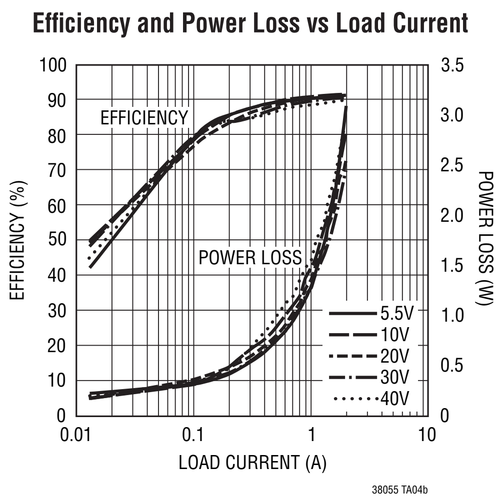


Figure 8. 5.5V to 40V to 12V/2A SEPIC Converter



TYPICAL APPLICATIONS

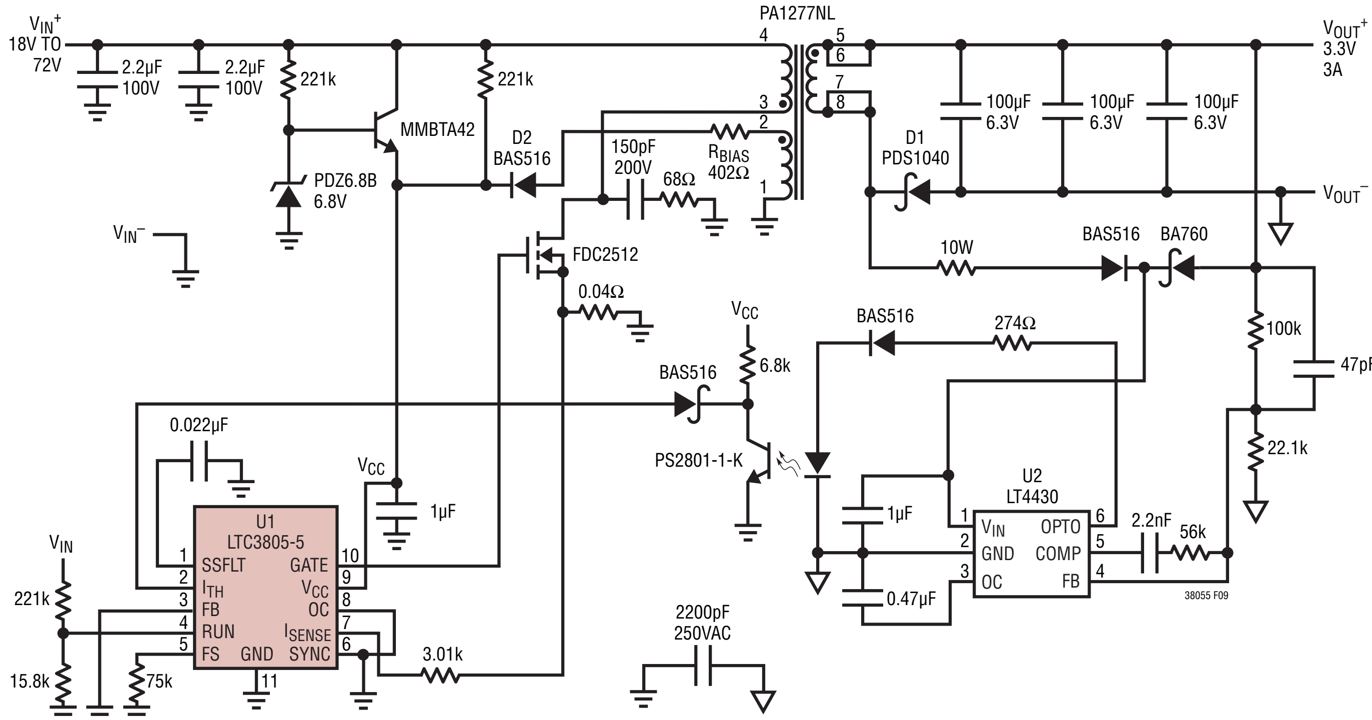
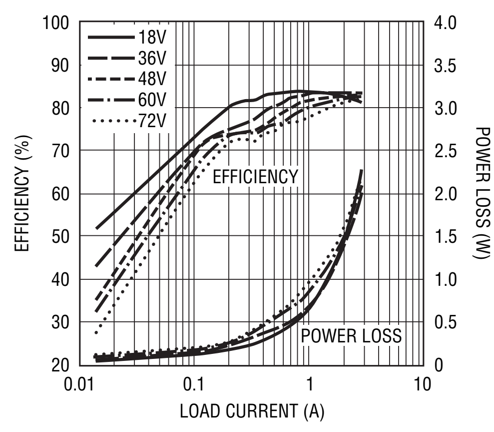


Figure 9. Isolated Telecom Supply: 18V to 72V Input to 3.3V/3A Output

Efficiency and Power Loss vs Load Current and V_{IN}



PACKAGE DESCRIPTION

DD Package
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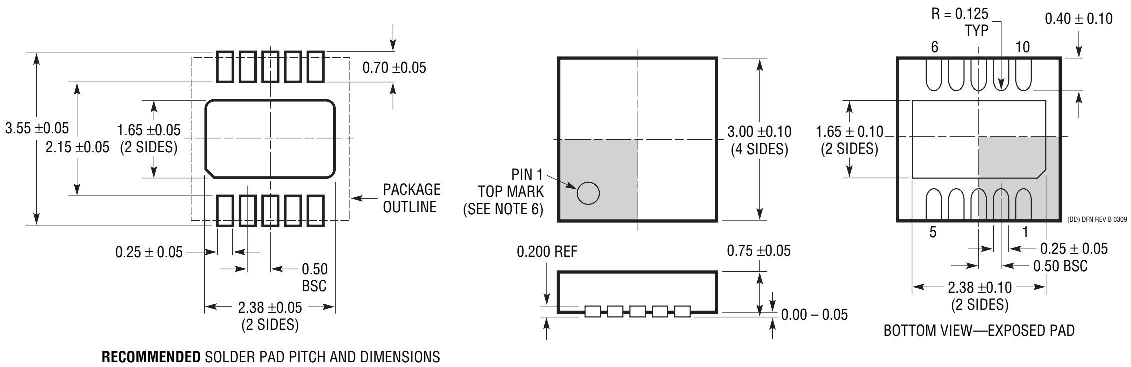
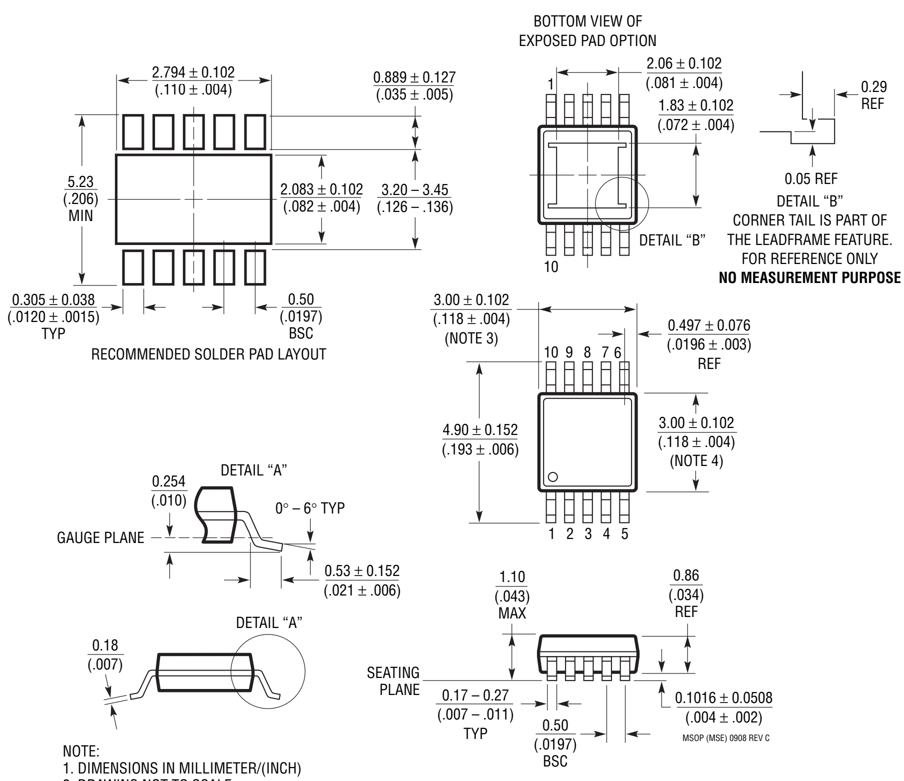
(Reference LTC DWG # 05-08-1699 Rev B)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

MSE Package
10-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1664 Rev C)



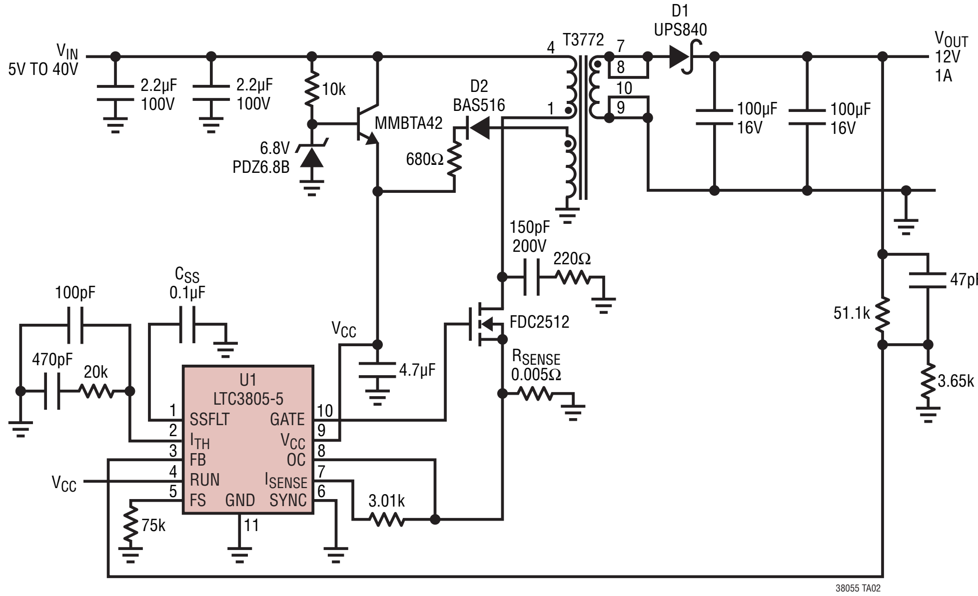
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY (Revision history begins at Rev D)

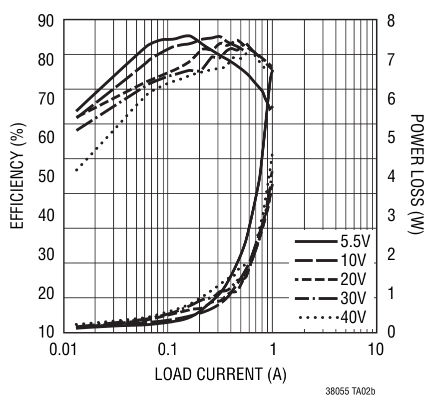
REV	DATE	DESCRIPTION	PAGE NUMBER
D	04/10	Updates to Absolute Maximum Ratings	2
		Changes to Electrical Characteristics Table	3
		Updates to Note 2	4
		Update to Pin 11 in Pin Functions	7
		Edits to Start-Up Shutdown in Operation Section	9
		Change to Typical Application	17, 20
		Updated Related Parts Table	20
E	05/11	Added MP-grade part. Reflected throughout the data sheet	1-20

TYPICAL APPLICATION

5V to 40V to 12V/1A Nonisolated Flyback Converter



Efficiency and Power Loss vs Load Current



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3748	100V No Opto Flyback Controller	$5V \le V_{IN} \le 100V$, Boundary Mode Operation, MSOP-16 with Extra High Voltage Pin Spacing
LT3758	Boost, Flyback, SEPIC and Inverting Controller	$5.5V \le V_{IN} \le 100V$, 100kHz to 1MHz Programmable Operating Frequency, 3mm × 3mm DFN-10 and MSOP-10E
LT3575	No Opto-Isolated Flyback with 60V Integrated Switch	$3V \le V_{IN} \le 40V$, Up to 14W, Boundary Mode Operation, TSSOP-16E
LTC3803/LTC3803-3/ LTC3803-5	Flyback DC/DC Controller with Fixed 200kHz or 300kHz Operating Frequency	V_{IN} and V_{OUT} Limited Only by External Components, 6-Pin ThinSOT™ Package
LTC3873/LTC3873-5	No R_{SENSE}™ Constant Frequency Flyback, Boost, SEPIC Controller	V_{IN} and V_{OUT} Limited Only by External Components, 8-Pin ThinSOT or 2mm × 3mm DFN-8 Packages
LT3825	No Opto-Isolated Synchronous Flyback Controller	V_{IN} 16V to 75V Limited by External Components, Up to 60W, TSSOP-16E

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