Keywords: DS4404, DS4402, power supply, power supplies, margining, power supply margining, power supply tolerance, tolerance, feedback, resistive, divider, vfb, feedback node, vref, reference voltage, DC/DC, DC-DC, converter, current, source, sink

APPLICATION NOTE 4149

How to Add Margining Capability to a DC-DC Converter

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Abstract: This application note explains how easy it is to add margining capability to a DC-DC converter by connecting it to a DS4404 4-channel adjustable current DAC (or the DS4402, 2-channel version).

This application note shows how to connect the DS4404, a 4-channel adjustable current DAC (or the DS4402, a 2-channel version of the DS4404), to a DC-DC converter circuit to add margining capability.

The circuit in **Figure 1** illustrates how simple it is to integrate the DS4404 into an existing design. The DS4404 is added to the feedback node (see the dashed line) so that the V_{OUT} of the DC-DC converter can be adjusted. On power up, the DS4404 outputs a current of 0A (appears as high impedance), essentially making the DS4404 transparent until it is written to through I²C.

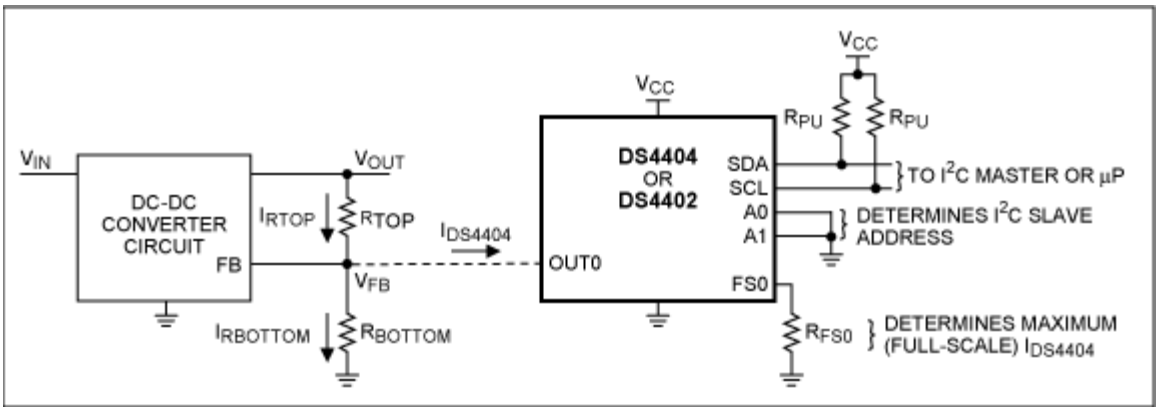

Figure 1. Connecting a DS4404 to a DC-DC converter feedback circuit.

Assume the following for our example (which are independent of the DS4404):

V_{IN} = 3V to 5.5V
V_{OUT} = 1.8V (desired nominal output voltage)
V_{FB} = 0.6V (not to be confused with V_{REF} of the DS4404)

The value of V_{FB} is found in the DC-DC converter's data sheet. It is important to verify that this voltage is within the OUTx voltage range specified in the DS4404's data sheet ($V_{OUT:SINK}$ and $V_{OUT:SOURCE}$). Finally, it is also important to check the input impedance of the DC-DC converter's FB pin; the example here assumes that it is high impedance.

Assume that we are using the DS4404 to add ±20% margining of V_{OUT}. Therefore, we have:

V_{OUTMAX} = 2.16V
V_{OUTNOM} = 1.8V
V_{OUTMIN} = 1.44V

Begin by determining the necessary relationship between R_{TOP} and R_{BOTTOM} which yield nominal V_{OUT}, V_{OUTNOM}, when I_{DS4404} = 0A.

$$V_{FB} = V_{OUTNOM}\left(\frac{R_{BOTTOM}}{R_{BOTTOM} + R_{TOP}}\right)$$

Solving for R_{TOP}, we get:

$$R_{TOP} = R_{BOTTOM}\left(\frac{V_{OUTNOM}}{V_{FB}} - 1\right) \qquad \text{Eq. 1}$$

So for our example:

$$R_{TOP} = R_{BOTTOM}\left(\frac{1.8V}{0.6V} - 1\right) = 2 \times R_{BOTTOM}$$

The current required to make V_{OUT} increase to V_{OUTMAX}, I_{DS4404}, is derived by summing the currents at the FB node.

$$I_{RTOP} = I_{RBOTTOM} + I_{DS4404}$$
$$I_{DS4404} = I_{RTOP} - I_{RBOTTOM} \qquad \text{Eq. 2}$$
$$I_{RTOP} = \left(\frac{V_{OUTMAX} - V_{FB}}{R_{TOP}}\right), \quad I_{RBOTTOM} = \left(\frac{V_{FB}}{R_{BOTTOM}}\right)$$
$$I_{DS4404} = \left(\frac{V_{OUTMAX} - V_{FB}}{R_{TOP}}\right) - \left(\frac{V_{FB}}{R_{BOTTOM}}\right)$$

This equation can be simplified by solving Equation 1 for R_{BOTTOM} and then substituting.

$$I_{DS4404} = \frac{V_{OUTMAX} - V_{OUTNOM}}{R_{TOP}}$$

Or in terms of margin percentage:

$$I_{DS4404} = \frac{V_{OUTNOM} \times margin}{R_{TOP}} \qquad \text{Eq. 3}$$

where margin = 0.2 for this example of ±20% margining.

However, before we can use this relationship to calculate R_{TOP} and R_{BOTTOM}, the full-scale current, I_{FS}, must be selected.

According to the DS4404's data sheet, the full-scale current needs to be between 0.5mA and 2.0mA (specified as $I_{OUT:SINK}$ and $I_{OUT:SOURCE}$ in the DS4404 data sheet, depending on whether sinking or sourcing current) to assure the accuracy and linearity specifications. Unfortunately, there is no one formula to calculate the ideal full-scale current. Every application will be different. Some items that influence the selection of the full-scale current are the desired number of steps, step size, as well as R_{TOP} and R_{BOTTOM} values. Likewise, there may be times when you want a particular register setting to correspond to a particular margin percentage. Either way, selecting the ideal full-scale current for your application will usually take several iterations of arbitrarily selecting a full-scale current (within the range) and then calculating R_{TOP}, R_{BOTTOM}, R_{FS}, and step size. Then, once a full-scale current is determined, you can choose to adjust it or some of the resistor values in order to end up with common resistor values.

Returning to the original example, to calculate R_{TOP} we will make $I_{FS} = I_{DS4404}$. This will give us 31 steps from V_{OUTNOM} to V_{OUTMAX} and 31 steps from V_{OUTNOM} to V_{OUTMIN}, which is more than adequate for our example.

Alternatively, we could begin by arbitrarily choosing I_{FS} to be in the center (1.25mA) of the specified range, and then perform all the calculations. Instead, for illustrative purposes we will perform the calculations for the endpoints of the range.

So for $I_{FS} = I_{DS4404}$ = 0.5mA.

Using Eq. 3 and solving for R_{TOP}:

$$R_{TOP} = \frac{V_{OUTNOM} \times margin}{I_{DS4404}} = \frac{1.8 \times 0.2}{0.5 \times 10^{-3}} = 720\Omega$$

$$R_{BOTTOM} = \frac{R_{TOP}}{2} = \frac{720}{2} = 360\Omega$$

Then R_{FS} is calculated using the formula given in the DS4404 data sheet along with V_{REF}, also found in the DS4404 data sheet:

$$R_{FS} = \frac{V_{REF}}{I_{FS}} \times \frac{31}{4} = \frac{1.23}{0.5 \times 10^{-3}} \times \frac{31}{4} = 19{,}065\Omega \approx 19k\Omega$$

$$\text{step size} = \frac{I_{FS}}{\text{number of steps}} = \frac{0.5 \times 10^{-3}}{31} = 16.1\mu A/\text{step}$$

Finally, for completeness we can determine the DS4404 output current as a function of register setting:

$$I_{OUT}(\text{register setting}) = \text{step size} \times \text{register setting}$$

Note: the register setting here does not include the sign bit, which is used to select sink or source. The DS4404 sinks current when the sign bit = 0, thus making V_{OUT} increase to V_{OUTMAX}. The DS4404 sources current when the sign bit = 1, thus decreasing V_{OUT} towards V_{OUTMIN}.

Likewise for $I_{FS} = I_{DS4404}$ = 2.0mA:

$$R_{TOP} = \frac{V_{OUTNOM} \times margin}{I_{DS4404}} = \frac{1.8 \times 0.2}{2.0 \times 10^{-3}} = 180\Omega$$

$$R_{BOTTOM} = \frac{R_{TOP}}{2} = \frac{180}{2} = 90\Omega$$

$$R_{FS} = \frac{V_{REF}}{I_{FS}} \times \frac{31}{4} = \frac{1.23}{2.0 \times 10^{-3}} \times \frac{31}{4} = 4{,}766\Omega \approx 4.7k\Omega$$

$$\text{step size} = \frac{I_{FS}}{\text{number of steps}} = \frac{2.0 \times 10^{-3}}{31} = 64.5\mu A/\text{step}$$

Comparing R_{TOP} and R_{BOTTOM} of the two cases, one can see that I_{FS} = 0.5mA is more attractive because the resistances are higher.

A similar article was published September 18, 2008 on the *EDN* website.

Related Parts		
DS4402	Two/Four-Channel, I²C Adjustable Current DAC	Free Samples
DS4404	Two/Four-Channel, I²C Adjustable Current DAC	Free Samples
DS4412	Dual-Channel, I²C Adjustable Sink/Source Current DAC	Free Samples
DS4424	Two-/Four-Channel, I²C, 7-Bit Sink/Source Current DAC	Free Samples

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