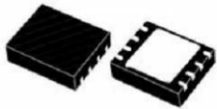# 4 A monolithic step-down current source with synchronous rectification

VFQFPN8 4x4     HSOP8

## Features

- 3.0 V to 18 V operating input voltage range
- 850 kHz fixed switching frequency
- 100 mV typ. current sense voltage drop
- PWM dimming
- ± 7% output current accuracy
- Synchronous rectification
- 95 mΩ HS/ 69 mΩ LS typical $R_{DS(on)}$
- Peak current mode architecture
- Embedded compensation network
- Ceramic output capacitor compliant
- Internal current limiting
- Thermal shutdown

## Applications

- High brightness LED driving
- Signage
- Halogen bulb replacement
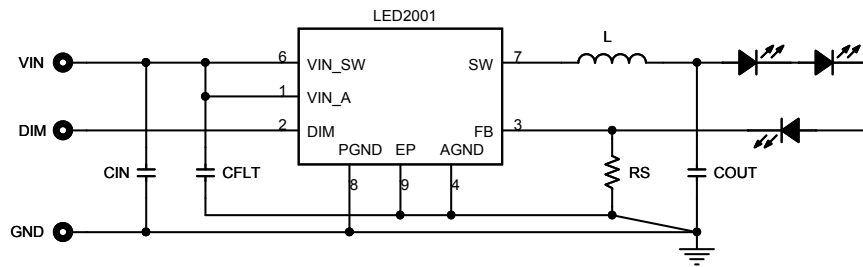- General lighting

| Product status link |
| --- |
| LED2001 |

## Description

The LED2001 is an 850 kHz fixed switching frequency monolithic step-down DC-DC converter designed to operate as precise constant current source with an adjustable current capability up to 4 A DC. The embedded PWM dimming circuitry features LED brightness control. The regulated output current is set connecting a sensing resistor to the feedback pin. The embedded synchronous rectification and the 100 mV typical $R_{SENSE}$ voltage drop enhance the efficiency performance.

The size of the overall application is minimized thanks to the high switching frequency and ceramic output capacitor compatibility. The device is fully protected against thermal overheating, overcurrent and output short-circuit. The LED2001 is available in VFQFPN 4x4 mm 8-lead package, and HSOP8.

**DS9524 - Rev 2 - June 2018**
For further information contact your local STMicroelectronics sales office.

www.st.com

# 1 Typical application circuit

**Figure 1. Typical application circuit**



AM12892v1

# 2 Pin settings

## 2.1 Pin connection

**Figure 2. Pin connection (top view)**
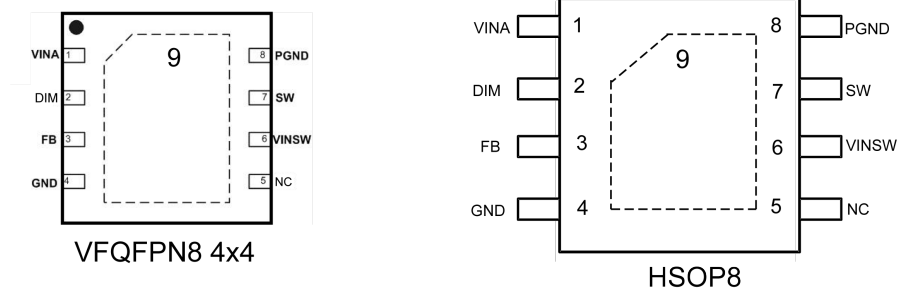


VFQFPN8 4x4

HSOP8

AM12893v1

## 2.2 Pin description

**Table 1. Pin description**

| VFQFPN8 4x4 mm | HS0P8 | Type | Description |
|---|---|---|---|
| 1 | 1 | $VIN_A$ | Analog circuitry power supply connection |
| 2 | 2 | DIM | Dimming control input. Logic low prevents the switching activity, logic high enables it. A square wave on this pin implements LED current PWM dimming. Connect to $VIN_A$ if not used (see Section 6.6 Dimming operation) |
| 3 | 3 | FB | Feedback input. Connect a proper sensing resistor to set the LED current |
| 4 | 4 | AGND | Analog circuitry ground connection |
| 5 | - | NC | Not connected |
| 6 | 6 | $VIN_{SW}$ | Power input voltage |
| 7 | 7 | SW | Regulator switching pin |
| 8 | 8 | PGND | Power ground |
| Exposed pad | Exposed pad | Exposed pad | Connect the exposed pad to AGND |

# 3    Maximum ratings

Table 2. **Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{INSW}$ | Power input voltage | -0.3 to 20 | V |
| $V_{INA}$ | Input voltage | -0.3 to 20 | V |
| $V_{DIM}$ | Dimming voltage | -0.3 to ($V_{INA}$) | V |
| $V_{SW}$ | Output switching voltage | -1 to $V_{IN}$ | V |
| $V_{PG}$ | Power Good | -0.3 to $V_{IN}$ | V |
| $V_{FB}$ | Feedback voltage | -0.3 to 2.5 | V |
| $I_{FB}$ | FB current | -1 to +1 | mA |
| $P_{TOT}$ | Power dissipation at $T_A$ < 60 °C | 2 | °C |
| $T_{OP}$ | Operating junction temperature range | -40 to 150 | °C |
| $T_{STG}$ | Storage temperature range | -55 to 150 | °C |

Table 3. **Thermal data**

| Symbol | Parameter | | Value | Unit |
|--------|-----------|---|-------|------|
| $R_{th\ JA}$ | Maximum thermal resistance junction-ambient[1] | VFQFPN8 4x4 | 40 | °C/W |
| | | HSOP8 | | |

1.   *Package mounted on the evaluation board.*

# 4 Electrical characteristics

$T_J$ = 25 °C, $V_{CC}$ = 12 V, unless otherwise specified.

**Table 4. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Operating input voltage range | [1] | 3 | | 18 | V |
| | Device ON level | | 2.6 | 2.75 | 2.9 | |
| | Device OFF level | | 2.4 | 2.55 | 2.7 | |
| $V_{FB}$ | feedback Voltage | $T_j$=25 °C [1] | 90 | 97 | 104 | mV |
| | | $T_j$= 125 °C | 90 | 100 | 110 | |
| $I_{FB}$ | $V_{FB}$ pin bias current | [1] | | | 600 | nA |
| $R_{DS(on)}$-P | High-side switch on-resistance | $I_{SW}$=750 mA | | 95 | | mΩ |
| $R_{DS(on)}$-N | Low-side switch on-resistance | | | 69 | | |
| $I_{LIM}$ | Maximum limiting current | [2] | | 5.6 | | A |
| **Oscillator** | | | | | | |
| $f_{SW}$ | Switching frequency | | 0.7 | 0.85 | 1 | MHz |
| D | Duty cycle | [2] | 0 | | 100 | % |
| **DC characteristics** | | | | | | |
| $I_Q$ | Quiescent current | | | 1.5 | 2.5 | mA |
| **Dimming** | | | | | | |
| $V_{DIM}$ | DIM threshold voltage | Switching activity | 1.2 | | | V |
| | | Switching activity prevented | | | 0.4 | |
| $I_{DIM}$ | DIM current | | | 2 | | µA |
| **Soft-start** | | | | | | |
| $T_{SS}$ | Soft-start duration | | | 1 | | ms |
| **Protection** | | | | | | |
| $T_{SHDN}$ | Thermal shutdown | | | 150 | | °C |
| | Hysteresis | | | 15 | | |

1. Specifications referred to $T_J$ from -40 to +125 °C. Specifications in the -40 to +125 °C temperature range are assured by design, characterization and statistical correlation.
2. Guaranteed by design.

# 5 Functional description

The LED2001 is based on a "peak current mode" architecture with fixed frequency control. As a consequence the intersection between the error amplifier output and the sensed inductor current generates the control signal to drive the power switch.

The main internal blocks shown in the block diagram in Figure 3. LED2001 block diagram are:

- High-side and low-side embedded power element for synchronous rectification
- A fully integrated sawtooth oscillator with a typical frequency of 850 kHz
- A transconductance error amplifier
- A high-side current sense amplifier to track the inductor current
- A pulse width modulator (PWM) comparator and the circuitry necessary to drive the internal power element
- The soft-start circuitry to decrease the inrush current at power-up
- The current limitation circuit based on the pulse-by-pulse current protection with frequency divider
- The dimming circuitry for output current PWM
- The thermal protection function circuitry

**Figure 3.** LED2001 block diagram
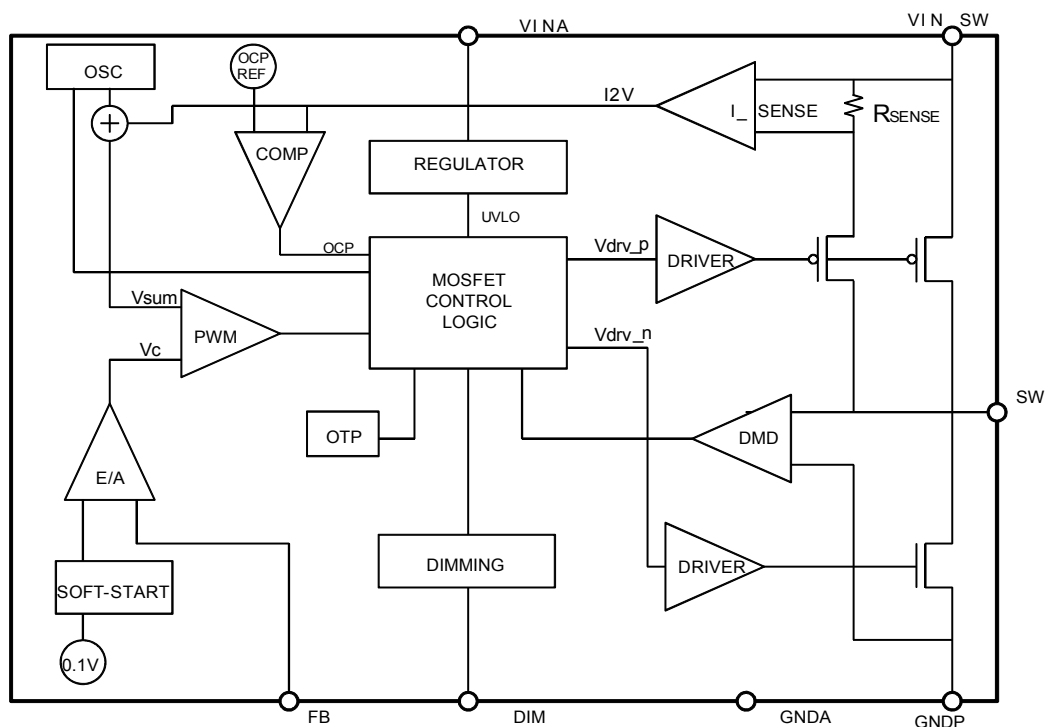


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## 5.1 Power supply and voltage reference

The internal regulator circuit consists of a start-up circuit, an internal voltage pre-regulator, the bandgap voltage reference and the bias block that provides current to all the blocks. The starter supplies the start-up current to the entire device when the input voltage goes high and the device is enabled. The pre-regulator block supplies the bandgap cell with a pre-regulated voltage that has a very low supply voltage noise sensitivity.

## 5.2 Voltage monitor

An internal block continuously senses the $V_{cc}$, $V_{ref}$ and $V_{bg}$. If the monitored voltages are good, the regulator begins operating. There is also a hysteresis on the $V_{cc}$ (UVLO).

**Figure 4. Internal circuit**
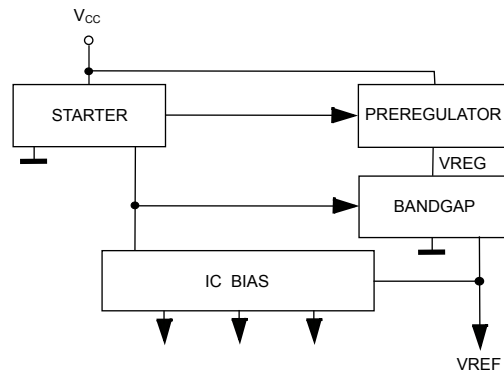


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## 5.3 Soft-start

The start-up phase is implemented ramping the reference of the embedded error amplifier in 1 ms typ. time. It minimizes the inrush current and decreases the stress of the power components at power up.

During normal operation a new soft-start cycle takes place in case of:

- thermal shutdown event
- UVLO event

The soft-start is disabled when DIM input goes high in order to maximize the dimming performance.

## 5.4 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non-inverting input is connected to the internal voltage reference (100 mV), while the inverting input (FB) is connected to the output current sensing resistor. The error amplifier is internally compensated to minimize the size of the final application.

**Table 5. Uncompensated error amplifier characteristics**

| Description | Values |
|:---:|:---:|
| Transconductance | 220 µS |
| Low frequency gain | 96 dB |
| $C_C$ | 195 pF |
| $R_C$ | 70 kΩ |

The error amplifier output is compared with the inductor current sense information to perform PWM control.

## 5.5 Thermal shutdown

The shutdown block generates a signal that disables the power stage if the temperature of the chip goes higher than a fixed internal threshold (150 ± 10 °C typical). The sensing element of the chip is close to the PDMOS area, ensuring fast and accurate temperature detection. A 15 °C typical hysteresis prevents the device from turning ON and OFF continuously during the protection operation.

# 6 Application notes

## 6.1 Closing the loop

**Figure 5. Block diagram of the loop**
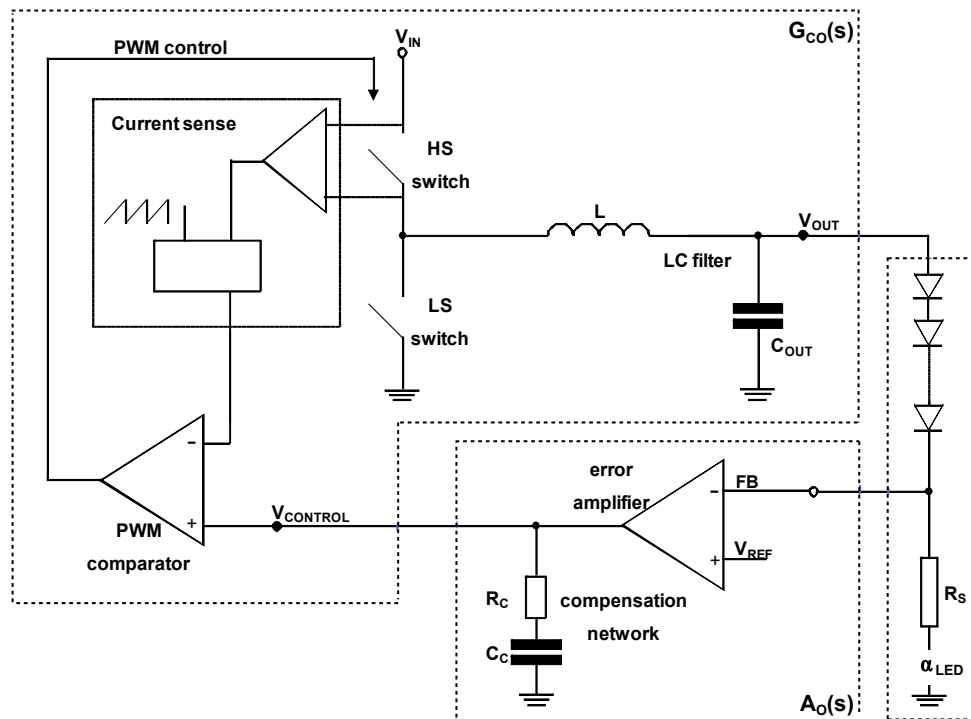


AM13490v1

## 6.2 G<sub>CO</sub>(s) control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as follows:
**Equation 1**

$$G_{CO}(s) = \frac{R_0}{R_i} \cdot \frac{1}{1 + \frac{R_0 \cdot T_{SW}}{L} \cdot \left[ m_C \cdot \left(1 - D\right) - 0.5\right]} \cdot \frac{\left(1 + \frac{s}{W_z}\right)}{\left(1 + \frac{s}{W_p}\right)} \cdot F_H(s)$$

where $R_0$ represents the load resistance, $R_i$ the equivalent sensing resistor of the current sense circuitry , $\omega_p$ the single pole introduced by the LC filter and $\omega_z$ the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.
**Equation 2**

$$\omega_z = \frac{1}{ESR \cdot C_{OUT}}$$

where ESR is the equivalent series resistor to the output capacitor.
**Equation 3**

$$\omega_P = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_C \cdot (1-D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}}$$

where:

**Equation 4**

$$m_C = 1 + \frac{S_e}{S_n}$$

$$S_e = V_{pp} \cdot f_{sw}$$

$$S_n = \frac{V_{IN} - V_{OUT}}{L} \cdot R_i$$

$S_n$ represents the slope of the sensed inductor current, $S_e$ the slope of the external ramp ($V_{PP}$ peak to peak amplitude equal to 1.2 V) that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

The sampling effect contribution $F_H(s)$ is:

**Equation 5**

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_P} + \frac{s^2}{\omega_n^2}}$$

where:

**Equation 6**

$$\omega_n = \pi \cdot f_{SW}$$

and

**Equation 7**

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1-D) - 0.5]}$$

## 6.3 Error amplifier compensation network

The LED2001 embeds ( see figure below) the error amplifier and a pre-defined compensation network, which stabilize the system in most application conditions.

Figure 6. **Transconductance embedded error amplifier**
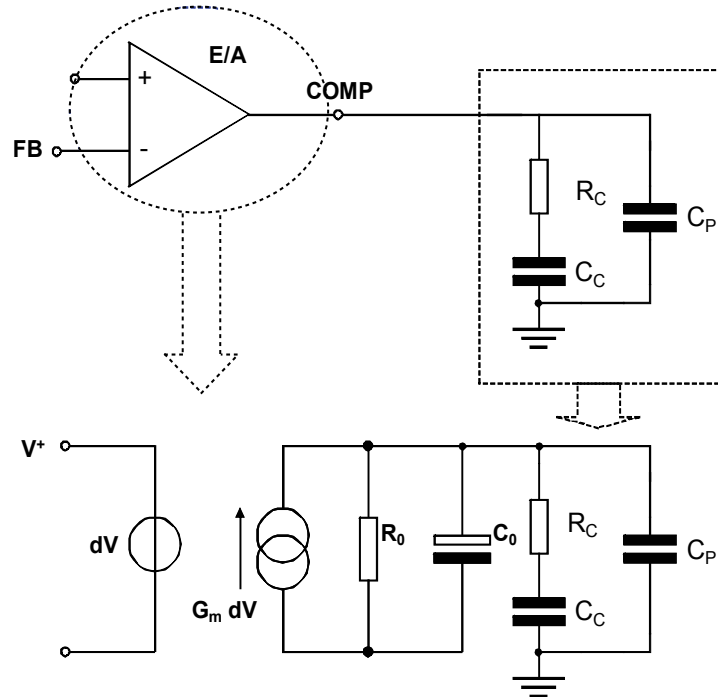


AM13491v1

$R_C$ and $C_C$ introduce a pole and a zero in the open loop gain. $C_P$ does not significantly affect system stability but it can be useful to reduce the noise at the output of the error amplifier.

The transfer function of the error amplifier and its compensation network is:

**Equation 8**

$$A_0(s) = \frac{A_{V0} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_c \cdot C_c + s \cdot (R_0 \cdot C_c + R_0 \cdot (C_0 + C_p) + R_c \cdot C_c) + 1}$$

Where $A_{V0} = G_m \cdot R_0$.

The poles of this transfer function are (if $C_c \gg C_0 + C_P$):

**Equation 9**

$$f_{P\,LF} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c}$$

**Equation 10**

$$f_{P\,HF} = \frac{1}{2 \cdot \pi \cdot R_c \cdot (C_0 + C_p)}$$

whereas the zero is defined as:

**Equation 11**

$$F_Z = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c}$$

The embedded compensation network is $R_C$=70 K, $C_C$=195 pF while $C_P$ and $C_O$ can be considered as negligible. The error amplifier output resistance is 240 MΩ, so the relevant singularities are:

**Equation 12**

$f_Z$ = 11.6 kHz

$f_{PLF}$ = 3.4 Hz

## 6.4 LED small signal model

Once the system reaches the working condition, LEDs composing the row are biased and their equivalent circuit can be considered as a resistor for frequencies << 1 MHz.

The LED manufacturer typically provides the equivalent dynamic resistance of the LED biased at different DC currents. This parameter is required to study the behavior of the system in the small signal analysis.

For instance, the equivalent dynamic resistance of Luxeon III Star from Lumiled measured with different biasing current levels is reported below:

**Equation 13**:

$r_{LED}$ { 1.3 Ω $I_{LED}$ = 350 mA; 0.9 Ω $I_{LED}$ = 700 mA;

If the LED datasheet does not report the equivalent resistor value, it can be simply derived as the tangent to the diode I-V characteristic in the present working point (see Figure 7. Equivalent series resistor).

**Figure 7. Equivalent series resistor**
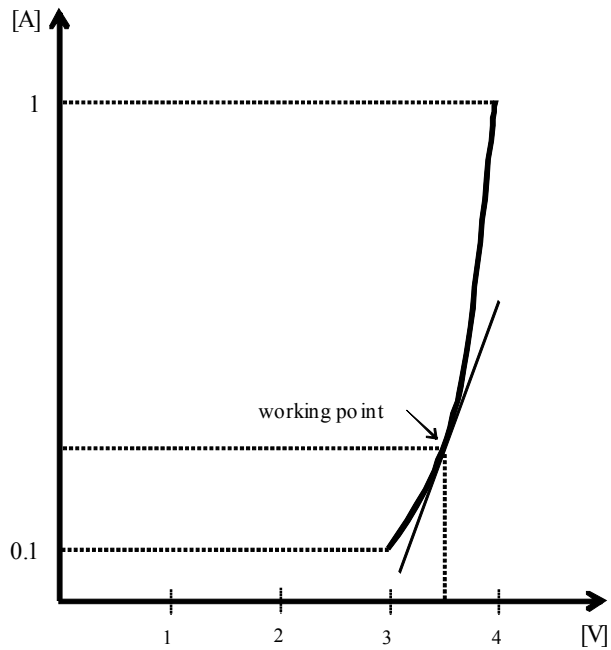


AM13492v1

Figure 8. Load equivalent circuit shows the equivalent circuit of the LED constant current generator.

**Figure 8. Load equivalent circuit**
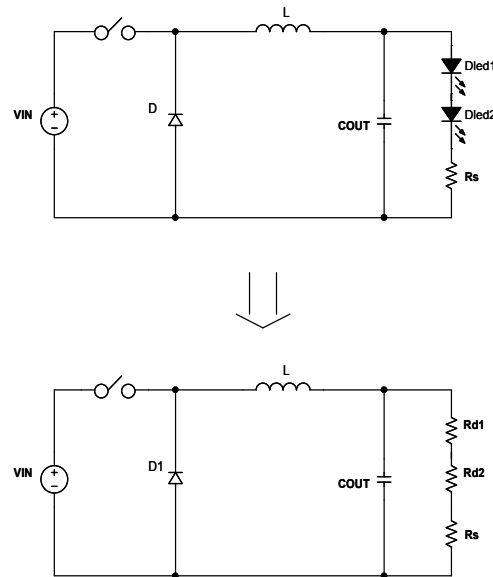


AM13493v1

As a consequence the LED equivalent circuit gives the $\alpha_{LED}(s)$ term correlating the output voltage with the high impedance FB input:

**Equation 14**

$$\alpha_{LED}(n_{LED}) = \frac{R_{SENSE}}{n_{LED} \cdot r_{LED} + R_{SENSE}}$$

## 6.5 Total loop gain

In summary, the open loop gain can be expressed as:

**Equation 15**

$$G(s) = G_{CO}(s) \cdot A_0(s) \cdot \alpha_{LED}(n_{LED})$$

**Example 1**

Design specification:

$V_{IN}$=12 V, $V_{FW\_LED}$=3.5 V, $n_{LED}$= 2, $r_{LED}$= 1.1 Ω, $I_{LED}$= 4 A, $I_{LED\ RIPPLE}$= 2%

The inductor and capacitor value are dimensioned in order to meet the ILED RIPPLE

specification (see Section 6.8.2 Inductor and output capacitor selection for output capacitor and inductor selection guidelines):

L=2.2 µH, $C_{OUT}$=2.2 µF MLCC (negligible ESR)

Accordingly, with Section 6.8.1 Sensing resistor the sensing resistor value is:

**Equation 16**

$$R_S = \frac{100mV}{4A} = 25\ m\Omega$$

**Equation 17**

$$\alpha_{LED}(n_{LED}) = \frac{R_{SENSE}}{n_{LED} \cdot r_{LED} + R_{SENSE}} = \frac{25\ m\Omega}{2 \times 1.1\Omega + 25\ m\Omega} = 0.011$$

The gain and phase margin Bode diagrams are plotted respectively in the figures below.

**Figure 9. Module plot**
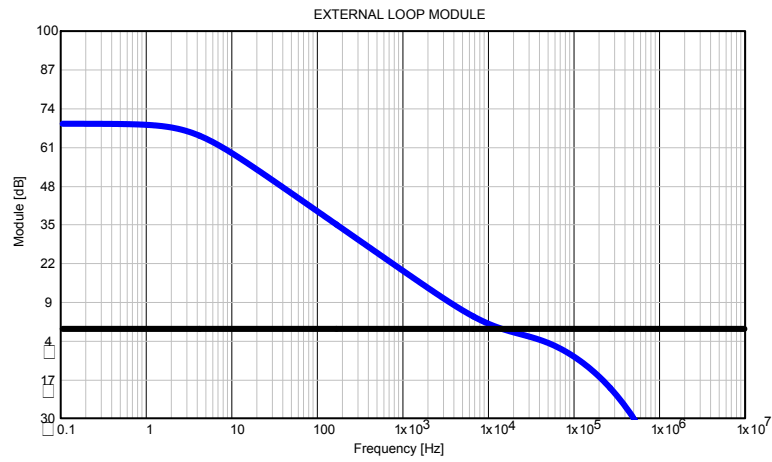


AM12900v1

**Figure 10. Phase plot**
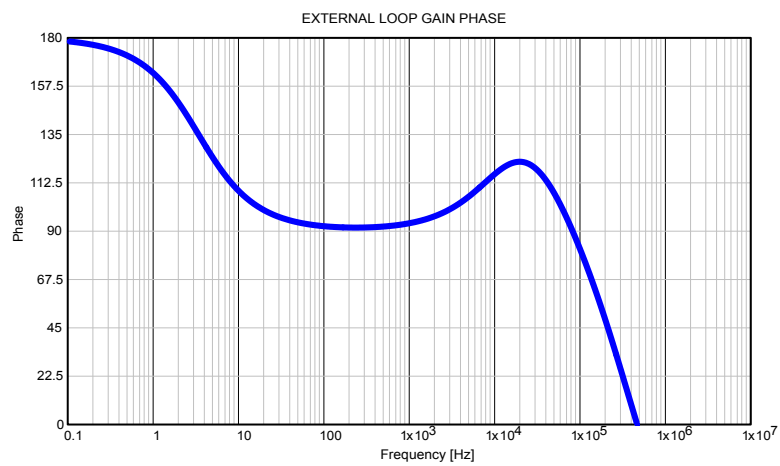


AM12901v1

The cut-off frequency and the phase margin are:

**Equation 18:**

$f_c$ = 14 kHz

pm = 120°

## 6.6 Dimming operation

The dimming input disables the switching activity, masking the PWM comparator output.

The inductor current dynamic performance when dimming input goes high depends on the designed system response. The best dimming performance is obtained by maximizing the bandwidth and phase margin, when possible.

As a general rule, the output capacitor minimization improves dimming performance.

**Figure 11. Dimming operation example**
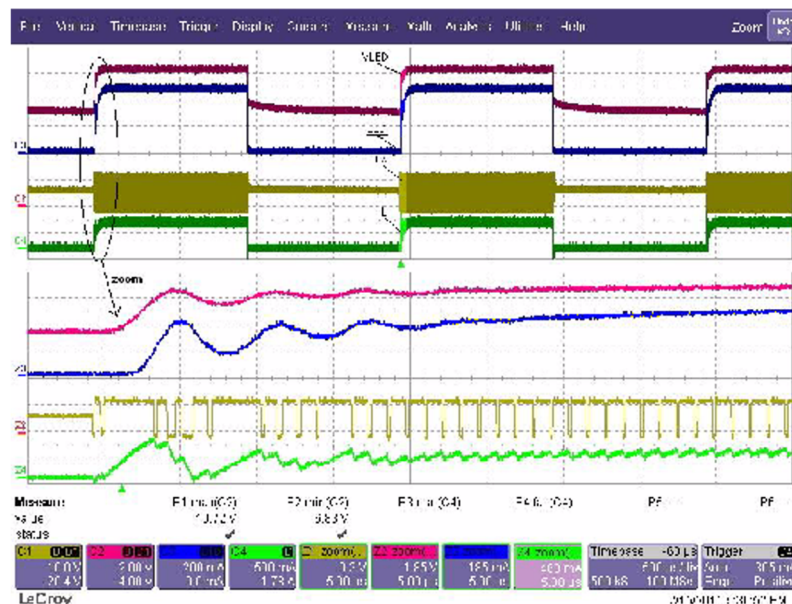


AM12902v1

In fact, when dimming enables the switching activity, a small capacitor value is fast charged with low inductor value. As a consequence, the LED current rising edge time is improved and the inductor current oscillation reduced. An oversized output capacitor value requires extra current for fast charge so generating an inductor current oscillations.

The switching activity is prevented as soon as the dimming signal goes low. Nevertheless, the LED current drops to zero only when the voltage, stored in the output capacitor, goes below a minimum voltage determined by the selected LEDs. As a consequence, a big capacitor value makes the LED current falling time worse than a smaller one.

The LED2001 device embeds dedicated circuitry to improve LED current falling time.

As soon as the dimming input goes low, the low-side is kept enabled to discharge $C_{OUT}$ until the LED current drops to 60% of the nominal current. A negative current limitation (-1 A typical) protects the device during this operation, see figure below.

**Figure 12. LED current falling edge operation**
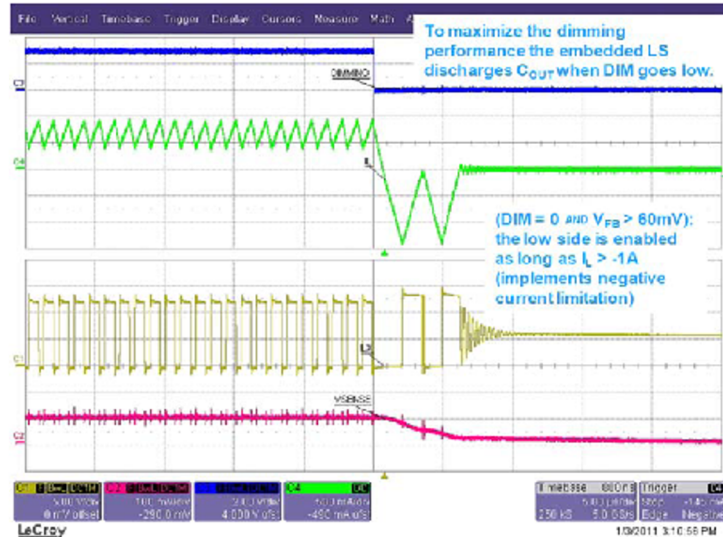


AM12903v1

### 6.6.1 Dimming frequency vs. dimming depth

As seen in Section 6.6 Dimming operation, the LEDs current rising and falling edge time mainly depends on the system bandwidth ($T_{RISE}$) and the selected output capacitor value ($T_{RISE}$ and $T_{FALL}$).

The dimming performance depends on the minimum current pulse shape specification of the final application. The ideal minimum current pulse has a rectangular shape, in any case it degenerates into a trapezoid or, at worst, into a triangle, depending on the ratio ($T_{RISE} + T_{FALL}$)/ $T_{DIM}$.

**Equation 19**

$$\begin{array}{ccc} \textbf{rectangle} & \textbf{trapezoid} & \textbf{triangle} \\ \dfrac{T_{RISE} + T_{FALL}}{T_{DIM}} \ll 1 \quad \square & \dfrac{T_{RISE} + T_{FALL}}{T_{DIM}} < 1 \quad \square & \dfrac{T_{RISE} + T_{FALL}}{T_{DIM}} = 1 \end{array}$$

The small signal response in Figure 11. Dimming operation example and Figure 12. LED current falling edge operation is considered as an example.

**Equation 20**

$T_{RISE} \cong 20 \ \mu s$

$T_{FALL} \cong 5 \ \mu s$

Assuming the minimum current pulse shape specification as:

**Equation 21**

$T_{RISE} + T_{FALL} = 0.5 \ \cdot D_{MIN} \ \cdot T_{DIMMING}$

it is possible to calculate the maximum dimming depth given the dimming frequency or vice versa.

**Figure 13. Dimming signal**
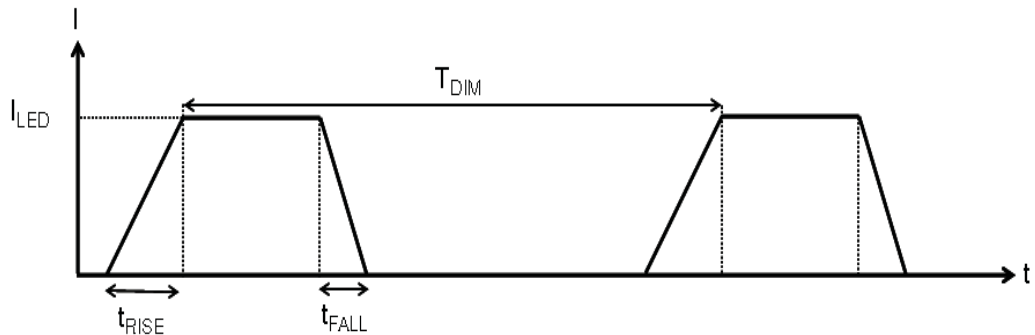


AM13499v1

For example, assuming a 1 kHz dimming frequency the maximum dimming depth is 5% or given a 2% dimming depth it follows a 200 Hz maximum $f_{DIM}$.

The LED2001 dimming performance is strictly dependent on the system small signal response. As a consequence, an optimized compensation network (good phase margin and bandwidth maximized) and minimized $C_{OUT}$ value are crucial for best performance.

## 6.7 eDesign studio software

The LED2001 is supported by the eDesign software which can be viewed online at www.st.com.

**Figure 14. eDesign studio software**
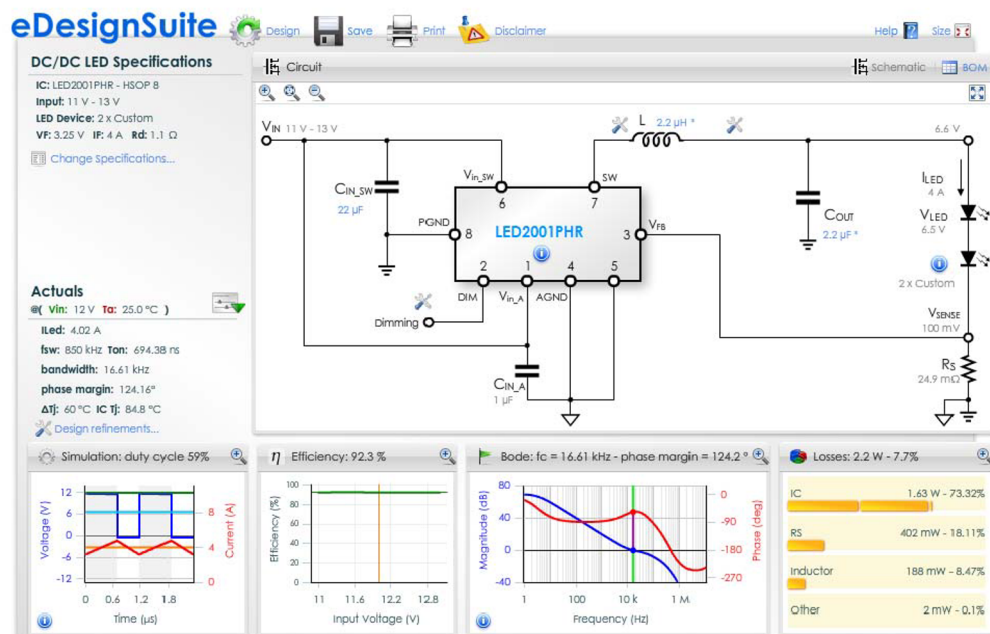


The software easily supports the component sizing according to the technical information given in this datasheet (see Section 6 Application notes and Section 6.8 Component selection).

The end user is requested to fill in the requested information such as the input voltage range, the selected LED parameters and the number of LEDs composing the row.

The software calculates external components according to the internal database. It is also possible to define new components and ask the software to use them.

Bode plots, estimated efficiency and thermal performance are provided.

Finally, the user can save the design and print all the information including the bill of material of the board.

## 6.8 Component selection

### 6.8.1 Sensing resistor

In closed loop operation the LED2001 feedback pin voltage is 100 mV, so the sensing resistor calculation is expressed as:

**Equation 22**

$$R_S = \frac{100mV}{I_{LED}}$$

Since the main loop (see Section 6.1 Closing the loop ) regulates the sensing resistor voltage drop, the average current is regulated into the LEDs. The integration period is at minimum 5 * $T_{SW}$ since the system bandwidth can be dimensioned up to $f_{SW}/5$ at maximum.

The system performs the output current regulation over a period, which is at least five times longer than the switching frequency. The output current regulation neglects the ripple current contribution and its reliance on external parameters like input voltage and output voltage variations (line transient and LED forward voltage spread). This performance cannot be achieved with simpler regulation loops like hysteretic control.

For the same reason, the switching frequency is constant over the application conditions, that helps to tune the EMI filtering and to guarantee the maximum LED current ripple specification in the application range. This performance cannot be achieved using constant ON/OFF time architectures.

### 6.8.2 Inductor and output capacitor selection

The output capacitor filters the inductor current ripple that, given the application condition, depends on the inductor value. As a consequence the LED current ripple, that is the main specification for a switching current source, depends on the inductor and output capacitor selection.

**Figure 15. Equivalent circuit**
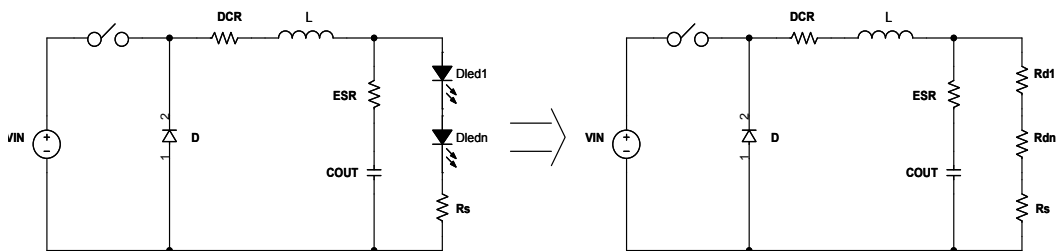


AM13500v1

The LED ripple current can be calculated as the inductor ripple current ratio flowing into the output impedance using the Laplace transform (see Figure 2):

**Equation 23**

$$\Delta I_{RIPPLE}(s) = \frac{\frac{8}{\pi^2} \cdot \Delta I_L \cdot (1 + s \cdot ESR \cdot C_{OUT})}{1 + s \cdot (R_S + ESR + n_{LED} \cdot R_{LED}) \cdot C_{OUT}}$$

where the term $8/\pi^2$ represents the main harmonic of the inductor current ripple (which has a triangular shape) and $\Delta I_L$ is the inductor current ripple.

**Equation 24**

$$\Delta I_L = \frac{V_{OUT}}{L} \cdot T_{OFF} = \frac{n_{LED} \cdot V_{FW\_LED} + 100mV}{L} \cdot T_{OFF}$$

so L value can be calculated as:

**Equation 25**

$$L = \frac{n_{LED} \cdot V_{FW\_LED} + 100mV}{\Delta I_L} \cdot T_{OFF} = \frac{n_{LED} \cdot V_{FW\_LED} + 100mV}{\Delta I_L} \cdot \left(1 - \frac{n_{LED} \cdot V_{FW\_LED} + 100mV}{V_{IN}}\right)$$

where $T_{OFF}$ is the OFF time of the embedded high switch, given by 1 - D.

As a consequence the lower the inductor value (so higher the current ripple), the higher $C_{OUT}$ value to meet the specification.

A general rule to dimension L value is:

**Equation 26**

$$\frac{\Delta I_L}{I_{LED}} \leq 0.5$$

Finally the required output capacitor value can be calculated equalizing the LED current ripple specification with the module of the Fourier transformer (see Equation 23) calculated at $f_{SW}$ frequency.

**Equation 27**

$$\left|\Delta I_{RIPPLE}(s = j \cdot \omega)\right| = \Delta I_{RIPPLE\_SPEC}$$

**Example 1**

$V_{IN}$ = 12 V, $I_{LED}$ = 700 mA, $\Delta I_{LED}/I_{LED}$ = 2%, $V_{FW\_LED}$ = 3.7 V, $n_{LED}$ = 2.

A lower inductor value maximizes the inductor current slew rate for better dimming performance. Equation 26 becomes:

**Equation 28**

$$\frac{\Delta I_L}{I_{LED}} = 0.5$$

which is satisfied selecting a 10 µH inductor value.

The output capacitor value has to be dimensioned according to Equation 27.

Finally, given the selected inductor value, a 2.2 µF ceramic capacitor value keeps the LED current ripple ratio lower than the 2% of the nominal current. An output ceramic capacitor type (negligible ESR) is suggested to minimize the ripple contribution given a fixed capacitor value.

**Table 6. Inductor selection**

| Manufacturer | Series | Inductor value (µH) | Saturation current (A) |
|---|---|---|---|
| Wurth Elektronik | WE-HCI 7040 | 1 to 4.7 | 20 to 7 |
| | WE-HCI 7050 | 4.9 to 10 | 20 to 4.0 |
| Coilcraft | XPL 7030 | 2.2 to 10 | 29 to 7.2 |

### 6.8.3 Input capacitor

The input capacitor must be able to support the maximum input operating voltage and the maximum RMS input current.

Since step-down converters draw current from the input in pulses, the input current is squared and the height of each pulse is equal to the output current. The input capacitor has to absorb all this switching current, whose RMS value can be up to the load current divided by two (worst case, with duty cycle of 50%). For this reason, the quality of these capacitors has to be very high to minimize the power dissipation generated by the internal ESR, thereby improving system reliability and efficiency. The critical parameter is usually the RMS current rating, which must be higher than the RMS current flowing through the capacitor. The maximum RMS input current (flowing through the input capacitor) is:

**Equation 29**

$$I_{RMS} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

Where $\eta$ is the expected system efficiency, D is the duty cycle and $I_O$ is the output DC current. Considering $\eta$ = 1 this function reaches its maximum value at D = 0.5 and the equivalent RMS current is equal to $I_O$ divided by 2. The maximum and minimum duty cycles are:

**Equation 30**

$$D_{MAX} = \frac{V_{OUT} + V_F}{V_{INMIN} - V_{SW}}$$

and

**Equation 31**

$$D_{MIN} = \frac{V_{OUT} + V_F}{V_{INMAX} - V_{SW}}$$

Where $V_F$ is the freewheeling diode forward voltage and $V_{SW}$ the voltage drop across the internal PDMOS. Considering the range $D_{MIN}$ to $D_{MAX}$, it is possible to determine the max. $I_{RMS}$ going through the input capacitor.

Capacitors that can be considered are:

•     Electrolytic capacitors:

These are widely used due to their low price and their availability in a wide range of RMS current ratings.

The only drawback is that, considering ripple current rating requirements, they are physically larger than other capacitors.

•     Ceramic capacitors:

If available for the required value and voltage rating, these capacitors usually have a higher RMS current rating for a given physical dimension (due to very low ESR).

The drawback is the considerably high cost.

•     Tantalum capacitors:

Small tantalum capacitors with very low ESR are more available. However, they can occasionally burn if subjected to very high current during charge.

Therefore, it is suggested to avoid this type of capacitor for the input filter of the device as they could be stressed by a high surge current when connected to the power supply.

**Table 7. List of ceramic capacitors for the LED2001**

| Manufacturer | Series | Capacitor value (µC) | Rated voltage (V) |
|---|---|---|---|
| Taiyo Yuden | UMK325BJ106MM-T | 10 | 50 |
| Murata | GRM42-2 X7R 475K 50 | 4.7 | 50 |

In case the selected capacitor is ceramic (so neglecting the ESR contribution), the input voltage ripple can be calculated as:

**Equation 32**

$$V_{IN\ PP} = \frac{I_O}{C_{IN} \cdot f_{SW}} \cdot \left[\left(1 - \frac{D}{\eta}\right) \cdot D + \frac{D}{\eta} \cdot (1 - D)\right]$$

## 6.9     Layout considerations

The layout of switching DC-DC converters is very important to minimize noise and interference. Power-generating portions of the layout are the main cause of noise and so high switching current loop areas should be kept as small as possible and lead lengths as short as possible.

High impedance paths (in particular the feedback connections) are susceptible to interference, so they should be as far as possible from the high current paths. A layout example is provided in Figure 16. Layout example.

The input and output loops are minimized to avoid radiation and high frequency resonance problems. The feedback pin to the sensing resistor path must be designed as short as possible to avoid pick-up noise. Another important issue is the ground plane of the board. Since the package has an exposed pad, it is very important to connect it to an extended ground plane in order to reduce the thermal resistance junction-to-ambient.

In addition, to increase the design noise immunity, different signal and power ground should be designed in the layout (see Section 6.12 Application circuit). The signal ground serves the small signal components, the device analog ground pin, the exposed pad and a small filtering capacitor connected to the VCC pin. The power ground serves the device ground pin and the input filter. The different grounds are connected underneath the output

capacitor. Neglecting the current ripple contribution, the current flowing through this component is constant during the switching activity and so this is the cleanest ground point of the buck application circuit.

**Figure 16. Layout example**
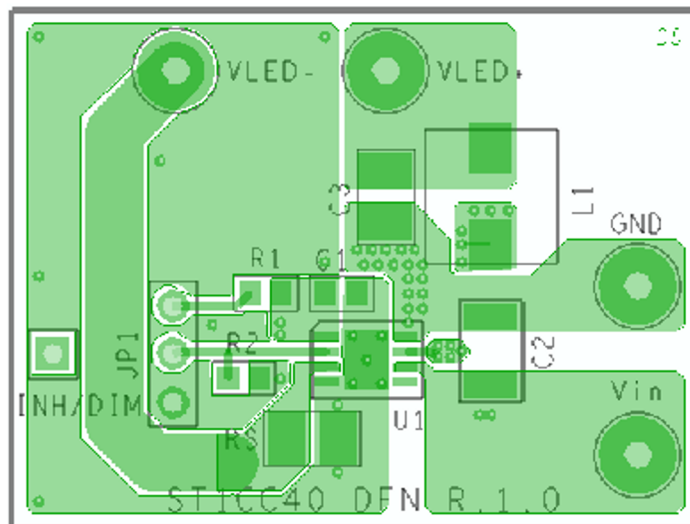


AM12907v1

## 6.10 Thermal considerations

The dissipated power of the device is tied to three different sources:

- Conduction losses due to the $R_{DS(on)}$, which are equal to:

**Equation 33**

$$P_{ON} = R_{RDSON\_HS} \cdot (I_{OUT})^2 \cdot D$$

$$P_{OFF} = R_{RDSON\_LS} \cdot (I_{OUT})^2 \cdot (1 - D)$$

Where D is the duty cycle of the application. Note that the duty cycle is theoretically given by the ratio between $V_{OUT}$ ($n_{LED}$ · $V_{LED}$ + 100 mV) and $V_{IN}$, but in practice it is substantially higher than this value to compensate for the losses in the overall application.

For this reason, the conduction losses related to the $R_{DS(on)}$ increase compared to an ideal case.

- Switching losses due to turning ON and OFF. These are derived using Equation 34:

**Equation 34**

$$P_{SW} = V_{IN} \cdot I_{OUT} \cdot \frac{(T_{RISE} + T_{FALL})}{2} \cdot F_{SW} = V_{IN} \cdot I_{OUT} \cdot T_{SW\_EQ} \cdot F_{SW}$$

Where $T_{RISE}$ and $T_{FALL}$ represent the switching times of the power element that cause the switching losses when driving an inductive load (see Figure 17. Switching losses). $T_{SW}$ is the equivalent switching time.

**Figure 17. Switching losses**
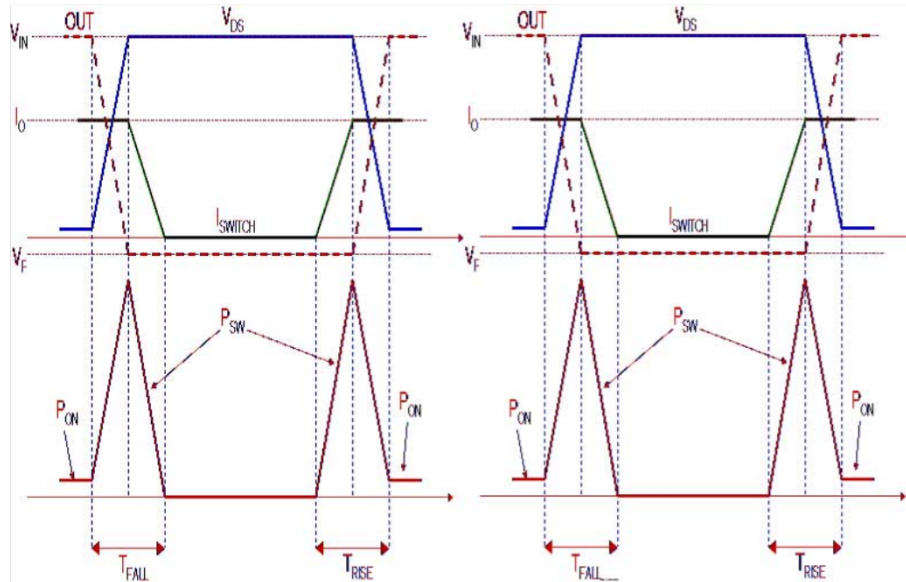


AM12908v1

- Quiescent current losses

**Equation 35**

$$P_Q = V_{IN} \cdot I_Q$$

**Example 2**

(see Compensation network design for alternative topologies):

$V_{IN}$ = 12 V, $V_{FW\_LED}$ = 3.5 V, $n_{LED}$ = 2, $I_{LED}$ = 700 mA.

The typical output voltage is:

**Equation 36**

$$V_{OUT} = n_{LED} \cdot V_{FW\_LED} + V_{FB} = 7.1 \ V$$

$R_{DSON\_HS}$ has a typical value of 95 mΩ and $R_{DSON\_LS}$ is 69 mΩ at 25 °C.

For the calculation we can estimate $R_{DSON\_HS}$ = 140 mΩ and $R_{DSON\_LS}$= 100 mΩ as a consequence of $T_J$ increase during the operation.

$T_{SW\_EQ}$ is approximately 12 ns.

$I_Q$ has a typical value of 1.5 mA at $V_{IN}$ = 12 V.

The overall internal losses are:

**Equation 37**

$$P_{TOT} = R_{DSON\_HS} \cdot (I_{OUT})^2 \cdot D + R_{DSON\_LS} \cdot (I_{OUT})^2 \cdot (1 - D) + V_{IN} \cdot I_{OUT} \cdot f_{sw} \cdot T_{sw} + V_{IN} \cdot I_Q$$

where $T_{SW\_EQ}$ = ($T_{RISE}$ + $T_{FALL}$ )/2 = 12 nS.

**Equation 38**

$$P_{TOT} = 0.14 \cdot 0.7^2 \cdot 0.6 + 0.1 \cdot 0.7^2 \cdot 0.4 + 12 \cdot 10^{-9} \cdot 850 \cdot 10^3 + 12 \cdot 1.5 \cdot 10^{-3} \cong 205mW$$

The junction temperature of the device is:

**Equation 39**

$$T_J = T_A + Rth_{J-A} \cdot P_{TOT}$$

Where $T_A$ is the ambient temperature and $Rth_{J-A}$ is the thermal resistance junction-to-ambient. The junction-to-ambient ($Rth_{J-A}$) thermal resistance of the device assembled in the HSOP8 package and mounted on the evaluation is about 40 °C/W.

Assuming the ambient temperature around 40 °C, the estimated junction temperature is:

$T_J = 60+0.205 \cdot 40 \cong 68\ °C$

## 6.11 Short-circuit protection

In overcurrent protection mode, when the peak current reaches the current limit threshold, the device disables the power element and it is able to reduce the conduction time down to the minimum value (approximately 100 ns typical) to keep the inductor current limited. This is the pulse-by-pulse current limitation to implement constant current protection feature.

In overcurrent condition, the duty cycle is strongly reduced and, in most applications, this is enough to limit the switch current to the current threshold.

The inductor current ripple during ON and OFF phases can be written as:

- ON phase

**Equation 40**

$$\Delta I_{L\ TON} = \frac{V_{IN} - V_{OUT} - (DCR_L + R_{DSON\ HS}) \cdot I}{L}(T_{ON})$$

- OFF phase

**Equation 41**

$$\Delta I_{L\ \ TON} = \frac{-(V_{OUT} + (DCR_L + R_{DSON\_LS}) \cdot I)}{L}(T_{OFF})$$

where $DCR_L$ is the series resistance of the inductor.

The pulse-by-pulse current limitation is effective to implement constant current protection when:

**Equation 42**

$$|\Delta I_{L\ TON}| = |\Delta I_{L\ TOFF}|$$

From Equation 40 and Equation 41 it can be seen that the implementation of the constant current protection becomes more critical the lower is the $V_{OUT}$ and the higher is $V_{IN}$.

In fact, in short-circuit condition the voltage applied to the inductor during the OFF time becomes equal to the voltage drop across parasitic components (typically the DCR of the inductor and the $R_{DS(on)}$) since $V_{OUT}$ is negligible, while during $T_{ON}$ the voltage applied to the inductor is maximized and it is approximately equal to $V_{IN}$.

In general the worst case scenario is a heavy short-circuit at the output with maximum input voltage. Equation 40 and Equation 41 in overcurrent conditions can be simplified to:

**Equation 43**

$$\Delta I_{L\ TON} = \frac{V_{IN} - (DCR_L + R_{DSON\ HS}) \cdot I}{L}(T_{ON\ MIN}) \approx \frac{V_{IN}}{L}(90\,ns)$$

considering $T_{ON}$ that has been already reduced to its minimum.

**Equation 44**

$$\Delta I_{L\ \ TOFF} = \frac{-(DCR_L + R_{DSON\_LS}) \cdot I}{L}(T_{SW} - 90ns) \cong \frac{-(DCR_L + R_{DSON\_LS}) \cdot I}{L} \cdot (1.18\mu s)$$

where $T_{SW} = 1/f_{SW}$ considering the nominal $f_{SW}$.

At higher input voltage $\Delta I_{L\ TON}$ may be higher than $\Delta I_{L\ TOFF}$ and so the inductor current can escalate. As a consequence, the system typically meets Equation 42 at a current level higher than the nominal value thanks to the increased voltage drop across stray components. In most of the application conditions the pulse-by-pulse current limitation is effective to limit the inductor current. Whenever the current escalates, a second level current protection called "Hiccup mode" is enabled. Hiccup protection offers an additional protection against heavy short-circuit conditions at very high input voltage even considering the spread of the minimum conduction time of the power element. If the hiccup current level (6.2 A typical) is triggered, the switching activity is prevented for 12 cycles.

Figure 1 shows the operation of the constant current protection when a short-circuit is applied to the output at the maximum input voltage.

Figure 18. **Constant current protection triggering hiccup mode**
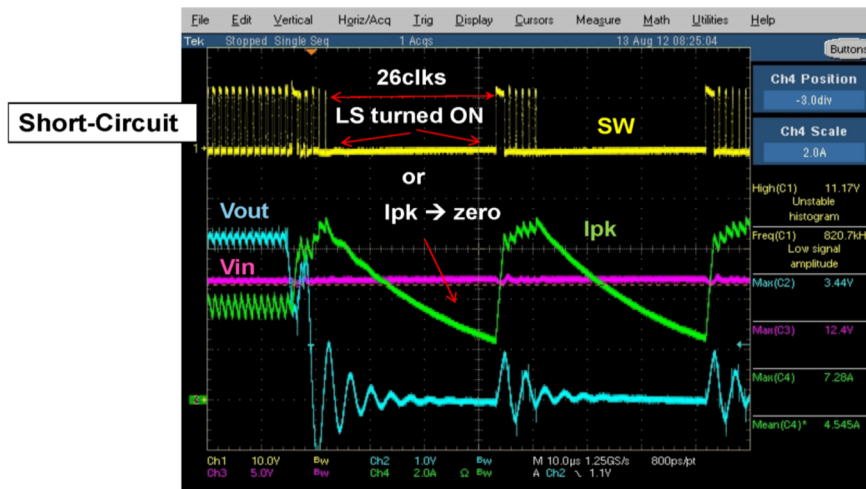


LED2001 Vin=12 V, Iout=4 A, Rsense=0.025 Ohm

During pulse skipping, high-side OFF, low-side keeps ON till 26 clks finish (13 clks for the LED2001) or $I_{pk}$ decreases to be zero value.

## 6.12 Application circuit

**Figure 19. Demonstration board application circuit**
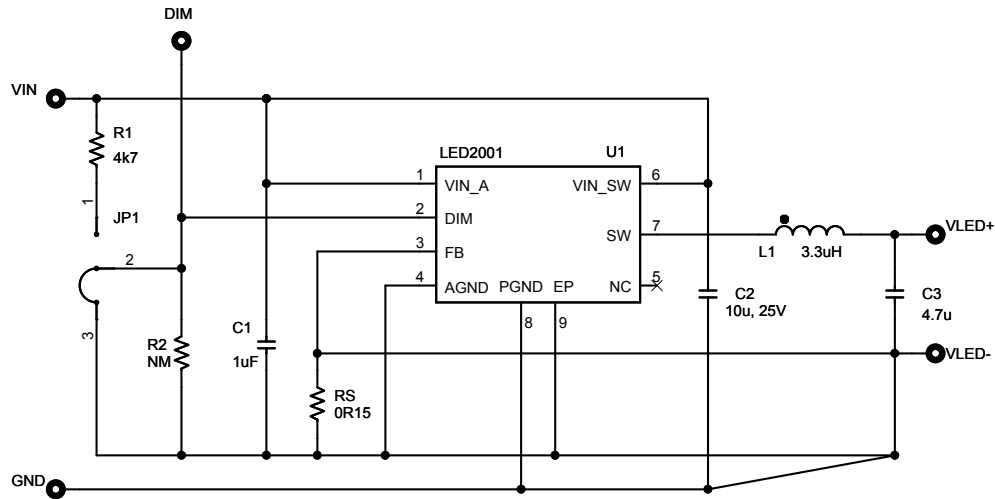


AM12910v1

**Table 8. Component list**

| Reference | Part number | Description | Manufacturer |
|-----------|-------------|-------------|--------------|
| C1 | | 1 µF 25 V (size 0805) | |
| C2 | GRM31CR61E226KE15L | 22 µF 25 V (size 1206) | Murata |
| C3 | GRM21BR71E475KA73L | 4.7 µF 25 V (size 0805) | |
| R1 | | 4.7 kΩ 5% (size 0603) | |
| R2 | | Not mounted | |
| $R_s$ | ERJ14BSFR27U | 0.15 Ω 1% (size 1206) | Panasonic |
| L1 | XAL6030-332MEB | 3.3 µH $I_{SAT}$ = 8.4 A (20% drop) $I_{RMS}$ = 7.3 A (40 °C rise) (size 6.36 x 6.56 x 6.1 mm) | Coilcraft |

**Figure 20. PCB layout (component side) DFN package**
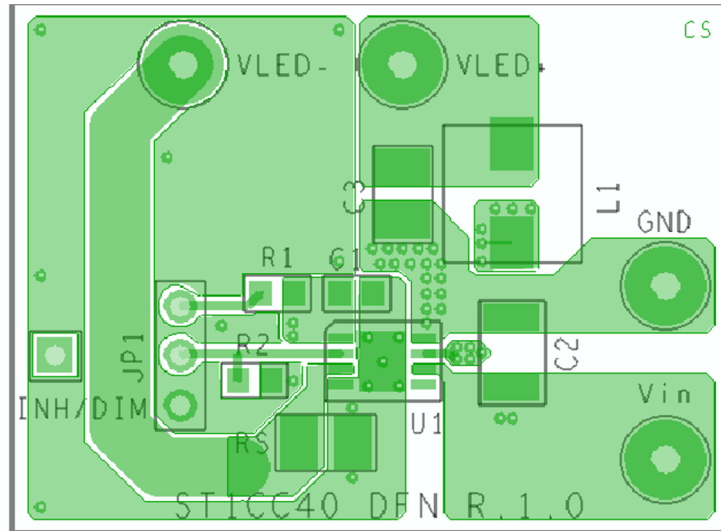


AM12911v1

**Figure 21. PCB layout (bottom side) DFN package**
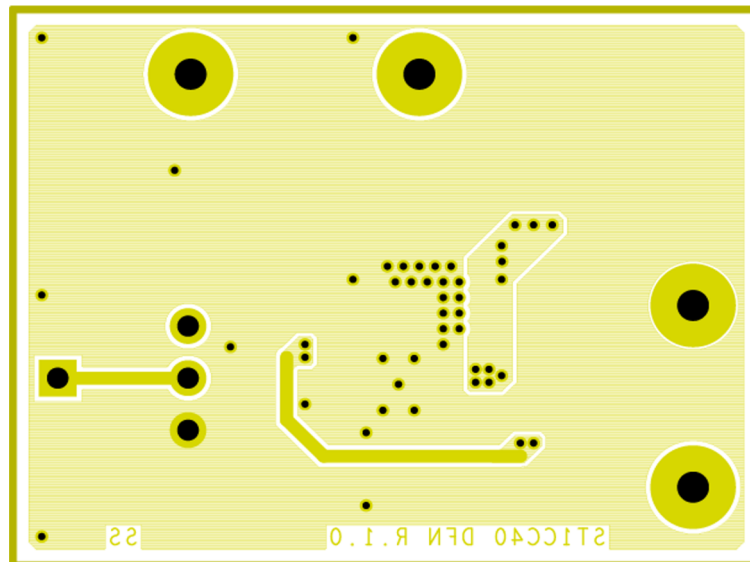


AM12912v1

Figure 22. **PCB layout (component side) HSOP8 package**
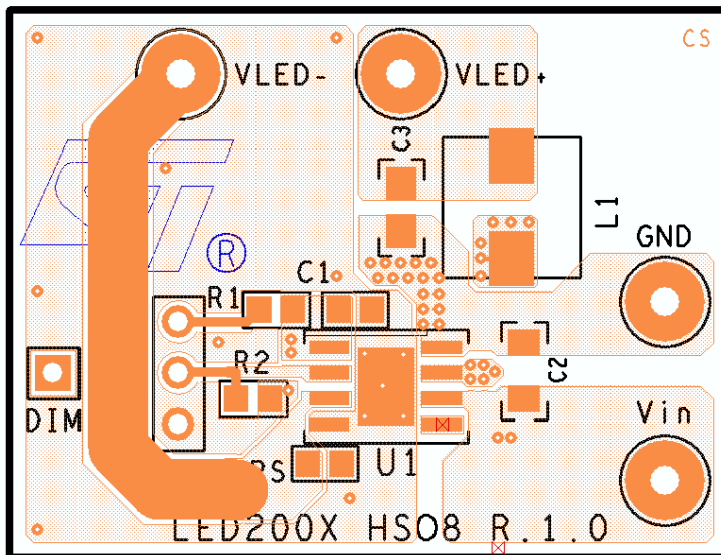


It is strongly recommended that the input capacitors are to be put as close as possible to the pins, see C1 and C2.

Figure 23. **PCB layout (bottom side) HSOP8 package**
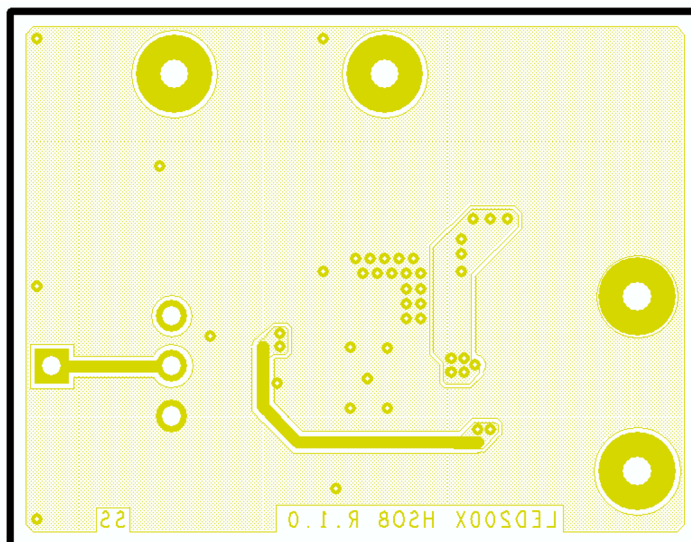
# 7 Typical characteristics

**Figure 24. Soft-start**
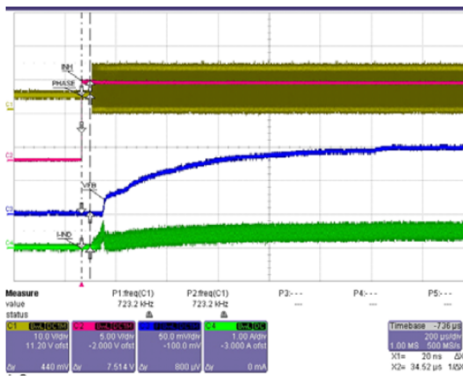


AM12913v1

**Figure 25. Load regulation**
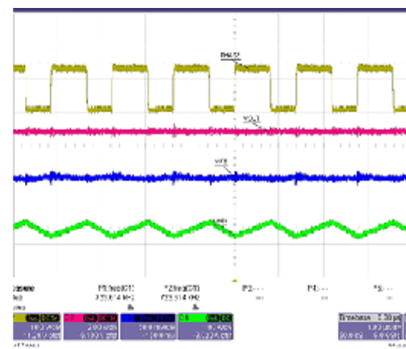


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**Figure 26. Dimming operation**
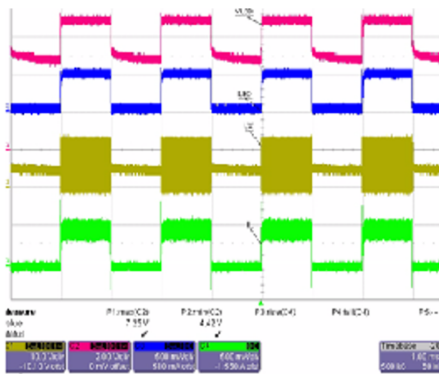


AM12915v1

**Figure 27. LED current rising edge**
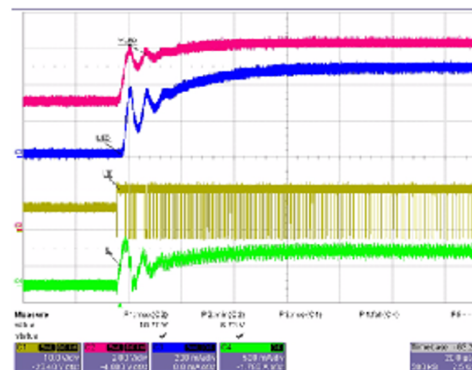


AM12916v1

**Figure 28. LED current falling edge**



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**Figure 29. Hiccup current protection**
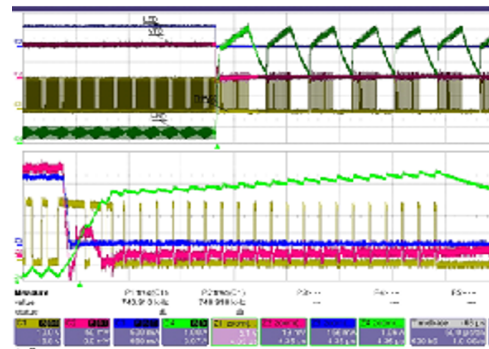


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**Figure 30. OCP blanking time**
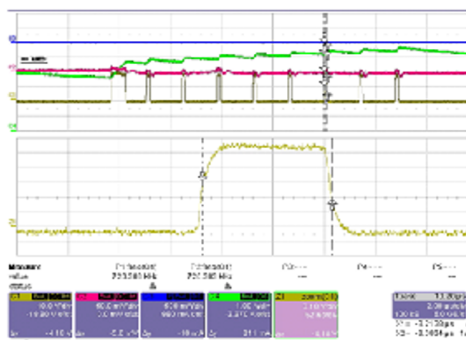


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**Figure 31. Thermal shutdown protection**
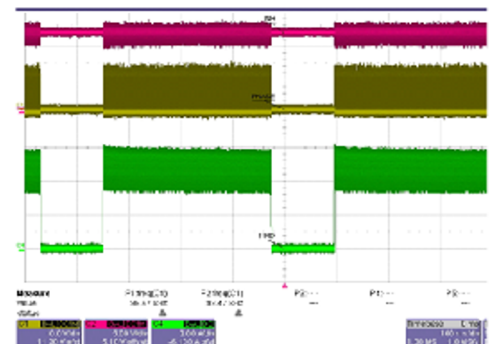


AM12920v1

# 8 Ordering information

**Table 9. Order code**

| Order code | Package | Packing |
|---|---|---|
| LED2001PUR | VFQFPN 4x4 8L | Tape and reel |
| LED2001PHR | HSOP8 | |

# 9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

## 9.1 VFQFPN8 (4x4x1.08 mm) package outline

Figure 32. VFQFPN8 (4x4x1.08 mm) package outline
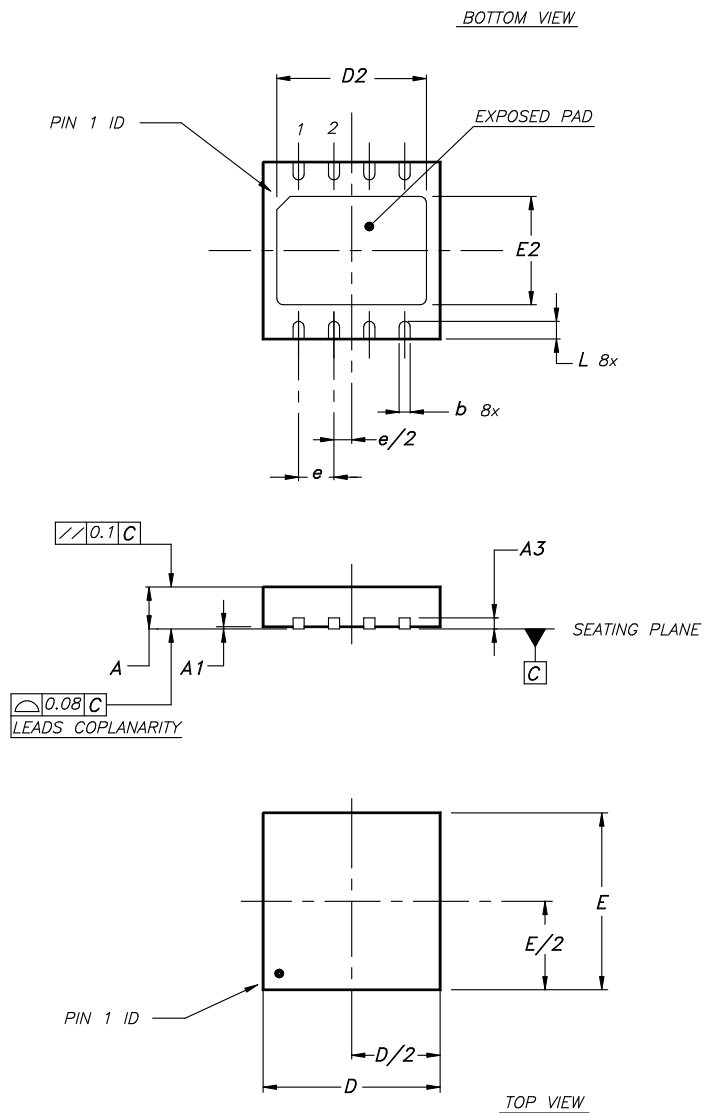
**Table 10. VFQFPN8 (4x4x1.08 mm) package mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.90 | 1 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | | 0.20 | |
| b | 0.23 | 0.30 | 0.38 |
| D | 3.90 | 4 | 4.10 |
| D2 | 2.82 | 3 | 3.23 |
| E | 3.90 | 4 | 4.10 |
| E2 | 2.05 | 2.20 | 2.30 |
| e | | 0.80 | |
| L | 0.40 | 0.50 | 0.60 |

**Figure 33. VFQFPN8 (4x4x1.08 mm) recommended footprint**
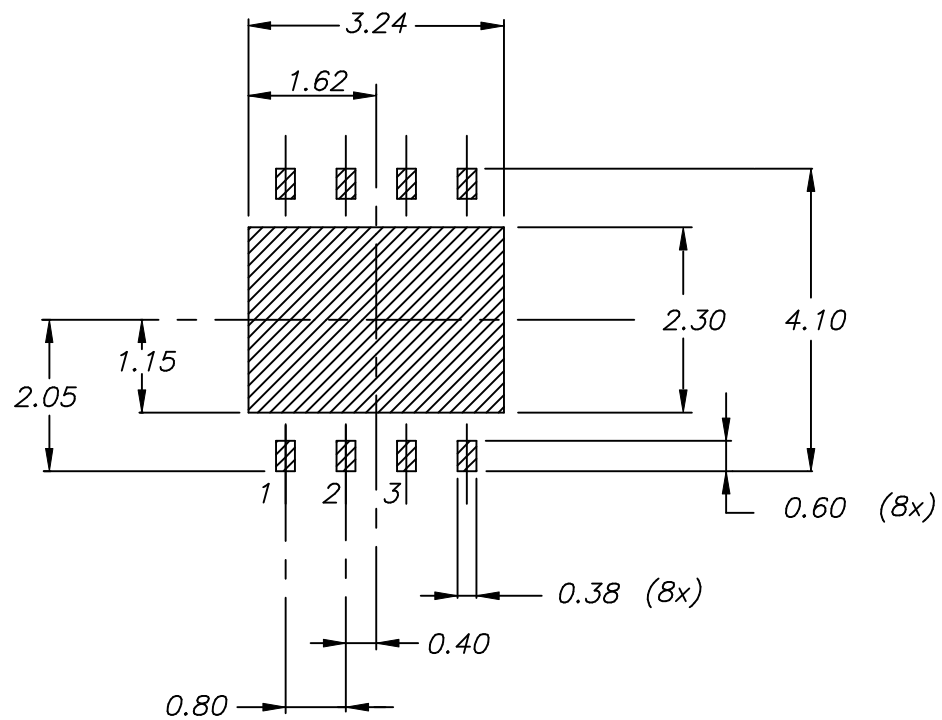
## 9.2 HSOP8 package information

**Figure 34. HSOP8 package outline**
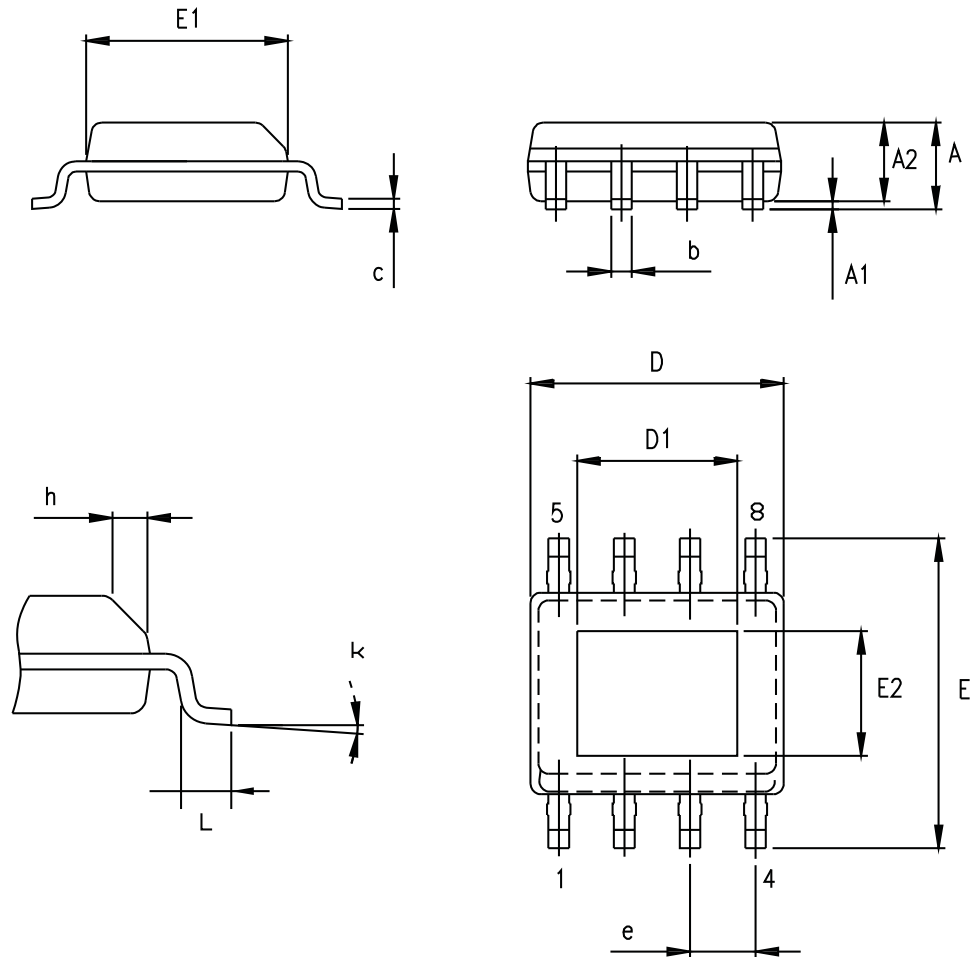


7195016_D

Table 11. **HSOP8 package mechanical data**

| Symbol | Dimensions (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | | | 1.75 |
| A1 | | | 0.15 |
| A2 | 1.25 | | |
| b | 0.38 | | 0.51 |
| c | 0.17 | | 0.25 |
| D | 4.80 | 4.90 | 5.00 |
| D1 | 3.10 | 3.30 | 3.50 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| E2 | 2.20 | 2.40 | 2.60 |
| e | | 1.27 | |
| h | 0.30 | | 0.50 |
| L | 0.45 | | 0.80 |
| k | 0° | | 8° |

# Revision history

**Table 12.** Document revision history

| Date | Revision | Changes |
|---|---|---|
| 20-May-2013 | 1 | Initial release. |
| 11-Jun-2018 | 2 | Updated Section 2.1 Pin connection.<br>Minor modifications throughout document. |

# Contents

# List of figures

# List of tables

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**