NCP781

150 V, 100 mA Very High Voltage Linear Regulator

The NCP781 is a very high−voltage tolerant linear regulator that offers the benefits of thermally enhanced DFN6 3.3 x 3.3 package and is able to withstand continuous DC or transient input voltages up to 150 V. The device is stable with small 0.1 μF Ceramic Output Capacitors which allows smaller PCB design at space constraining applications. The devices features enable pin compatible with standard CMOS logic.

Features

- Wide Input Voltage Range: 6 V to 150 V
- Output Voltage Versions:
  Fixed: 3.3 V, 5 V, 15 V
  Adjustable: from 1.23 V up to 15 V
- ±2.5% Accuracy at Room Temperature
- Very Low Quiescent Current of Typ. 25 μA
- Standby Current: 1 μA
- Stable with a 0.1 μF Ceramic Output Capacitor
- Very High PSRR: 83/56 dB@1/100 kHz
- Thermal Shutdown and Current Limit Protection
- Available in Thermally Enhanced DFN6 3.3 x 3.3, 0.65P Package
- Ideal for Harsh Environments
- These are Pb−free Devices

Typical Applications

- Telecom, Industrial
- Bias Power Supplies, Led Lighting

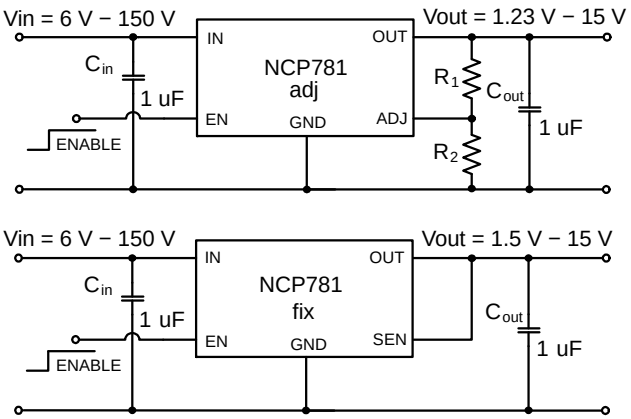

Figure 1. Typical Applications

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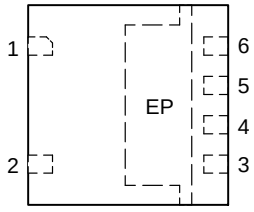
DFN6
S SUFFIX
CASE 506DF

MARKING DIAGRAM

781N = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

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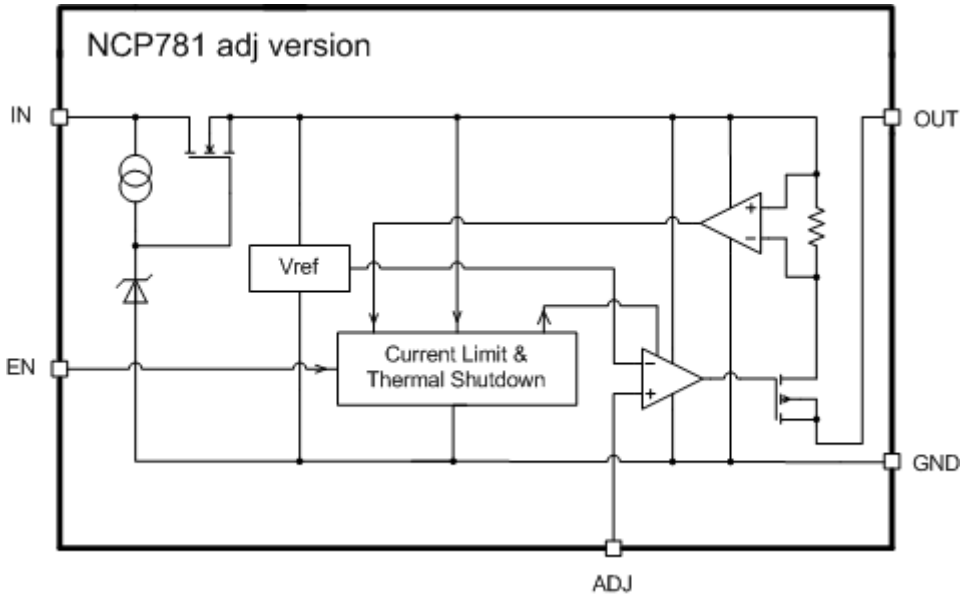


Figure 2. Simplified Block Diagram for Adjustable Version

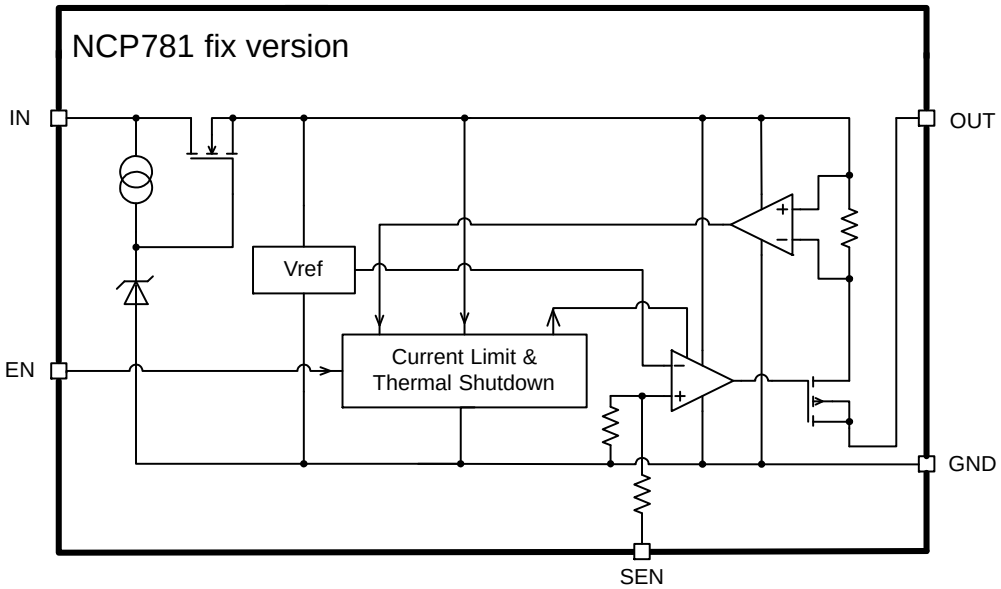


Figure 3. Simplified Block Diagram for Fixed Version

Table 1. PIN FUNCTION DESCRIPTION

Pin No. DFN6 3.3 x 3.3	Pin Name	Description
1	IN	Positive Power Supply Input
2	EN	Chip Enable pin (Active “H”)
3	NC	Not Connected
4	GND	Power Supply Ground
5	OUT	Regulated Output Voltage
6	ADJ/SEN	Output Voltage Adjust Input (Adjustable Version), Sense pin for output voltage sensing, connect to pin 5 (Fixed Voltage Versions)
EP	EP	EP should be connected to GND potential

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{IN}	150	V
Output Voltage Range (Note 2)	V_{OUT}	−0.3 to 20 V	V
Enable Input Range	V_{EN}	−0.3 to (Vin + 0.3) V	V
Adjustable Input Range	V_{ADJ}	−0.3 to 5 V	V
Output Short Circuit Duration	t_{sc}	unlimited	s
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	TSTG	−55 to 150	°C
ESD Capability, Human Body Model (Notes 3, 4)	ESDHBM	2	kV
ESD Charged Device Model ESD (Notes 3, 4)	ESDCDM	750	V
Moisture Sensitivity Level	MSL	1	−
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 5)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTIC and APPLICATION INFORMATION for Safe operating Area
2. The device has limited reverse bias protection. Reverse bias protection feature valid only if (V_{OUT} − V_{IN}) < 7 V.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged−Device Model ESD Capability per JEDEC JSD22−C101E
   Latchup Current Maximum Rating: ≤ 150 mA per JEDEC standard: JESD78
4. Except IN and EN pins.
5. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 2. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, DFN6, 3.3 x 3.3 mm (Note 6) Thermal Resistance, Junction−to−Air (Note 7)	$R_{\theta JA}$	125	°C/W

6. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
7. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 3. ELECTRICAL CHARACTERISTICS − Adjustable −40°C ≤ T_J ≤ 125°C; V_{IN} = Voutnom + 10 V, C_{IN} = C_{OUT} = 1 μF, unless otherwise noted. Typical values are at T_A = +25°C. (Notes 8, 9)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
INPUT REGULATOR						
Operating Input Voltage		V_{IN}	6		150	V
OUTPUT REGULATOR						
Reference Voltage Accuracy	−40°C ≤ T_J ≤125°C, I_{OUT} = 50 μA 6 V ≤ V_{IN} ≤ 150 V		−3%	1.23 V	+3%	%
Reference Voltage Accuracy	T_J = 25°C, I_{OUT} = 50 μA 6 V ≤ V_{IN} ≤ 150 V		−2.5%	1.23 V	+2.5%	%
Line Regulation	15 V ≤ V_{IN} ≤ 150 V I_{OUT} = 50 μA	Reg_{line}		0.25	0.5	%Vout
Load Regulation		Reg_{load}		0.4	0.8	%Vout
Dropout Voltage (Note 10) 3.3 V 5.0 V 12.0 V 15.0 V	V_{DO} = V_{IN} − (V_{OUT} − (3%Voutnom)) I_{OUT} = 100 mA	V_{DO}	 − − − −	 4 4 4.4 4.7	 6.5 7.0 7.5 9.5	V
DISABLE, QUIESCENT AND GROUND CURRENTS						
Disable Current	V_{EN} = 0 V, V_{IN} = 150 V	I_{DIS}	−	1	10	μA
Quiescent Current	I_{OUT} = 0 mA	I_Q	−	25	55	μA
Ground Current	I_{OUT} = 100 mA	I_{GND}	−	250	400	μA
Enable Pin Current	1.5 V < V_{EN} < 150 V	I_{EN}		500		nA
ADJ Pin Current	6 V < V_{IN} < 150 V, ADJ = V_{OUT}	I_{ADJ}		5		nA
CURRENT LIMIT PROTECTION						
Current Limit (Note 11)	V_{OUT} = V_{OUTNOM} − (10% V_{OUTNOM})	I_{LIM}	110			mA
Short Circuit Current Limit	V_{OUT} = 0 V, Vin = 25 V	I_{SC}		220		mA
ENABLE THRESHOLDS						
Enable Input Threshold Voltage Voltage Increasing, Logic High Voltage Decreasing, Logic Low	 High Low	$V_{TH(EN)}$	 1.5 −	 − −	 − 0.4	V
PSRR AND NOISE						
Power Supply Ripple Rejection (Note 12)	V_{IN} = 25 V + 200 mV_{pp} modulation V_{OUT} = 1.23 V, Cout = 1.0 μF I_{OUT} = 10 mA f = 1 kHz f = 10 kHz f = 100 kHz	PSRR	 − − −	 83 75 56	 − − −	dB
Output Noise Voltage (Note 12)	V_{out} = 1.23 V, V_{in} = 150 V I_{OUT} = 1 mA, Cout = 1.0 μF f = 100 Hz to 100 kHz	V_{NOISE}	 −	130	 −	μV_{rms}
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 12)		T_{SD}	−	160	−	°C
Thermal Shutdown Hysteresis (Note 12)		T_{SH}	−	15	−	°C

8. Performance guaranteed over the indicated operating temperature range by design and characterization production tested at Tj = Ta = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
9. I_{OUT} > 50 μA at V_{IN} > 50 V
10. Not characterized at V_{OUTNOM} < 3.3 V.
11. Respect to SOA
12. Guaranteed by design and characterization

Table 4. ELECTRICAL CHARACTERISTICS − 3.3 V −40°C ≤ T_J ≤ 125°C; V_{OUT} = 3.3 V typical, V_{IN} = 13.3 V, C_{IN} = C_{OUT} = 1 μF, unless otherwise noted. Typical values are at T_A = +25°C. (Notes 13, 14)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
INPUT REGULATOR						
Operating Input Voltage		V_{IN}	6		150	V
OUTPUT REGULATOR						
Output Voltage Accuracy	−40°C ≤ T_J ≤ 125°C (V_{OUTNOM} + 10 V) ≤ V_{IN} ≤ 150 V		−3%	3.3	+3%	V
Output Voltage Accuracy	T_J = 25°C, I_{OUT} = 50 μA (V_{OUTNOM} + 10 V) ≤ V_{IN} ≤ 150 V		−2.5%	3.3	+2.5%	V
Line Regulation	15 V ≤ V_{IN} ≤ 150 V I_{OUT} = 50 μA	Reg_{line}		8.3	16.5	mV
Load Regulation (Note 16)	V_{IN} = 13.3 V	Reg_{load}		13.2	26.5	mV
Dropout Voltage (Note 15)	I_{OUT} = 100 mA	V_{DO}		4.0	6.5	V
DISABLE, QUIESCENT AND GROUND CURRENTS						
Disable Current	V_{EN} = 0 V, V_{IN} = 150 V	I_{DIS}	−	1	10	μA
Quiescent Current	I_{OUT} = 0 mA	I_Q	−	27	57	μA
Ground Current	I_{OUT} = 100 mA	I_{GND}	−	250	400	μA
Enable pin current	1.5 V < V_{EN} < 150 V	I_{EN}		500		nA
CURRENT LIMIT PROTECTION						
Current Limit (Note 16)	V_{OUT} = V_{OUTNOM} − (10% V_{OUTNOM})	I_{LIM}	110			mA
Short Circuit Current Limit	V_{OUT} = 0 V, Vin = 25 V	I_{SC}		220		mA
ENABLE THRESHOLDS						
Enable Input Threshold Voltage Voltage Increasing, Logic High Voltage Decreasing, Logic Low	 High Low	$V_{TH(EN)}$	 1.5 −	 − −	 − 0.4	V
PSRR AND NOISE						
Power Supply Ripple Rejection (Note 17)	V_{IN} = 25 V + 200 mV_{pp} modulation V_{OUT} = 3.3 V, C_{OUT} = 1.0 μF I_{OUT} = 10 mA f = 1 kHz f = 10 kHz f = 100 kHz	PSRR	 − − −	 75 62 48	 − − −	dB
Output Noise Voltage (Note 17)	V_{out} = 3.3 V, V_{in} = 150 V I_{OUT} = 1 mA, C_{OUT} = 1.0 μF f = 100 Hz to 100 kHz	V_{NOISE}	 −	260	 −	μV_{rms}
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 17)		T_{SD}	−	160	−	°C
Thermal Shutdown Hysteresis (Note 17)		T_{SH}	−	15	−	°C

13. Performance guaranteed over the indicated operating temperature range by design and characterization production tested at Tj = Ta = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
14. I_{OUT} > 50 μA at V_{IN} > 50 V
15. Characterized when V_{OUT} falls 99 mV below the regulated voltage and only for devices with V_{OUTNOM} = 3.3 V
16. Respect to SOA
17. Guaranteed by design and characterization

Table 5. ELECTRICAL CHARACTERISTICS − 5.0 V −40°C ≤ T_J ≤ 125°C; V_{OUT} = 5.0 V typical, V_{IN} = 15 V, C_{IN} = C_{OUT} = 1 μF, unless otherwise noted. Typical values are at T_A = +25°C. (Notes 18, 19)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
INPUT REGULATOR						
Operating Input Voltage		V_{IN}	6		150	V
OUTPUT REGULATOR						
Output Voltage Accuracy	−40°C ≤ T_J ≤ 125°C (V_{OUTNOM} + 10 V) ≤ V_{IN} ≤ 150 V		−3%	5.0	+3%	V
Output Voltage Accuracy	T_J = 25°C, I_{OUT} = 50 μA (V_{OUTNOM} + 10 V) ≤ V_{IN} ≤ 150 V		−2.5%	5.0	+2.5%	V
Line Regulation	15 V ≤ V_{IN} ≤ 150 V I_{OUT} = 50 μA	Reg_{line}		12.5	25	mV
Load Regulation (Note 21)	V_{IN} = 15 V, 50 μA ≤ I_{OUT} ≤ 100 mA	Reg_{load}		20	40	mV
Dropout Voltage (Note 20)		V_{DO}		4	7.0	V
DISABLE, QUIESCENT AND GROUND CURRENTS						
Disable Current	V_{EN} = 0 V, V_{IN} = 150 V	I_{DIS}	−	1	10	μA
Quiescent Current	I_{OUT} = 0 mA	I_Q	−	27	57	μA
Ground Current	I_{OUT} = 100 mA	I_{GND}	−	250	400	μA
Enable pin current	1.5 V < V_{EN} < 150 V	I_{EN}		500		nA
CURRENT LIMIT PROTECTION						
Current Limit (Note 21)	V_{OUT} = V_{OUTNOM} − (10% V_{OUTNOM})	I_{LIM}	110			mA
Short Circuit Current Limit	V_{OUT} = 0 V, Vin = 25 V	I_{SC}		220		mA
ENABLE THRESHOLDS						
Enable Input Threshold Voltage Voltage Increasing, Logic High Voltage Decreasing, Logic Low	 High Low	$V_{TH(EN)}$	 1.5 −	 − −	 − 0.4	V
PSRR AND NOISE						
Power Supply Ripple Rejection (Note 22)	V_{IN} = 25 V + 200 mV_{pp} modulation V_{OUT} = 5.0 V, C_{OUT} = 1.0 μF I_{OUT} = 10 mA f = 1 kHz f = 10 kHz f = 100 kHz	PSRR	 − − −	 65 56 45	 − − −	dB
Output Noise Voltage (Note 22)	V_{out} = 5.0 V, V_{in} = 150 V I_{OUT} = 1 mA, C_{OUT} = 1.0 μF f = 100 Hz to 100 kHz	V_{NOISE}	 −	300	 −	μV_{rms}
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 22)		T_{SD}	−	160	−	°C
Thermal Shutdown Hysteresis (Note 22)		T_{SH}	−	15	−	°C

18. Performance guaranteed over the indicated operating temperature range by design and characterization production tested at Tj = Ta = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
19. I_{OUT} > 50 μA at V_{IN} > 50 V
20. Characterized when V_{OUT} falls 150 mV below the regulated voltage and only for devices with V_{OUTNOM} = 5.0 V
21. Respect to SOA
22. Guaranteed by design and characterization

Table 6. ELECTRICAL CHARACTERISTICS − 15 V −40°C ≤ T_J ≤ 125°C; V_{OUT} = 15.0 V typical, V_{IN} = 25 V, C_{IN} = C_{OUT} = 1 μF, unless otherwise noted. Typical values are at T_A = +25°C. (Notes 23, 24)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
INPUT REGULATOR						
Operating Input Voltage		V_{IN}	6		150	V
OUTPUT REGULATOR						
Output Voltage Accuracy	−40°C ≤ T_J ≤ 125°C (V_{OUTNOM} + 10 V) ≤ V_{IN} ≤ 150 V		−3%	15.0	+3%	V
Output Voltage Accuracy	T_J = 25°C, I_{OUT} = 50 μA (V_{OUTNOM} + 10 V) ≤ V_{IN} ≤ 150 V		−2.5%	15.0	+2.5%	V
Line Regulation	25 V ≤ V_{IN} ≤ 150 V I_{OUT} = 50 μA	Reg_{line}		37.5	75	mV
Load Regulation (Note 26)	V_{IN} = 25 V, 50 μA ≤ I_{OUT} ≤ 100 mA	Reg_{load}		60	120	mV
Dropout Voltage (Note 25)		V_{DO}		4.7	9.5	V
DISABLE, QUIESCENT AND GROUND CURRENTS						
Disable Current	V_{EN} = 0 V, V_{IN} = 150 V	I_{DIS}	−	1	10	μA
Quiescent Current	I_{OUT} = 0 mA	I_Q	−	27	57	μA
Ground Current	I_{OUT} = 100 mA	I_{GND}	−	250	400	μA
Enable pin current	1.5 V < V_{EN} < 150 V	I_{EN}		500		nA
CURRENT LIMIT PROTECTION						
Current Limit (Note 26)	V_{OUT} = V_{OUTNOM} − (3% V_{OUTNOM})	I_{LIM}	110			mA
Short Circuit Current Limit	V_{OUT} = 0 V, Vin = 25 V	I_{SC}		220		mA
ENABLE THRESHOLDS						
Enable Input Threshold Voltage Voltage Increasing, Logic High Voltage Decreasing, Logic Low	 High Low	$V_{TH(EN)}$	 1.5 −	 − −	 − 0.4	V
PSRR AND NOISE						
Power Supply Ripple Rejection (Note 27)	V_{IN} = 25 V + 200 mV_{pp} modulation V_{OUT} = 15 V, C_{OUT} = 1.0 μF I_{OUT} = 10 mA f = 1 kHz f = 10 kHz f = 100 kHz	PSRR	 − − −	 53 50 43	 − − −	dB
Output Noise Voltage (Note 27)	V_{out} = 15 V, V_{in} = 150 V I_{OUT} = 1 mA, C_{OUT} = 1.0 μF f = 100 Hz to 100 kHz	V_{NOISE}	 −	530	 −	μV_{rms}
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 27)		T_{SD}	−	160	−	°C
Thermal Shutdown Hysteresis (Note 27)		T_{SH}	−	15	−	°C

23. Performance guaranteed over the indicated operating temperature range by design and characterization production tested at Tj = Ta = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
24. I_{OUT} > 50 μA at V_{IN} > 50 V
25. Characterized when V_{OUT} falls 450 mV below the regulated voltage and only for devices with V_{OUTNOM} = 15.0 V
26. Respect to SOA
27. Guaranteed by design and characterization

TYPICAL CHARACTERISTICS

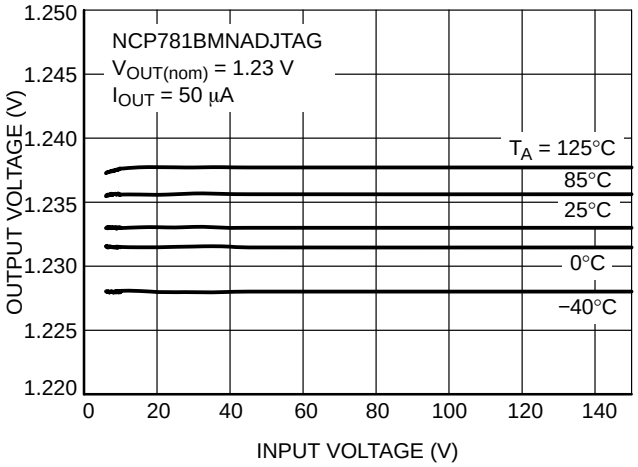


Figure 4. Output Voltage vs. Input Voltage at NCP781BMNADJTAG

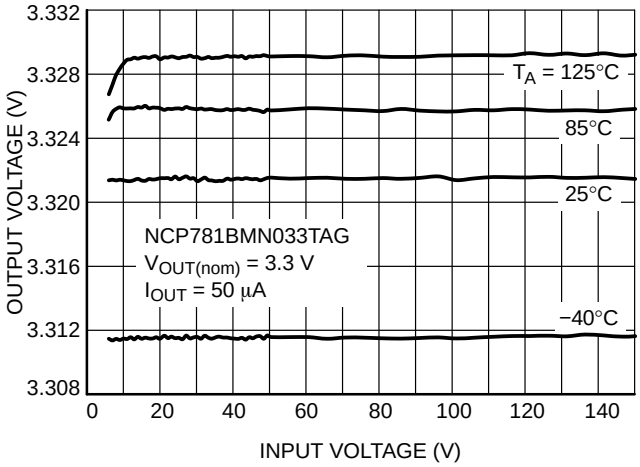


Figure 5. Output Voltage vs. Input Voltage at NCP781BMN033TAG

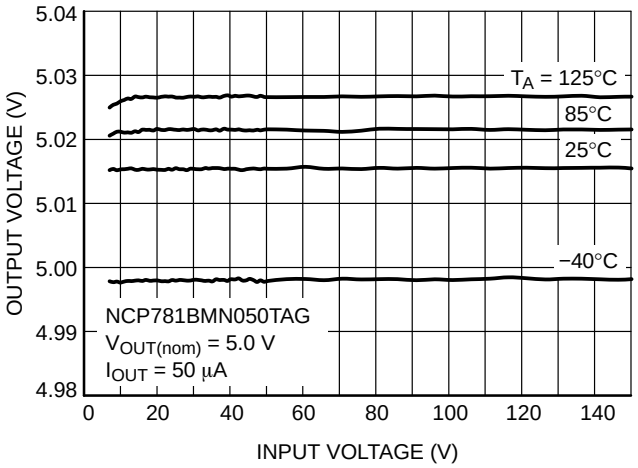


Figure 6. Output Voltage vs. Input Voltage at NCP781BMN050TAG

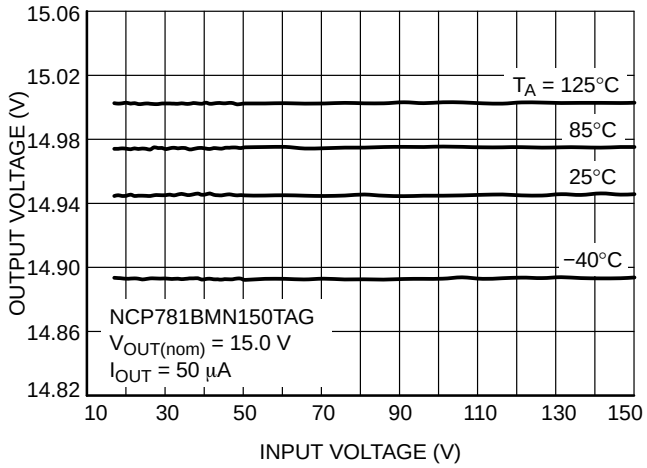


Figure 7. Output Voltage vs. Input Voltage at NCP781BMN150TAG

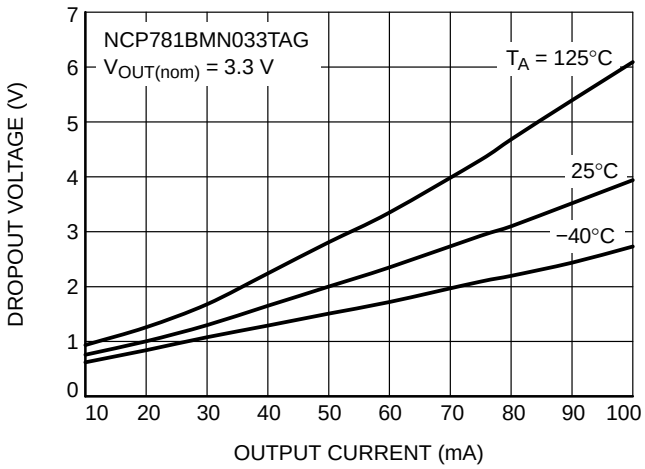


Figure 8. Dropout Voltage vs. Output Current at NCP781BMN033TAG

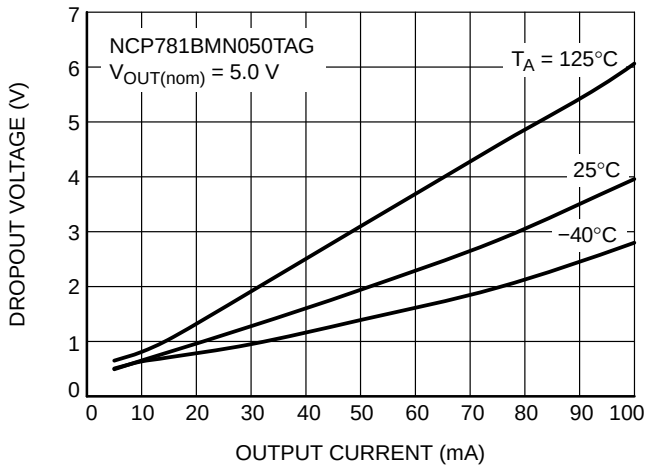


Figure 9. Dropout Voltage vs. Output Current at NCP781BMN050TAG

TYPICAL CHARACTERISTICS

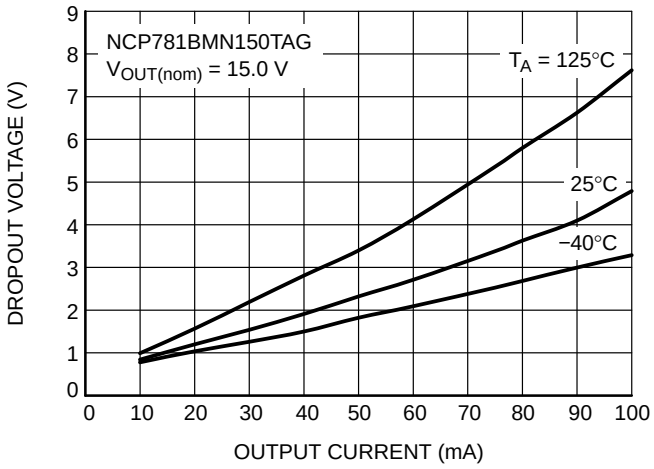


Figure 10. Dropout Voltage vs. Output Current at NCP781BMN150TAG

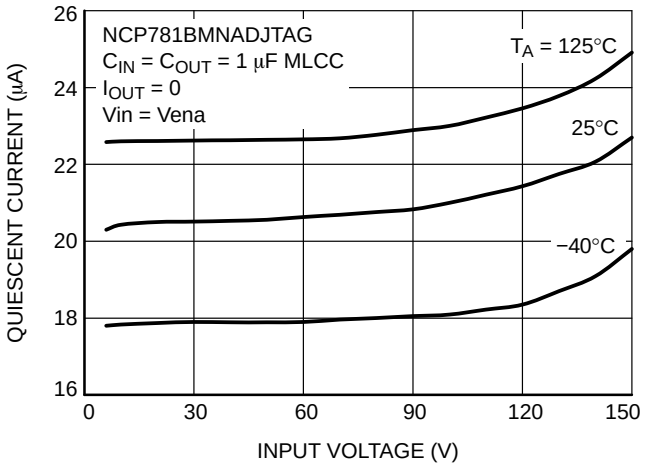


Figure 11. Quiescent Current vs. Input Voltage at NCP781BMNADJTAG

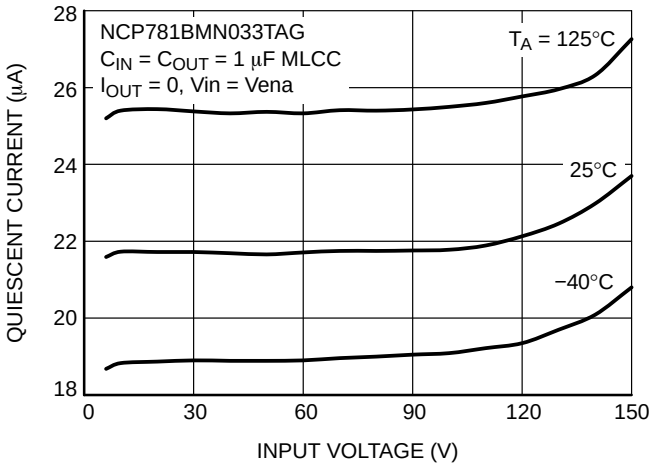


Figure 12. Quiescent Current vs. Input Voltage at NCP781BMN033TAG

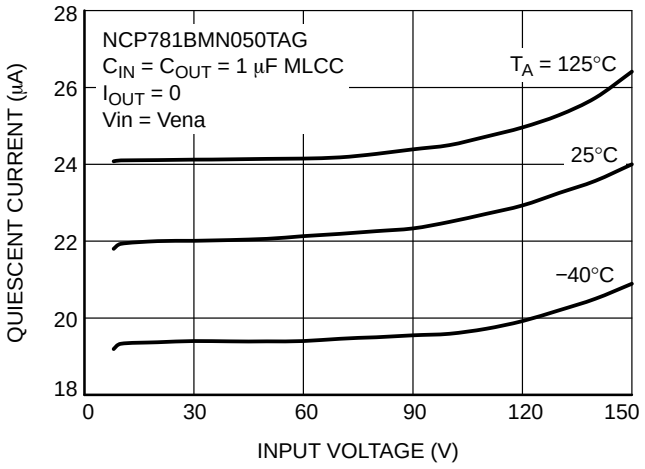


Figure 13. Quiescent Current vs. Input Voltage at NCP781BMN050TAG

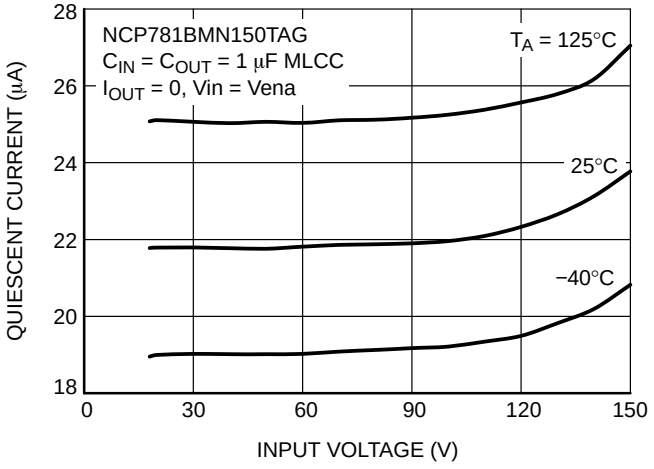


Figure 14. Quiescent Current vs. Input Voltage at NCP781BMN150TAG

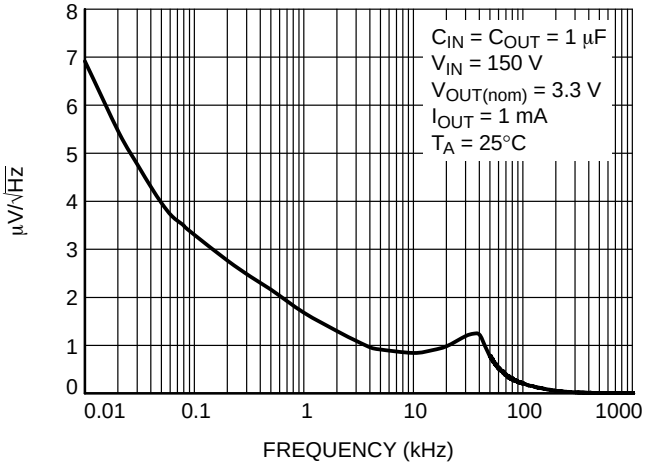


Figure 15. Output Voltage Noise Spectral Density at NCP781BMN033TAG

TYPICAL CHARACTERISTICS

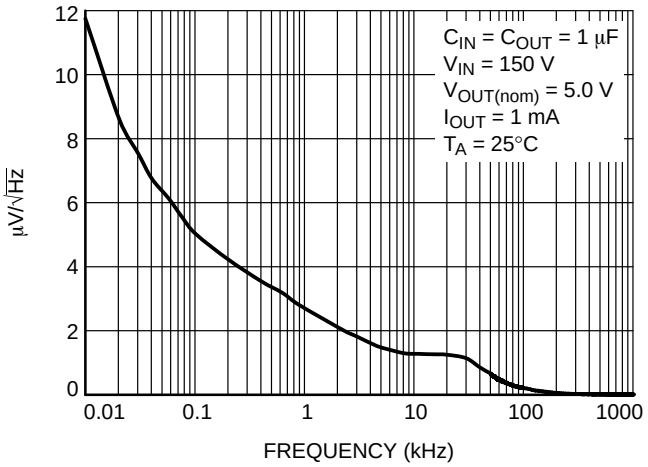


Figure 16. Output Voltage Noise Spectral Density at NCP781BMN050TAG

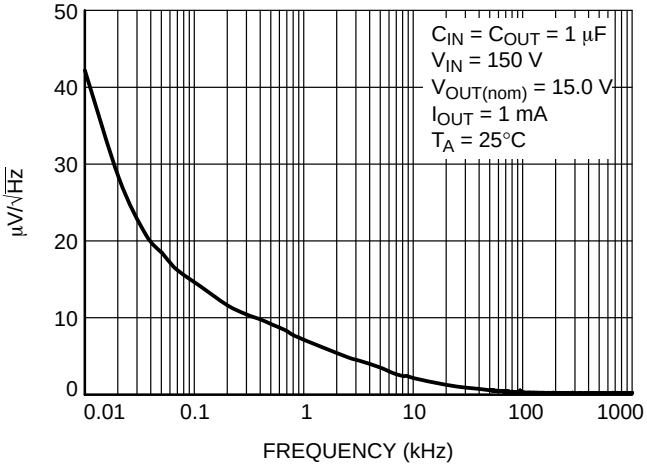


Figure 17. Output Voltage Noise Spectral Density at NCP781BMN150TAG

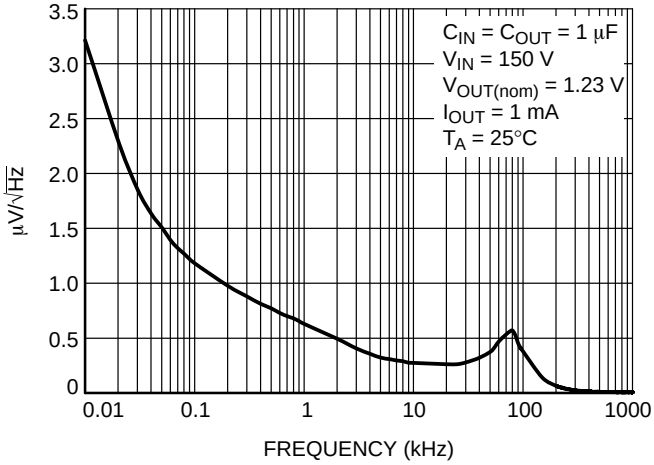


Figure 18. Output Voltage Noise Spectral Density at NCP781BMNADJTAG

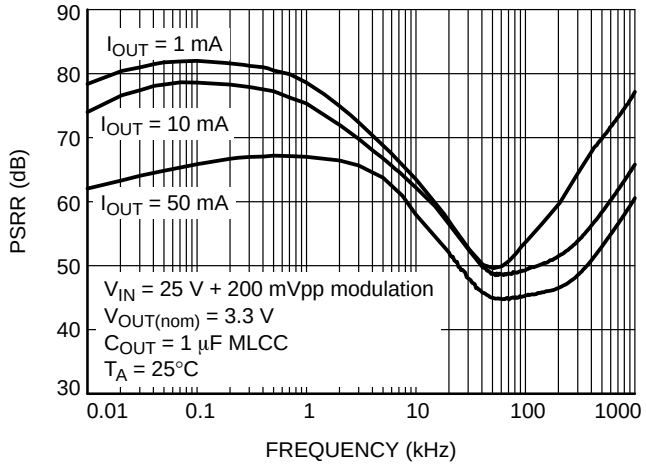


Figure 19. PSRR vs. Frequency at NCP781BMN033TAG

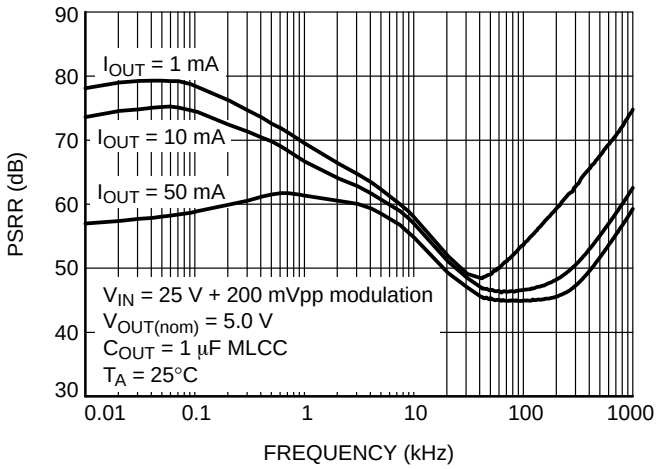


Figure 20. PSRR vs. Frequency at NCP781BMN050TAG

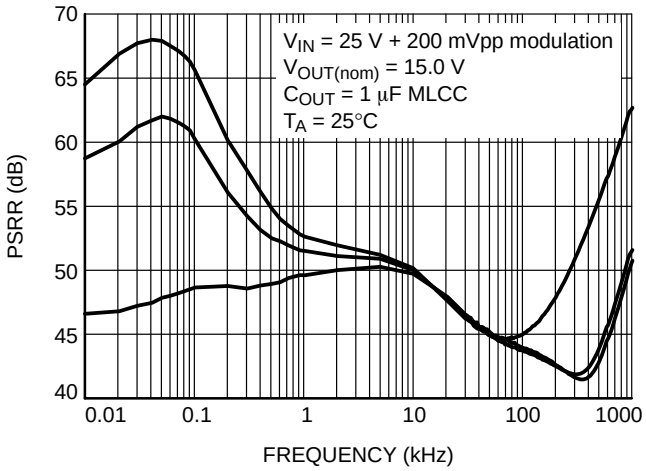


Figure 21. PSRR vs. Frequency at NCP781BMN150TAG

TYPICAL CHARACTERISTICS

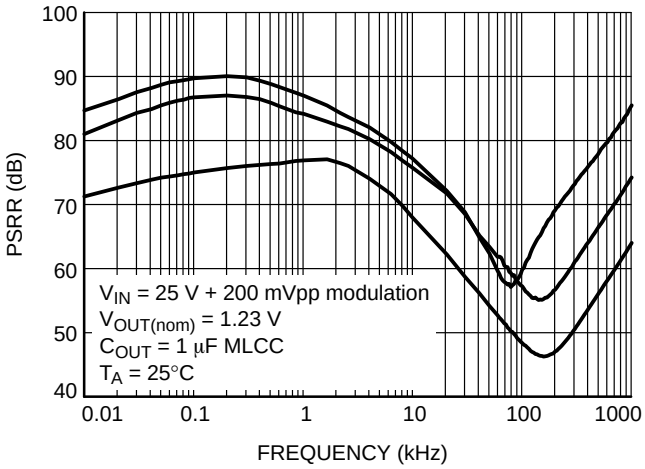


Figure 22. PSRR vs. Frequency at NCP781BMNADJTAG

APPLICATIONS INFORMATION

The NCP781 is very high input voltage regulator with internal thermal shutdown and internal current limit. Typical application circuits are shown in Figure 23.

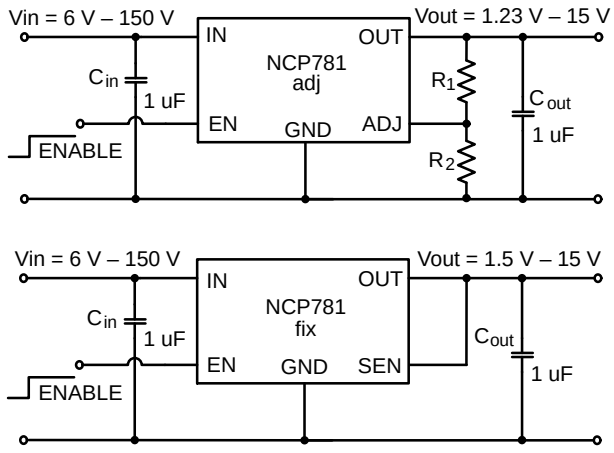


Figure 23. Typical Application Circuits

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCP781 package. Higher capacitance and lower ESR will improve the overall line and load transient response.

Output Decoupling (C_{out})

The NCP781 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The minimum output decoupling value is 0.1 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices up to 10 μF. The larger values improve noise rejection, load regulation and transient response.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. The turn−on/turn−off transient voltage being supplied to the enable pin should exceed a slew rate of 150 mV/μs to ensure correct operation. If the enable function is not to be used then the pin should be connected directly to V_{in}.

Output Voltage Adjust

The output voltage can be adjusted from 1.23 V to 15 V using resistors between the output and the ADJ input. The output voltage and resistors are chosen using Equation 1 and Equation 2.

$$V_{OUT} = 1.23 \times \left(1 + \frac{R_1}{R_2}\right) + \left(I_{ADJ} \times R_1\right) \quad \text{(eq. 1)}$$

$$R_2 \cong R_1 \times \frac{1}{\frac{V_{OUT}}{1.25} - 1} \quad \text{(eq. 2)}$$

Input bias current I_{ADJ} is typically less than 5 nA. Choose R1 arbitrarily to minimize errors due to the bias current and to minimize noise contribution to the output voltage. Use Equation 2 to find the required value for R2. This device does not require a minimal load.

Thermal Considerations

As power in the NCP781 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCP781 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCP781 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 3)}$$

The power dissipated by the NCP781 can be calculated from the following equations:

$$P_D \approx V_{in} \times \left(I_{GND} @ I_{OUT}\right) + I_{OUT} \times \left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 4)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{OUT} \times I_{OUT}\right)}{I_{OUT} + I_{GND}} \quad \text{(eq. 5)}$$

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCP781, and make traces as short as possible.

ORDERING INFORMATION

Part No.	Output Voltage (V)	Marking	Package	Shipping†
NCP781BMNADJTAG	Adj	781N BADJ	DFN6 (Pb−Free)	3000 / Tape & Reel (Contact sales office for availability)
NCP781BMN033TAG	3.3	781N B033		
NCP781BMN050TAG	5	781N B050		
NCP781BMN150TAG	15	781N B150		

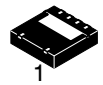
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

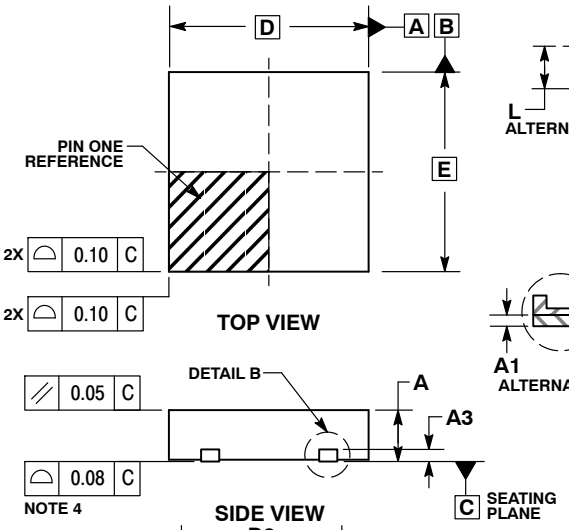
ON Semiconductor®

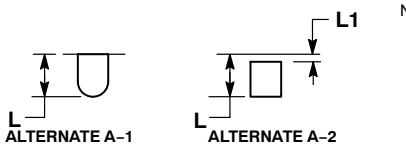
DFN6 3.3x3.3, 0.65P
CASE 506DF
ISSUE B

DATE 23 JUN 2016

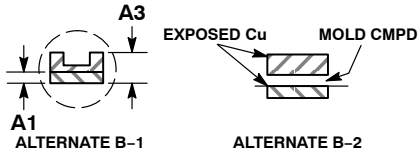


SCALE 2:1

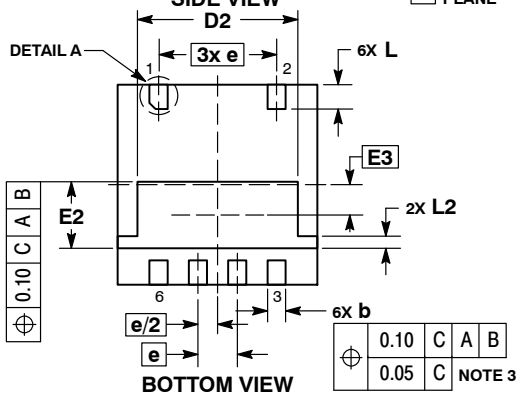




DETAIL A
ALTERNATE CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP..
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A ALTERNATE CONSTRUCTION A–2 AND DETAIL B ALTERNATE CONSTRUCTION B–2 ARE NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	0.90
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	3.30 BSC	
D2	2.55	2.75
E	3.30 BSC	
E2	1.00	1.20
E3	0.50 BSC	
e	0.65 BSC	
L	0.35	0.45
L1	0.00	0.15
L2	0.20 REF	

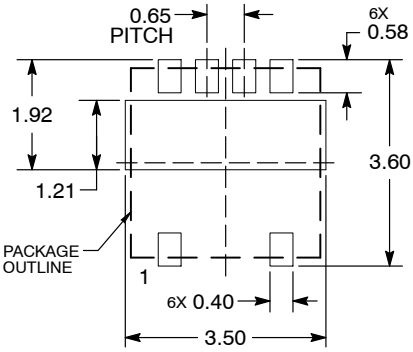
GENERIC MARKING DIAGRAM*

A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFN6 3.3X3.3, 0.65P**	**PAGE 1 OF 1**

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