MIGRATION FROM W29N01GV TO W29N01HV
1G-BIT 3.3V
NAND FLASH MEMORY

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Table of Contents

1. INTRODUCTION

This application note details how to migrate designs from Winbond W29N01GV (1G-bit) NAND Flash memory to W29N01HV (1G-bit) NAND Flash memory.

The memory array totals 138,412,032 bytes, and organized into 1,024 erasable blocks of 135,168 bytes. Each block consists of 64 programmable pages of 2,112-bytes each. Each page consists of 2,048-bytes for the main data storage area and 64-bytes for the spare data area (The spare area is typically used for error management functions).

The W29N01HV supports the standard NAND flash memory interface using the multiplexed 8-bit bus to transfer data, addresses, and command instructions. The five control signals, CLE, ALE, #CE, #RE and #WE handle the bus interface protocol. Also, the device has two other signal pins, the #WP (Write Protect) and the RY/#BY (Ready/Busy) for monitoring the device status.

Note: All the information provided in this guide illustrates only the differences for each section. Please refer to the respective data sheets for more information.

2. FEATURES COMPARISON

Most of the features between W29N01GV and W29N01HV are the same, except a few differences that are highlight in Table 2.1. Refer to the respective W29N01GV and W29N01HV data sheets to verify any other features.

Table 2.1 Feature Difference

Command Set	W29N01GV	W29N01HV
Standard NAND command set	V	V
Sequential Cache Read	V	
Random Cache Read	V	
Cache Program	V	
Copy Back	V	V
OTP Data Program/Read/Lock	V	

3. DC ELECTRICAL CHARACTERISTICS – NO DIFFERENCE

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	

Sequential Read current	Icc1	tRC= tRC MIN
		#CE=VIL
		IOUT=0mA
			-	25	35	mA

Program current	Icc2	-	-	25	35	mA
Erase current	Icc3	-	-	25	35	mA
Standby current (TTL)	I_{SB1}	#CE=VIH #WP=0V/Vcc	-	-	1	mA
Standby current (CMOS)	I_{SB2}	#CE=Vcc – 0.2V #WP=0V/Vcc	-	10	50	µA
Input leakage current	I_{LI}	V_{IN}= 0 V to Vcc	-	-	±10	µA
Output leakage current	I_{LO}	V_{OUT}=0V to Vcc	-	-	±10	µA
Input high voltage	V_{IH}	I/O7~0, #CE,#WE,#RE, #WP,CLE,ALE	0.8 x Vcc	-	Vcc + 0.3	V
Input low voltage	V_{IL}	-	-0.3	-	0.2 x Vcc	V
Output high voltage(1)	V_{OH}	I_{OH}=-400µA	2.4	-	-	V
Output low voltage(1)	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
Output low current(2)	$I_{OL(RY/\#BY)}$	V_{OL}=0.4V	8	10		mA

Table 3.1 DC Electrical Characteristics

Note:

1. **VOH and VOL may need to be relaxed if I/O drive strength is not set to full.**
2. **IOL (RY/#BY) may need to be relaxed if RY/#BY pull-down strength is not set to full**

4. AC TIMING CHARACTERISTICS FOR OPERATION – NO DIFFERENCE

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
ALE to #RE Delay	tAR	10	-	ns
#CE Access Time	tCEA	-	25	ns
#CE HIGH to Output High-Z(1)	tCHZ	-	30	ns
CLE to #RE Delay	tCLR	10	-	ns
#CE HIGH to Output Hold	tCOH	15	-	ns
Output High-Z to #RE LOW	tIR	0	-	ns
Data Transfer from Cell to Data Register	tR	-	25	µs
READ Cycle Time	tRC	25	-	ns
#RE Access Time	tREA	-	20	ns
#RE HIGH Hold Time	tREH	10	-	ns
#RE HIGH to Output Hold	tRHOH	15	-	ns
#RE HIGH to #WE LOW	tRHW	100	-	ns
#RE HIGH to Output High-Z(1)	tRHZ	-	100	ns
#RE LOW to output hold	tRLOH	5	-	ns
#RE Pulse Width	tRP	12	-	ns
Ready to #RE LOW	tRR	20	-	ns
Reset Time (READ/PROGRAM/ERASE)(2)	tRST	-	5/10/500	µs
#WE HIGH to Busy(3)	tWB	-	100	ns
#WE HIGH to #RE LOW	tWHR	60	-	ns

Table 4.1 AC timing characteristics for Operation

Notes:

1. **Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 % tested.**
2. **The RESET (FFh) command is issued while the device is idle, the device goes busy for a maximum of 5us.**
3. **Do not issue new command during tWB, even if RY/#BY is ready.**

5. PROGRAM AND ERASE CHARACTERISTICS – NO DIFFERENCE

PARAMETER	SYMBOL	SPEC		UNIT
		TYP	MAX	
Number of partial page programs	NoP	-	4	cycles
Page Program time	tPROG	250	700	µs
Block Erase Time	tBERS	2	10	ms

Table 5.1 Program and Erase Characteristics

6. DEVICE ID

# of Byte/Cycles	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle	5th Byte/Cycle
W29N01GV	EFh	F1h	80h	95h	00h
W29N01HV	EFh	F1h	00h	95h	00h
Description	MFR ID	Device ID	Cache Programming supporting ID	Page Size:2KB Spare Area Size:64b BLK Size w/o Spare:128KB Organized:x8 or x16 Serial Access:25ns	

7. PART NUMBER COMPARISON

W29N01GV	W29N01HV
W29N01GVSIAA	W29N01HVSIAA
W29N01GVBIAA	W29N01HVBIAA
W29N01GVDIAA	W29N01HVDIAA

8. SUMMARY

The difference between W29N01GV (1G-bit) NAND Flash memory and W29N01HV (1G-bit) NAND Flash memory is the features innovation and its respective device ID. All other standard ONFI command set and AC/DC are the same with each other. Customers can easily migrate from W29N01GV to W29N01HV.

9. COMPARISON TABLE

Green line is "Mandatory spec" by ONFi

Outline					
	Maker			Winbond	Winbond
	P/N			W29N01GV	W29N01HV
	Density			1Gbit	1Gb
	Vcc			2.7-3.6V	2.7-3.6V
	Org.			x8	x8
	Memory Cell			SLC	SLC
Command sets					
	Read	1st set		00h	00h
		2nd set		30h	30h
	Read for Copy back	1st set		00h	00h
		2nd set		35h	35h
	Cache Read sequential	1st set		31h	-
		2nd set		-	-
	Cache Read random	1st set		00h	-
		2nd set		31h	-
	Cache read Last address	1st set		3Fh	-
		2nd set		-	-
	Read ID	1st set		90h	90h
		2nd set		-	-
	Reset	1st set		FFh	FFh
		2nd set		-	-
	Page Program	1st set		80h	80h
		2nd set		10h	10h
	Cache Program	1st set		80h	-
		2nd set		15h	-
	Copy-back Program	1st set		85h	85h
		2nd set		10h	10h
	Block erase	1st set		60h	60h
		2nd set		D0h	D0h
	Random Data Input	1st set		85h	85h
		2nd set		-	-
	Random Data output	1st set		05h	05h
		2nd set		E0h	E0h
	Read status	1st set		70h	70h
		2nd set		-	-

ONFI v1	Read Unique ID	1st set		EDh	-
		2nd set		--	-
	Read parameter page	1st set		ECh	ECh
		2nd set		--	-
	Set features	1st set		EFh	-
		2nd set		--	-
	Get features	1st set		EEh	-
		2nd set		--	-
Legacy OTP	**OTP DATA PRG**	1st set		A0h	-
		2nd set		10h	-
	OTP DATA PROTECT	1st set		A5h	-
		2nd set		10h	-
	OTP DATA READ	1st set		AFh	-
		2nd set		30h	-
AC spec		Value			
	tR	Max	Data transfer from Cell to array	25 us	25 us
	tAR	Min	ALE to #RE delay	10 ns	10 ns
	tCLR	Min	CLE to #RE delay	10 ns	10 ns
	tRR	Min	Ready to #RE low	20 ns	20 ns
	tRP	Min	#RE pulse width	12 ns	12 ns
	tWB	Max	#WE high to Busy	100 ns	100 ns
	tWW	Min	#WP high to #WE low	100 ns	100 ns
	tRC	Min	Read cycle time	25 ns	25 ns
	tREA	Max	#RE access time	20 ns	20 ns
	tCEA	Max	#CE access time	25 ns	25 ns
	tRHZ	Max	#RE high to output hi-z	100 ns	100 ns
	tCHZ	Max	#CE high to output Hi-z	30 ns	30 ns
	tRHOH	Min	#RE high to output hold	15 ns	15 ns
	tRLOH	Min	#RE low to output hold	5ns	5 ns
	tCOH	Min	#CE high to output hold	15 ns	15 ns
	tREH	Min	#RE high hold time	10 ns	10 ns
	tIR	Min	Output hi-z to #RE low	0 ns	0 ns
	tRHW	Min	#RE high to #WE low	100 ns	100 ns
	tWHR	Min	#WE high to #RE low	60 ns	60 ns
	tRST (R/P/E)	Max	device resetting time	5/10/500 us	5/10/500 us
	tRCBSY (tDCBSYR1)	Max(typ)	Data cache busy in read (1st 31h)	25 us/3 us	-
	tDCBSYR 2	Max	Data cache busy in read (next 31h and 3Fh)	25 us	-

	tPROG	Max (typ)	program time	0.7 (0.25) ms	0.7 (0.25) ms
	tCBSY	Max	Dummy busy time for cache program	700 (3) us	-
	Nop	Max	Number of Partial program cycles in the same page	4 cycles	4 cycles
	tBERS	Max (typ)	Block erase time	10 (2) ms	10 (2) ms
	tCLS	Min	CLE setup time	10 ns	10 ns
	tCLH	Min	CLE Hold time	5 ns	5 ns
	tCS	Min	#CE setup time	15 ns	15 ns
	tCH	Min	#CE hold time	5 ns	5 ns
	tWP	Min	#WE pulse width	12 ns	12 ns
	tALS	Min	ALE setup time	10 ns	10 ns
	tALH	Min	ALE hold time	5 ns	5 ns
	tDS	Min	Data setup time	10 ns	10 ns
	tDH	Min	Data hold time	5 ns	5 ns
	tWC	Min	Write cycle time	25 ns	25 ns
	tWH	Min	#WE high hold time	10 ns	10 ns
	tADL	Min	Address to Data loading time	70 ns	70 ns
ONFI	tFEAT	Max	Busy time for SET/GET Features ope.	1 us	-
	tLBSY	Max	Busy time for PRG/ERS on locked blk	3 us	-
	tOBSY	Max	Busy time for OTP data prg ope. If protected	30 us	-
DC spec		Value			
	Icc1	Max (typ)	Page read with serial access	35 (25) mA	35 (25) mA
	Icc2	Max (typ)	Program operating current	35 (25) mA	35 (25) mA
	Icc3	Max (typ)	Erase operating current	35 (25) mA	35 (25) mA
	Isb (CMOS)	Max (typ)	standby current (CMOS)	50 (10) uA	50 (10) uA
	ILI	Max	Input leakage current	+ - 10 uA	+ - 10 uA
	ILO	Max	Output leakage current	+ - 10 uA	+ - 10 uA
	VIH	Min to Max	Input high voltage	0.8*Vcc to Vcc+0.3	0.8*Vcc to Vcc+0.3
	VIL	Min to Max	Input low voltage	-0.3 to 0.2*Vcc	-0.3 to 0.2*Vcc
	VOH	Min	output high voltage level	2.4V	2.4V
	VOL	Max	output low voltage level	0.4V	0.4V
	IOL	Min (typ)	output low current	8 (10) mA	8 (10) mA
Valid block		Value			
		Min/blocks		1004	1004
		Max/blocks		1024	1024
	Max invalid block ratio			2%	2%

Other specs				
	On chip ECC		NONE	NONE
	POR method (busy period)		Reset cmd	Auto
	Random page programming		Prohibit	Prohibit

10. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
1.0	01/07/2016		Initial Version
2.0	03/22/2016	6~9	Add comparison table
3.0	03/25/2016	6	Add Part No. Table