

DSP56301

24-Bit Digital Signal Processor

The DSP56301 is a member of the DSP56300 core family of programmable CMOS DSPs. This family uses a high-performance, single clock cycle per instruction engine. Significant architectural features of the DSP56300 core family include a barrel shifter, 24-bit addressing, instruction cache, and DMA. The DSP56301 performs at 66/80/100 MIPS using an internal 66/80/100 MHz clock at 3.0–3.6 volts. The DSP56300 core family offers a rich instruction set and low power dissipation, as well as increasing levels of speed and power, enabling wireless, telecommunications, and multimedia products.

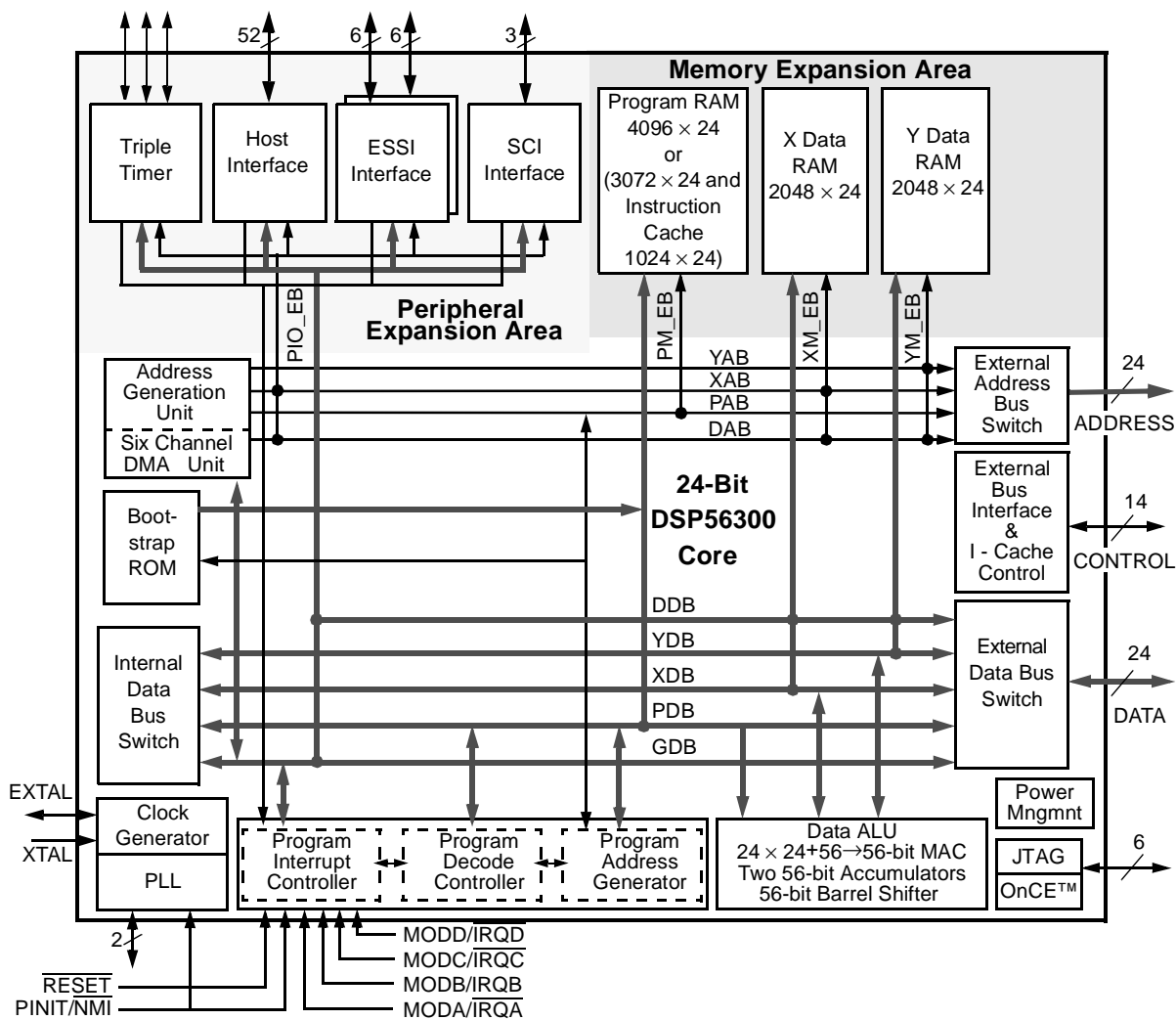


Figure 1. DSP56301 Block Diagram

DSP56301 Features

- High-performance DSP56300 core
 - 66/80/100 Million Instructions Per Second (MIPS) with a 66/80/100 MHz clock at 3.3 V
 - Object code compatible with the DSP56000 core
 - Highly parallel instruction set
 - Fully pipelined 24 x 24-bit parallel multiplier-accumulator
 - 56-bit parallel barrel shifter
 - 24-bit or 16-bit arithmetic support under software control
 - Position independent code support
 - Addressing modes optimized for DSP applications
 - On-chip instruction cache controller
 - On-chip memory-expandable hardware stack
 - Nested hardware DO loops
 - Fast auto-return interrupts
 - On-chip concurrent six-channel DMA controller
 - On-chip Phase Lock Loop (PLL) and clock generator
 - On-Chip Emulation (OnCE™) module
 - Joint Action Test Group (JTAG) Test Access Port (TAP)
 - Address tracing mode that reflects internal accesses at the external port

- On-chip memories

- Program RAM, Instruction Cache, X data RAM, and Y data RAM size are programmable:

| Instruction Cache | Switch Mode | Program RAM Size | Instruction Cache Size | X Data RAM Size | Y Data Ram Size |
|-------------------|-------------|------------------|------------------------|-----------------|-----------------|
| disabled | disabled | 4096 × 24-bit | 0 | 2048 × 24-bit | 2048 × 24-bit |
| enabled | disabled | 3072 × 24-bit | 1024 × 24-bit | 2048 × 24-bit | 2048 × 24-bit |
| disabled | enabled | 2048 × 24-bit | 0 | 3072 × 24-bit | 3072 × 24-bit |
| enabled | enabled | 1024 × 24-bit | 1024 × 24-bit | 3072 × 24-bit | 3072 × 24-bit |

- 192 × 24-bit bootstrap ROM
- Off-chip memory expansion
 - Data memory expansion to two 16 M x 24-bit word memory spaces
 - Program memory expansion to one 16 M x 24-bit word memory space
 - External memory expansion port
 - Chip Select Logic requiring no additional circuitry to interface to SRAMs and SSRAMs
 - On-chip DRAM controller that requires no additional circuitry to interface to DRAMs
- On-chip peripherals
 - 32-bit parallel PCI/Universal Host Interface (HI32), PCI Rev. 2.1 compliant with no additional interface logic required for other DSP563xx buses
 - ISA interface requires only 74LS45-style buffer
 - Two Enhanced Synchronous Serial Interfaces (ESSI)
 - Serial Communications Interface (SCI) with baud rate generator
 - Triple timer module
 - Up to 42 programmable General Purpose I/O pins (GPIO), depending on which peripherals are enabled
- Reduced power dissipation
 - Very low power CMOS design
 - Wait and Stop low power standby modes
 - Fully-static logic, operation frequency down to 0 Hz (DC)
 - Optimized power management circuitry

Target Applications

The DSP56301 is intended as for general-purpose digital signal processing, particularly in multimedia and telecommunication applications, such as videoconferencing and cellular telephony.

Product Documentation

The documents listed in **Table 1** are required for a complete description of the DSP56301 and are necessary to design with the part properly. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, a Freescale Literature Distribution Center, or the Freescale web site listed on the back cover of this document.

Table 1. DSP56301 Documentation

| Topic | Description | Order Number |
|-------------------------|--|--------------|
| DSP56300 Family Manual | Detailed description of the DSP56300 family architecture and the 24-bit core processor and instruction set | DSP56300FM |
| DSP56301 User's Manual | Detailed description of DSP56301 memory, peripherals, and interfaces | DSP56301UM |
| DSP56301 Technical Data | DSP56301 pin and package descriptions; electrical and timing specifications | DSP56301 |

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