Keywords: design migration, MCM, multichip module

APPLICATION NOTE 396

Design Migration from DS21Q55 to DS21Q50 or DS21Q59

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Abstract: The DS21Q55 is a quad multichip module (MCM) device featuring independent transceivers that can be software configured for T1, E1, or J1 operation. Each is composed of a line interface unit (LIU), framer, HDLC controllers, and a TDM backplane interface, and is controlled via an 8-bit parallel port configured for Intel or Motorola bus operations. The DS21Q55 is software compatible with the DS2155 single transceiver and is pin compatible with the DS21Qx5y family of products. The DS21Q59 E1 quad transceiver contains all of the necessary functions for connection to four E1 lines. The DS21Q59 is a direct replacement for the DS21Q50 with the addition of signaling access and improved interrupt handling. Both are composed of a LIU, framer, and a TDM backplane interface, and are controlled via an 8-bit parallel port configured for Intel or Motorola bus operations or serial port operation.

Pin Similarities and Disimilarities Among DS21Q55, DS21Q50, and DS21Q59

The following table shows the pins that are available on DS21Q55, DS21Q50, and DS21Q59.

NAME	TYPE	FUNCTION	DS21Q55	DS21Q50/59
4/8/16MCK	O	4.096MHz, 8.192MHz, or 16.384 MHz Clock		X
A0-A4	I	Address Bus Bit 0 (LSB) to Address Bus Bit 4	X	X
A5/ALE(AS)	I	Address Bus Bit 5 (MSB)/Address Latch Enable		X
A5, A6	I	Address Bus Bit 5 to Address Bus Bit 6	X	
A7/ALE(AS)	I	Address Bus Bit 7 (MSB)/Address Latch Enable	X	
AJACKI	I	Alternate Jitter Attenuator Clock Input		X
AJACKO	O	Alternate Jitter Attenuator Clock Output		X
BPCLK1	O	Back Plane Clock, Transceiver 1	X	
BPCLK2	O	Back Plane Clock, Transceiver 2	X	
BPCLK3	O	Back Plane Clock, Transceiver 3	X	
BPCLK4	O	Back Plane Clock, Transceiver 4	X	
BTS0	I	Bus Type Select 0		X
BTS1	I	Bus Type Select		X

BTS	I	Bus Type Select (0 = Intel® / 1 = Motorola®)	**X**	
CS	I	Chip Select		**X**
CS1	I	Chip Select, Transceiver 1	**X**	
CS2	I	Chip Select, Transceiver 2	**X**	
CS3	I	Chip Select, Transceiver 3	**X**	
CS4	I	Chip Select, Transceiver 4	**X**	
D0/AD0-	I/O	Data Bus Bit 0/Address/Data Bus Bit 0 (LSB) to Data	**X**	**X**
D7/AD7		Bus Bit 7/Address/Data Bus Bit 7 (MSB)		
DVDD1	--	Digital Positive Supply	**X** (Note 1)	**X**
DVDD2	--	Digital Positive Supply	**X** (Note 1)	**X**
DVDD3	--	Digital Positive Supply	**X** (Note 1)	**X**
DVDD4	--	Digital Positive Supply	**X** (Note 1)	**X**
DVSS1	--	Digital Signal Ground	**X** (Note 2)	**X**
DVSS2	--	Digital Signal Ground	**X** (Note 2)	**X**
DVSS3	--	Digital Signal Ground	**X** (Note 2)	**X**
DVSS4	--	Digital Signal Ground	**X** (Note 2)	**X**
ESIBRD1	--	Extended System Information Bus Read, Transceiver 1	**X**	
ESIBRD2	--	Extended System Information Bus Read, Transceiver 2	**X**	
ESIBRD3	--	Extended System Information Bus Read, Transceiver 3	**X**	
ESIBRD4	--	Extended System Information Bus Read, Transceiver 4	**X**	
ESIBS0_1	I/O	Extended System Information Bus 0, Transceiver 1	**X**	
ESIBS0_2	I/O	Extended System Information Bus 0, Transceiver 2	**X**	
ESIBS0_3	I/O	Extended System Information Bus 0, Transceiver 3	**X**	
ESIBS0_4	I/O	Extended System Information Bus 0, Transceiver 4	**X**	
ESIBS1_1	I/O	Extended System Information Bus 1, Transceiver 1	**X**	
ESIBS1_2	I/O	Extended System Information Bus 1, Transceiver 2	**X**	
ESIBS1_3	I/O	Extended System Information Bus 1, Transceiver 3	**X**	
ESIBS1_4	I/O	Extended System Information Bus 1, Transceiver 4	**X**	
INT	O	Interrupt	**X**	**X**
JTCLK	I	JTAG Clock	**X**	
JTDI	I	JTAG Data Input, Transceiver 1	**X**	
JTDO	O	JTAG Data Output, Transceiver 4	**X**	
JTMS	I	JTAG Test Mode Select	**X**	
JTRST	I	JTAG Reset	**X**	
LIUC	I	Line Interface Connect	**X**	
MCLK	I	Master Clock Input		**X**

MCLK1	I	Master Clock, Transceiver 1 and Transceiver 3	X	
MCLK2	I	Master Clock, Transceiver 2 and Transceiver 4	X	
MUX	I	Mux Bus Select	X	
OUTA1	O	User Selectable Output A		X
OUTA2	O	User Selectable Output A		X
OUTA3	O	User Selectable Output A		X
OUTA4	O	User Selectable Output A		X
OUTB1	O	User Selectable Output B		X
OUTB2	O	User Selectable Output B		X
OUTB3	O	User Selectable Output B		X
OUTB4	O	User Selectable Output B		X
PBTS	I	Parallel Bus Type Select		X
RCHBLK1	O	Receive Channel Block, Transceiver #1.	X	
RCHBLK2	O	Receive Channel Block, Transceiver #2.	X	
RCHBLK3	O	Receive Channel Block, Transceiver #3.	X	
RCHBLK4	O	Receive Channel Block, Transceiver #4.	X	
RCHCLK1	O	Receive Channel Clock, Transceiver #1.	X	
RCHCLK2	O	Receive Channel Clock, Transceiver #2.	X	
RCHCLK3	O	Receive Channel Clock, Transceiver #3.	X	
RCHCLK4	O	Receive Channel Clock, Transceiver #4.	X	
RCLK1	O	Receive Clock Output from the Framer, Transceiver #1.	X	
RCLK2	O	Receive Clock Output from the Framer, Transceiver #2.	X	
RCLK3	O	Receive Clock Output from the Framer, Transceiver #3.	X	
RCLK4	O	Receive Clock Output from the Framer, Transceiver #4.	X	
RCLKI1	I	Receive Clock Input for the LIU, Transceiver #1.	X	
RCLKI2	I	Receive Clock Input for the LIU, Transceiver #2.	X	
RCLKI3	I	Receive Clock Input for the LIU, Transceiver #3.	X	
RCLKI4	I	Receive Clock Input for the LIU, Transceiver #4.	X	
RCLKO1	O	Receive Clock Output from the LIU, Transceiver #1.	X	
RCLKO2	O	Receive Clock Output from the LIU, Transceiver #2.	X	
RCLKO3	O	Receive Clock Output from the LIU, Transceiver #3.	X	
RCLKO4	O	Receive Clock Output from the LIU, Transceiver #4.	X	
RD*(DS*)	I	Read Input (Data Strobe)	X	X
REFCLK	I/O	Reference Clock		X
RFSYNC1	O	Receive Frame Sync (before the receive elastic store), Transceiver #1.	X	
RFSYNC2	O	Receive Frame Sync (before the receive elastic	X	

		store), Transceiver #2.		
RFSYNC3	O	Receive Frame Sync (before the receive elastic store), Transceiver #3.	X	
RFSYNC4	O	Receive Frame Sync (before the receive elastic store), Transceiver #4.	X	
RLCLK1	O	Receive Link Clock, Transceiver #1.	X	
RLCLK2	O	Receive Link Clock, Transceiver #2.	X	
RLCLK3	O	Receive Link Clock, Transceiver #3.	X	
RLCLK4	O	Receive Link Clock, Transceiver #4.	X	
RLINK1	O	Receive Link Data, Transceiver #1.	X	
RLINK2	O	Receive Link Data, Transceiver #2.	X	
RLINK3	O	Receive Link Data, Transceiver #3.	X	
RLINK4	O	Receive Link Data, Transceiver #4.	X	
RLOS/LOTC1	O	Receive Loss of Sync / Loss Of Transmit Clock, Transceiver #1.	X	
RLOS/LOTC2	O	Receive Loss of Sync / Loss Of Transmit Clock, Transceiver #2.	X	
RLOS/LOTC3	O	Receive Loss of Sync / Loss Of Transmit Clock, Transceiver #3.	X	
RLOS/LOTC4	O	Receive Loss of Sync / Loss Of Transmit Clock, Transceiver #4.	X	
RMSYNC1	O	Receive Multiframe Sync, Transceiver #1.	X	
RMSYNC2	O	Receive Multiframe Sync, Transceiver #2.	X	
RMSYNC3	O	Receive Multiframe Sync, Transceiver #3.	X	
RMSYNC4	O	Receive Multiframe Sync, Transceiver #4.	X	
RNEGI1	I	Receive Negative Data for the Framer, Transceiver #1.	X	
RNEGI2	I	Receive Negative Data for the Framer, Transceiver #2.	X	
RNEGI3	I	Receive Negative Data for the Framer, Transceiver #3.	X	
RNEGI4	I	Receive Negative Data for the Framer, Transceiver #4.	X	
RNEGO1	O	Receive Negative Data from the LIU, Transceiver #1.	X	
RNEGO2	O	Receive Negative Data from the LIU, Transceiver #2.	X	
RNEGO3	O	Receive Negative Data from the LIU, Transceiver #3.	X	
RNEGO4	O	Receive Negative Data from the LIU, Transceiver #4.	X	
RPOSI1	I	Recekve Positive Data for the Framer, Transceiver #1.	X	

RPOSI2	I	Recekve Positive Data for the Framer, Transceiver #2.	X	
RPOSI3	I	Recekve Positive Data for the Framer, Transceiver #3.	X	
RPOSI4	I	Recekve Positive Data for the Framer, Transceiver #4.	X	
RPOSO1	O	Receive Positive Data from the LIU, Transceiver #1.	X	
RPOSO2	O	Receive Positive Data from the LIU, Transceiver #2.	X	
RPOSO3	O	Receive Positive Data from the LIU, Transceiver #3.	X	
RPOSO4	O	Receive Positive Data from the LIU, Transceiver #4.	X	
RRING1	I	Receive Analog Ring Input, Transceiver #1.	X	X
RRING2	I	Receive Analog Ring Input, Transceiver #2.	X	X
RRING3	I	Receive Analog Ring Input, Transceiver #3.	X	X
RRING4	I	Receive Analog Ring Input, Transceiver #4.	X	X
RSER1	O	Receive Serial Data, Transceiver #1.	X	X
RSER2	O	Receive Serial Data, Transceiver #2.	X	X
RSER3	O	Receive Serial Data, Transceiver #3.	X	X
RSER4	O	Receive Serial Data, Transceiver #4.	X	X
RSIG1	O	Receive Signaling Output, Transceiver #1.	X	
RSIG2	O	Receive Signaling Output, Transceiver #2.	X	
RSIG3	O	Receive Signaling Output, Transceiver #3.	X	
RSIG4	O	Receive Signaling Output, Transceiver #4.	X	
RSIGF1	O	Receive Signaling Freeze Output, Transceiver #1.	X	
RSIGF2	O	Receive Signaling Freeze Output, Transceiver #2.	X	
RSIGF3	O	Receive Signaling Freeze Output, Transceiver #3.	X	
RSIGF4	O	Receive Signaling Freeze Output, Transceiver #4.	X	
RSYNC1	I/O	Receive Sync, Transceiver #1.	X	X
RSYNC2	I/O	Receive Sync, Transceiver #2.	X	X
RSYNC3	I/O	Receive Sync, Transceiver #3.	X	X
RSYNC4	I/O	Receive Sync, Transceiver #4.	X	X
RSYSCLK1	I	Receive System Clock, Transceiver #1.	X	
RSYSCLK2	I	Receive System Clock, Transceiver #2.	X	
RSYSCLK3	I	Receive System Clock, Transceiver #3.	X	
RSYSCLK4	I	Receive System Clock, Transceiver #4.	X	
RTIP1	I	Receive Analog Tip Input, Transceiver #1.	X	X
RTIP2	I	Receive Analog Tip Input, Transceiver #2.	X	X
RTIP3	I	Receive Analog Tip Input, Transceiver #3.	X	X
RTIP4	I	Receive Analog Tip Input, Transceiver #4.	X	X
RVDD1	--	Receive Analog Positive Supply.	X	X
RVDD2	--	Receive Analog Positive Supply.	X	X
RVDD3	--	Receive Analog Positive Supply.	X	X

RVDD4	--	Receive Analog Positive Supply.	X	X
RVSS1	--	Receive Analog Signal Ground	X (Note 3)	X
RVSS2	--	Receive Analog Signal Ground	X (Note 3)	X
RVSS3	--	Receive Analog Signal Ground	X (Note 3)	X
RVSS4	--	Receive Analog Signal Ground	X (Note 3)	X
SYSCLK1	I	Transmit/Receive System Clock		X
SYSCLK2	I	Transmit/Receive System Clock		X
SYSCLK3	I	Transmit/Receive System Clock		X
SYSCLK4	I	Transmit/Receive System Clock		X
TCHBLK1	O	Transmit Channel Block, Transceiver #1.	X	
TCHBLK2	O	Transmit Channel Block, Transceiver #2.	X	
TCHBLK3	O	Transmit Channel Block, Transceiver #3.	X	
TCHBLK4	O	Transmit Channel Block, Transceiver #4.	X	
TCHCLK1	O	Transmit Channel Clock, Transceiver #1.	X	
TCHCLK2	O	Transmit Channel Clock, Transceiver #2.	X	
TCHCLK3	O	Transmit Channel Clock, Transceiver #3.	X	
TCHCLK4	O	Transmit Channel Clock, Transceiver #4.	X	
TCLK1	I	Transmit Clock, Transceiver #1.	X	X
TCLK2	I	Transmit Clock, Transceiver #2.	X	X
TCLK3	I	Transmit Clock, Transceiver #3.	X	X
TCLK4	I	Transmit Clock, Transceiver #4.	X	X
TCLKI1	I	Transmit Clock Input for the LIU, Transceiver #1.	X	
TCLKI2	I	Transmit Clock Input for the LIU, Transceiver #2.	X	
TCLKI3	I	Transmit Clock Input for the LIU, Transceiver #3.	X	
TCLKI4	I	Transmit Clock Input for the LIU, Transceiver #4.	X	
TCLKO1	O	Transmit Clock Output from the Framer, Transceiver #1.	X	
TCLKO2	O	Transmit Clock Output from the Framer, Transceiver #2.	X	
TCLKO3	O	Transmit Clock Output from the Framer, Transceiver #3.	X	
TCLKO4	O	Transmit Clock Output from the Framer, Transceiver #4.	X	
TLCLK1	O	Transmit Link Clock, Transceiver #1.	X	
TLCLK2	O	Transmit Link Clock, Transceiver #2.	X	
TLCLK3	O	Transmit Link Clock, Transceiver #3.	X	
TLCLK4	O	Transmit Link Clock, Transceiver #4.	X	
TLINK1	I	Transmit Link Data, Transceiver #1.	X	
TLINK2	I	Transmit Link Data, Transceiver #2.	X	
TLINK3	I	Transmit Link Data, Transceiver #3.	X	

TLINK4	I	Transmit Link Data, Transceiver #4.	X	
TNEGI1	I	Transmit Negative Data Input for the LIU, Transceiver #1.	X	
TNEGI2	I	Transmit Negative Data Input for the LIU, Transceiver #2.	X	
TNEGI3	I	Transmit Negative Data Input for the LIU, Transceiver #3.	X	
TNEGI4	I	Transmit Negative Data Input for the LIU, Transceiver #4.	X	
TNEGO1	O	Transmit Negative Data Output from Framer, Transceiver #1.	X	
TNEGO2	O	Transmit Negative Data Output from Framer, Transceiver #2.	X	
TNEGO3	O	Transmit Negative Data Output from Framer, Transceiver #3.	X	
TNEGO4	O	Transmit Negative Data Output from Framer, Transceiver #4.	X	
TPOSI1	I	Transmit Positive Data Input for the LIU, Transceiver #1.	X	
TPOSI2	I	Transmit Positive Data Input for the LIU, Transceiver #2.	X	
TPOSI3	I	Transmit Positive Data Input for the LIU, Transceiver #3.	X	
TPOSI4	I	Transmit Positive Data Input for the LIU, Transceiver #4.	X	
TPOSO1	O	Transmit Positive Data Output from Framer, Transceiver #1.	X	
TPOSO2	O	Transmit Positive Data Output from Framer, Transceiver #2.	X	
TPOSO3	O	Transmit Positive Data Output from Framer, Transceiver #3.	X	
TPOSO4	O	Transmit Positive Data Output from Framer, Transceiver #4.	X	
TRING1	O	Transmit Analog Ring Output, Transceiver #1.	X	X
TRING2	O	Transmit Analog Ring Output, Transceiver #2.	X	X
TRING3	O	Transmit Analog Ring Output, Transceiver #3.	X	X
TRING4	O	Transmit Analog Ring Output, Transceiver #4.	X	X
TS0	I	Transceiver Select 0		X
TS1	I	Transceiver Select 1		X
TSER1	I	Transmit Serial Data, Transceiver #1.	X	X
TSER2	I	Transmit Serial Data, Transceiver #2.	X	X
TSER3	I	Transmit Serial Data, Transceiver #3.	X	X
TSER4	I	Transmit Serial Data, Transceiver #4.	X	X
TSIG1	I	Transmit Signaling Input, Transceiver #1.	X	

TSIG2	I	Transmit Signaling Input, Transceiver #2.	X	
TSIG3	I	Transmit Signaling Input, Transceiver #3.	X	
TSIG4	I	Transmit Signaling Input, Transceiver #4.	X	
TSSYNC1	I	Transmit System Sync, Transceiver #1.	X	
TSSYNC2	I	Transmit System Sync, Transceiver #2.	X	
TSSYNC3	I	Transmit System Sync, Transceiver #3.	X	
TSSYNC4	I	Transmit System Sync, Transceiver #4.	X	
TSTRST	I	Test/Reset	X	
TSYNC1	I/O	Transmit Sync, Transceiver #1.	X	X
TSYNC2	I/O	Transmit Sync, Transceiver #2.	X	X
TSYNC3	I/O	Transmit Sync, Transceiver #3.	X	X
TSYNC4	I/O	Transmit Sync, Transceiver #4.	X	X
TSYSCLK1	I	Transmit System Clock, Transceiver #1.	X	
TSYSCLK2	I	Transmit System Clock, Transceiver #2.	X	
TSYSCLK3	I	Transmit System Clock, Transceiver #3.	X	
TSYSCLK4	I	Transmit System Clock, Transceiver #4.	X	
TTIP1	O	Transmit Analog Tip Output, Transceiver #1.	X	X
TTIP2	O	Transmit Analog Tip Output, Transceiver #2.	X	X
TTIP3	O	Transmit Analog Tip Output, Transceiver #3.	X	X
TTIP4	O	Transmit Analog Tip Output, Transceiver #4.	X	X
TVDD1	--	Transmit Analog Positive Supply.	X	X
TVDD2	--	Transmit Analog Positive Supply.	X	X
TVDD3	--	Transmit Analog Positive Supply.	X	X
TVDD4	--	Transmit Analog Positive Supply.	X	X
TVSS1	--	Transmit Analog Signal Ground.	X	X
TVSS2	--	Transmit Analog Signal Ground.	X	X
TVSS3	--	Transmit Analog Signal Ground.	X	X
TVSS4	--	Transmit Analog Signal Ground.	X	X
WR* (R/W*)	I	Write Input (Read/Write)	X	X

Note 1: These are actually four V_{DD} power supply pins for each DS21Q55 supply line.
Note 2: These are actually three ground supply pins for each DS21Q55 supply line.
Note 3: These are actually two Analog Ground Supply pins for each supply line on the receive side for the DS21Q55 device.

Functional disimilarities among DS21Q55, DS21Q50 and DS21Q59.

DS21Q55 can do all the functional operations that DS21Q50 and DS21Q59 can do. Below are the functions that DS2155 can perform but DS21Q50 or DS21Q59 can not perform.

1. E1, T1 and J1 operation. Both the devices DS21Q50 and DS21Q59 are for E1 only.

2. JATG Capabilities: Each device (DS2155) has its own JTAG state machine and therefore is treated as 4 separate devices when testing. Each DS2155 IEEE 1149.1 design supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGH-Z, CLAMP, and IDCODE.

3. HDLC controller. The HDLC controllers transmit and receive data via the framer block. The HDLC controllers can be assigned to any time slot, group of time slots, portion of a time slot or Sa bits (E1).

4. Extended System Information Bus (ESIB) function allows up to eight transceivers, 2 DS21Q55s, to be accessed via a single read for interrupt status or other user selectable alarm status information.

5. Both the DS21Q50 and DS21Q59 do not have Transmission Elastic Store.

6. Both the DS21Q50 and DS21Q59 do not have Per Channel Idle Code.

7. Both the DS21Q50 and DS21Q59 do not have Hardware signalling. The DS21Q50 does not have SW signalling feature either, but DS21Q59 does.

Disimilarities between DS21Q50 and DS21Q59

Register Disimilarities

Most of the registers are the same between the DS21Q50 and DS21Q59. Since the DS21Q59 support CAS/CCS signalling, so it has some extra registers that are not available on DS21Q50.

ADDRESS	R/W	REGISTER NAME	DS21Q50	DS21Q59
1F	R/W	Test 2	**X**	
1F	R/W	Common Control 7		**X**
2F	R/W	Test 1	**X**	
2F	R/W	Common Control 6		**X**
30	R/W	Signaling Access Register 1		**X**
31	R/W	Signaling Access Register 2		**X**
32	R/W	Signaling Access Register 3		**X**
33	R/W	Signaling Access Register 4		**X**
34	R/W	Signaling Access Register 5		**X**
35	R/W	Signaling Access Register 6		**X**
36	R/W	Signaling Access Register 7		**X**
37	R/W	Signaling Access Register 8		**X**
38	R/W	Signaling Access Register 9		**X**
39	R/W	Signaling Access Register 10		**X**
3A	R/W	Signaling Access Register 11		**X**

3B	R/W	Signaling Access Register 12		**X**
3C	R/W	Signaling Access Register 13		**X**
3D	R/W	Signaling Access Register 14		**X**
3E	R/W	Signaling Access Register 15		**X**
3F	R/W	Signaling Access Register 16		**X**

Signaling Operation of DS21Q59

These Signaling Access Registers are not available on DS21Q50. Registers SA1 and SA16 are used to access the transmit and receive signaling function. Normally, reading these registers accesses the receive signaling data and writing these registers sources signaling data for the transmitter. The user can read what was written to the transmit signaling buffer by setting CCR6.5 = 1, then reading SA1 - SA16. In most applications however, CCR6.5 should be set = 0.

Receive Signaling

Signaling data is sampled from time slot 16 in the receive data stream and copied into the receive signaling buffers. The host can access the signaling data by reading SA1 through SA16. The signaling information in these registers is always updated on multiframe boundaries. The SR2.7 bit in Status Register 2 can be used to alert the host that new signaling data is present in the receive signaling buffers. The host has 2ms to read the signaling buffers before they are updated.

Transmit Signaling

Insertion of signaling data from the transmit signaling buffers is enabled by setting CCR6.3 = 1. Signaling data is loaded into the transmit-signaling buffers by writing the signaling data to SA1 - SA16. On multiframe boundaries, the contents of the transmit signaling buffer is loaded into a shift register for placement in the appropriate bit position in the outgoing data stream. The user can utilize the transmit multiframe interrupt in status register 2 (SR2.5) to know when to update the signaling bits. The host has 2ms to update the signaling data. The user only needs to update the signaling data that has changed since the last update.

CAS Operation

For CAS mode, the user must provide the CAS alignment pattern (4 zeros in the upper nibble of TS16). Typically this is done by setting the upper 4 bits of SA1 = 0. The lower four bits are alarm bits. The user only needs to update the appropriate channel associated signaling data in SA2 - SA16 on multiframe boundaries.

Disimilarities on Control, ID, and Test Registers

For the DS21Q50, the operation of the DS21Q50 is configured via a set of seven control registers. The DS21Q50 has only five Common Control Registers (CCR1 to CCR5).

The device Identification Register (IDR) is at address 0Fh. The MSB of this read-only register is fixed to a one indicating that an E1 Quad Transceiver is present. The next 3 MSBs are reserved for future use. The lower 4 bits of the device ID register are used to identify the revision of the device. This register exists in Transceiver #1 only. (TS0, TS1 = 0)

The Test registers at addresses 1E, 1F, and 2F hex are used by the factory in testing the DS21Q50. On power-up, the Test registers should be set to 00h in order for the DS21Q50 to operate properly.

Register Name: **IDR**

Register Description: **Device Identification Register**
Register Address: **0F Hex**

Bit#	7	6	5	4	3	2	1	0
SYM	1	0	0	0	ID3	ID2	ID1	ID0

SYMBOL	BIT	NAME AND DESCRIPTION
1	7	**Bit 7.**
0	6	**Bit 6.**
0	5	**Bit 5.**
0	4	**Bit 4.**
ID3	3	**Chip Revision Bit 3.** MSB of a decimal code that represents the chip revision.
ID2	1	**Chip Revision Bit 2.**
ID1	2	**Chip Revision Bit 1.**
ID0	0	**Chip Revision Bit 0.** LSB of a decimal code that represents the chip revision.

For the DS21Q59, the operation of the DS21Q59 is configured via a set of nine control registers. There are seven Common Control Registers (CCR1 to CCR7).

There is a device identification register (IDR) at address 0Fh. The 4 MSBs of this read-only register are fixed to 1 0 0 1, indicating that a DS21Q59 E1 quad transceiver is present. The lower 4 bits of the device ID register are used to identify the revision of the device. This register exists in Transceiver #1 only. (TS0, TS1 = 0)

The test register at addresses 1E, is used by the factory in testing the DS21Q59. On power-up, the test register should be set to 00h in order for the DS21Q59 to operate properly.

Register Name: **IDR**
Register Description: **Device Identification Register**
Register Address: **0F Hex**

Bit#	7	6	5	4	3	2	1	0
SYM	1	0	0	1	ID3	ID2	ID1	ID0

SYMBOL	BIT	NAME AND DESCRIPTION
1	7	**Bit 7.**
0	6	**Bit 6.**
0	5	**Bit 5.**
1	4	**Bit 4.**
ID3	3	**Chip Revision Bit 3.** MSB of a decimal code that represents the chip revision.
ID2	1	**Chip Revision Bit 2.**
ID1	2	**Chip Revision Bit 1.**

ID0	0	**Chip Revision Bit 0.** LSB of a decimal code that represents the chip revision.

Disimilarities on Interrupt Handling

The DS21Q59 is a direct replacement for the DS21Q50 with the addition of improved interrupt handling. IN DS21Q59, some event-based interrupts will occur continuously as long as the event is occurring (RSLIP, SEC, TMF, RMF, TAF, RAF, RCMF). Other event-based interrupts force the INT pin low only once when the event is first detected (LOTC, PRSBD, RDMA, RSA1, RSA0), i.e., the PRBSD interrupt will fire once when the receiver detects the PRBS pattern. IF the receiver continues to receive the PRBS pattern, no more interrupts will fire. If the receiver then detects that PRBS is no longer being sent, the receiver will reset and when it receives the PRBS pattern again, another interrupt will fire.

DS21Q59 can quickly determine which of status registers in the 4 ports are causing an interrupt by reading one of the unused addresses such as 0Ch, 0Dh or 0Eh in any port.

Bit#	7	6	5	4	3	2	1	0
SYM	SR2P4	SR1P4	SR2P3	SR1P3	SR2P2	SR1P2	SR2P1	SR1P1

SYMBOL	BIT	NAME AND DESCRIPTION
SR2P4	7	**Status Register 2 Port 4.** A one in this bit position indicates that Status Register 2 in port 4 is asserting an interrupt.
SR1P4	6	**Status Register 1 Port 4.** A one in this bit position indicates that Status Register 1 in port 4 is asserting an interrupt.
SR2P3	5	**Status Register 2 Port 3.** A one in this bit position indicates that Status Register 2 in port 3 is asserting an interrupt.
SR1P3	4	**Status Register 1 Port 3.** A one in this bit position indicates that Status Register 1 in port 3 is asserting an interrupt.
SR2P2	3	**Status Register 2 Port 2.** A one in this bit position indicates that Status Register 2 in port 2 is asserting an interrupt.
SR1P2	2	**Status Register 1 Port 2.** A one in this bit position indicates that Status Register 1 in port 2 is asserting an interrupt.
SR2P1	1	**Status Register 2 Port 1.** A one in this bit position indicates that Status Register 2 in port 1 is asserting an interrupt.
SR1P1	0	**Status Register 1 Port 1.** A one in this bit position indicates that Status Register 1 in port 1 is asserting an interrupt.

If you have any questions on migration, then please contact the Maxim Telecommunication Applications support.

Related Parts	
DS21Q50	Quad E1 Transceiver
DS21Q55	Quad T1/E1/J1 Transceiver
DS21Q59	E1 Quad Transceiver

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples
Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 396: http://www.maximintegrated.com/an396
APPLICATION NOTE 396, AN396, AN 396, APP396, Appnote396, Appnote 396