WP_MICRODAA_011 April 2008

MicroDAA DC Control Loop Operation

This white paper provides additional information on the DC control loop as implemented in the 73M1x22 and 73M1x66B MicroDAA™ devices.

The MicroDAA DC control loop is designed to allow the relatively high voltages that exist on the line to operate with the 73M1916/73M1912 that is powered by a 3.3 V supply generated from the transformer barrier signal coming from the host side 73M1906B/73M1902. A small amount of current (~7 mA) is also taken from the line. The function of the DC loop is to control the DC voltage/current ratio so that the DAA presents an approximately 50 Ω load in series with a fixed DC voltage bias thereby providing the proper Tip/Ring voltage. This is accomplished though a servo loop that samples the voltage and adjusts its output to compensate for the current variations from the line.

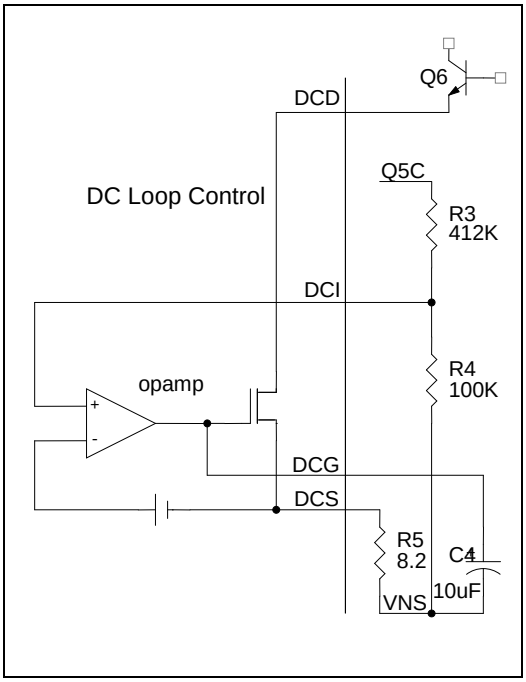

Figure 1: Simplified DC Loop Circuit

Figure 1 is a simplified diagram of the DC loop and its control. The switch transistor Q6 is turned on when the 73M1916 or 73M1912 is set to off hook. The collector of Q5 (Q5C) is the point that is the output of the DC loop since this is the output of the transmit AC signal and must also determine the DC operating point. This output is sensed by the divider R3 and R4 which comprise a 5:1 divider. This divider is used to keep the voltages within the power supply limits of the 73M1916/73M1912. The "battery" represents the voltage offset on top of which the 50 Ω resistance resides. The 50 Ω is realized by the resistance of R5 (8.2 Ω) times the divider ratio of R3/R4 (about 5, so 8.2X5=41 Ω) plus the other external resistances, the main one being the resettable fuse that is typically 8 Ω. There are other fixed voltage drops that contribute to the total voltage at Tip/Ring, such as the switch "on" voltage and diode bridge. These are all factored in to the voltage level set by the DCVI(1:0) bits of the MicroDAA.

The DC loop control supports two acquisition modes controlled by the state of ENNOM. There is a "fast" acquisition mode that allows the loop to settle quickly when going off hook (ENNOM=0), and there is a "slow" nominal mode that provides the higher AC impedance needed when the DC loop has settled (ENNOM=1). The 73M1916/73M1912 should only be set to the slow mode after the DC level has had adequate time to settle, at least 300 ms to prevent any circuit instability. Once the DC loop has fully settled in the fast mode, the ENNOM bit is set to 1 so the tip/ring voltage will not be affected by fast transient changes at the line. If the loop is broken for any reason, the ENNOM bit should be reset to 0 so the DC loop can settle quickly again when the loop is restored, after which ENNOM can be re-enabled. This can easily be sensed by monitoring the loop voltage and /or current in registers 1Bh and 1Ch.

Figure 2 shows the relationship between the loop current and the tip to ring voltage with the four DCVI settings available on the 73M1x66B/73M1x22. These settings should satisfy any country's PTT requirements.

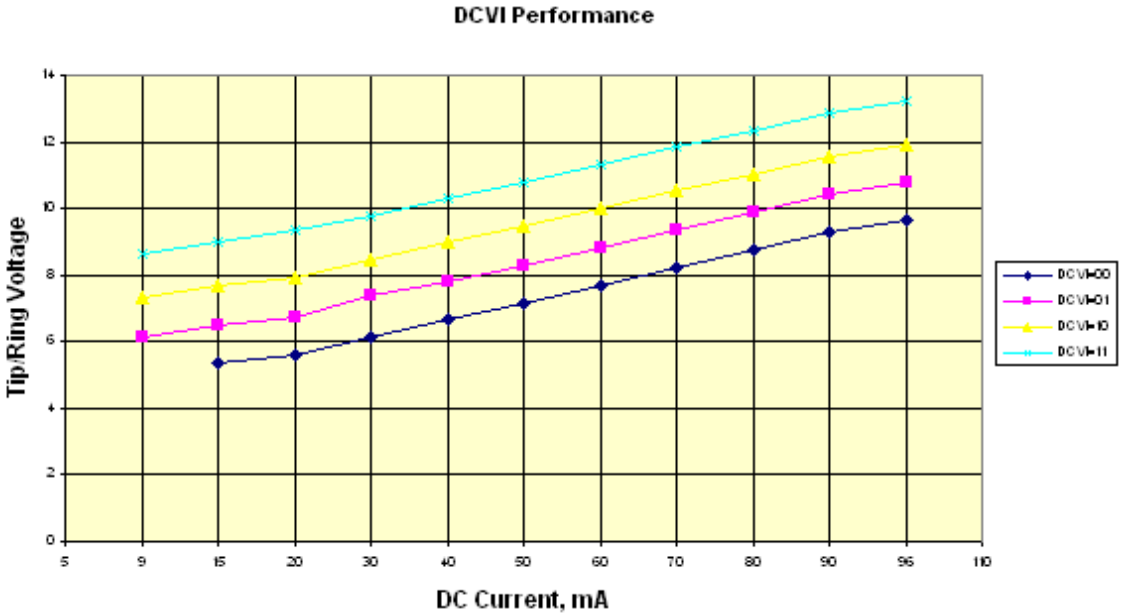

Figure 2: DCVI Characteristics of the 73M1966B

In the case of Australia two different loop conditions are supported by the MicroDAA. The steady-state hold condition is met by using the DCVI1:0=11 setting above, but there is also a separate condition immediately after going off hook that is also defined in AS/ACIF S002 called the seize state. At this time the tip/ring voltage must be at a lower level than during the hold time, and this can be accomplished but using the "seize mode" which is selected by setting ENDC=1 and at the same time ENAC=0. The resulting tip/ring voltage is shown in Figure 3.

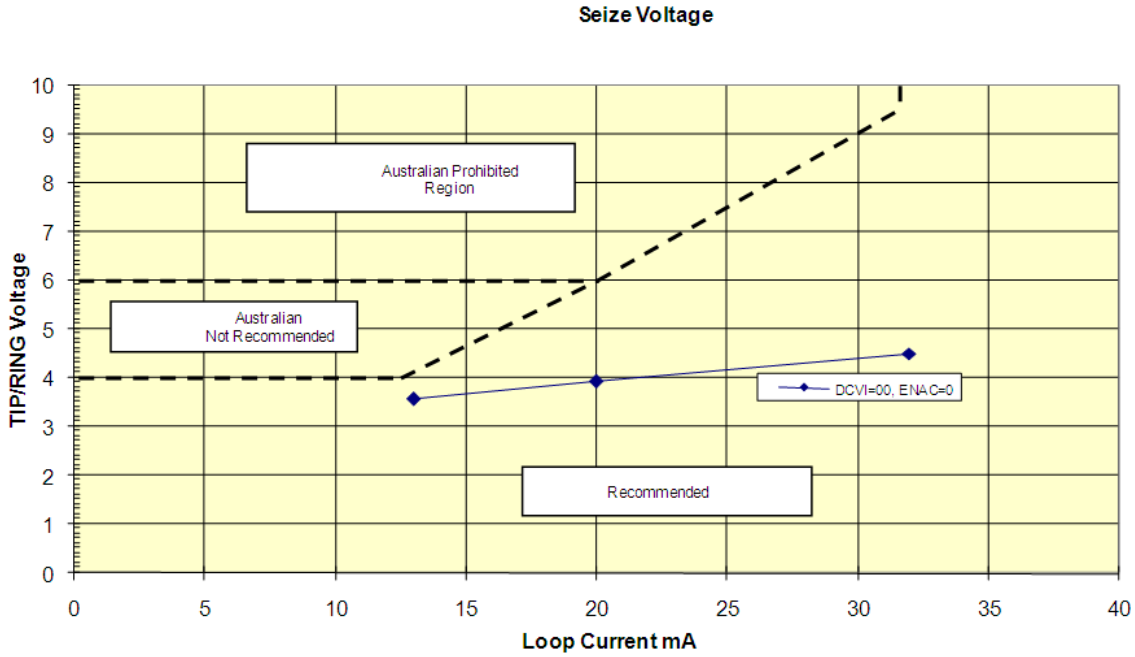

Figure 3: Seize State DCVI Performance

The DCVI characteristics in seize mode have a much lower voltage for a given current than when in the hold mode with both ENDC and ENAC set to 1. During seize mode the setting of the DCVI bits has no effect on the tip/ring DC voltage. This assures the CO is able to detect the off hook state of the CPE device. The seize state is only required for the first 300 ms after going off hook, after which the hold state should be enabled.