ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at
www.onsemi.com

onsemi and onsemi and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi** product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner. Other names and brands may be claimed as the property of others.

J110

JFET - General Purpose

N−Channel − Depletion

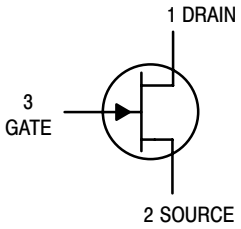
N−Channel Junction Field Effect Transistors, depletion mode (Type A) designed for general purpose audio amplifiers, analog switches and choppers.

Features

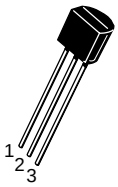
- N−Channel for Higher Gain
- Drain and Source Interchangeable
- High AC Input Impedance
- High DC Input Resistance
- Low $R_{DS(on)}$ < 18 Ω
- Fast Switching $t_{d(on)} + t_r$ = 8.0 ns (Typ)
- Low Noise $\overline{en}$ = 6.0 nV/$\sqrt{Hz}$ @ 10 Hz (Typ)
- Pb−Free Packages are Available*

ON Semiconductor®

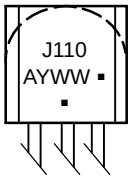
http://onsemi.com



MARKING DIAGRAM



CASE 29
TO−92 (TO−226)
STYLE 5



J110 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Gate−Source Voltage	VG_S	−25	Vdc
Drain−Gate Voltage	V_{DG}	−25	Vdc
Gate Current	I_G	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	 310 2.82	 mW mW/°C
Operating Junction Temp Range	T_J	135	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
J110	TO−92	1000 Units / Box
J110G	TO−92 (Pb−Free)	1000 Units / Box
J110RLRA	TO−92	2000 / Tape & Reel
J110RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

© Semiconductor Components Industries, LLC, 2005

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
STATIC CHARACTERISTICS					
Gate−Source Breakdown Voltage	(I_G = −1.0 μAdc)	$V_{(BR)GSS}$	−25	−	Vdc
Gate Reverse Current	(V_{GS} = −15 Vdc, V_{DS} = 0) (V_{GS} = −15 Vdc, V_{DS} = 0, T_A = 100°C)	I_{GSS}	− −	−3.0 −200	nAdc
Gate−Source Cutoff Voltage	(V_{DS} = 5.0 Vdc, I_D = 1.0 μAdc)	$V_{GS(off)}$	−0.5	−4.0	Vdc
Drain Source On−Resistance	(V_{DS} ≤ 0.1 V, V_{GS} = 0 V)	$R_{DS(on)}$	−	18	Ω
Zero−Gate−Voltage Drain Current (Note 1)	(V_{DS} = 15 Vdc)	I_{DSS}	10	−	mAdc
DYNAMIC CHARACTERISTICS					
Drain−Gate and Source−Gate On−Capacitance (V_{DS} = V_{GS} = 0, f = 1.0 MHz)		$C_{dg(on)}$ + $C_{sg(on)}$	−	85	pF
Drain−Gate Off−Capacitance	(V_{GS} = −10 Vdc, f = 1.0 MHz)	$C_{dg(off)}$	−	15	pF
Source−Gate Off−Capacitance	(V_{GS} = −10 Vdc, f = 1.0 MHz)	$C_{sg(off)}$	−	15	pF

1. Pulse Width = 300 μs, Duty Cycle = 3.0%.

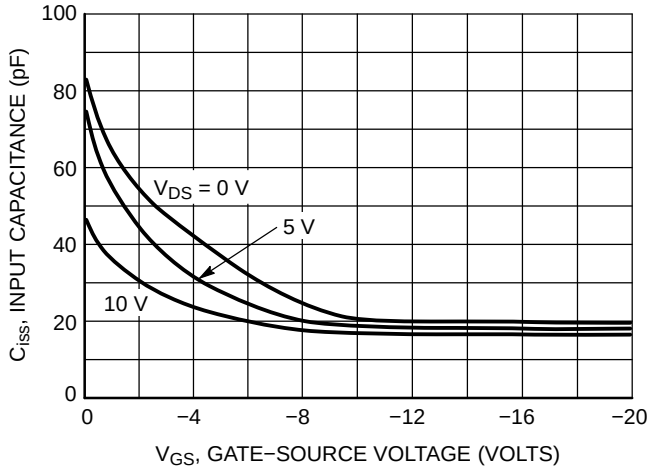


Figure 1. Common Source Input Capacitance versus Gate−Source Voltage

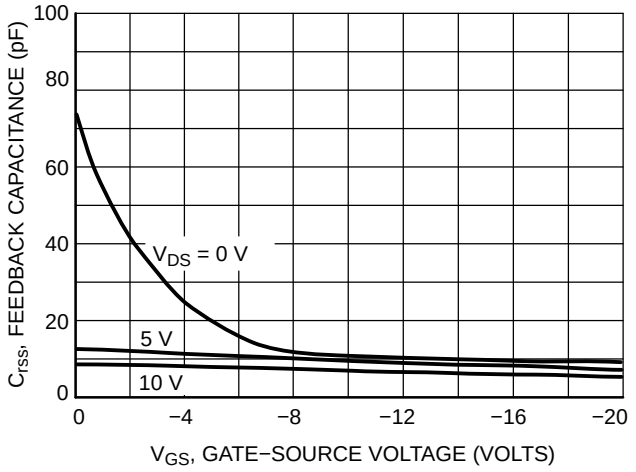


Figure 2. Common Source Reverse Feedback Capacitance versus Gate−Source Voltage

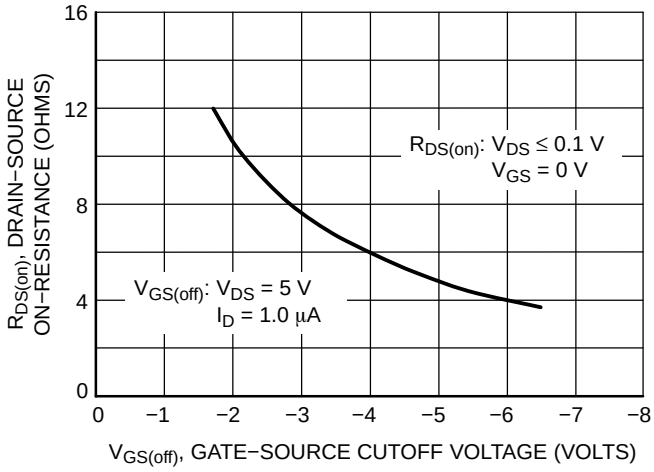


Figure 3. On−Resistance versus Gate−Source Cutoff Voltage

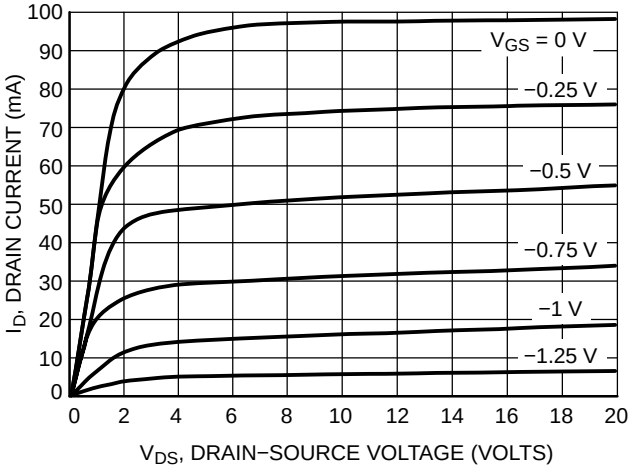


Figure 4. Output Characteristic $V_{GS(off)}$ = −2.0 V

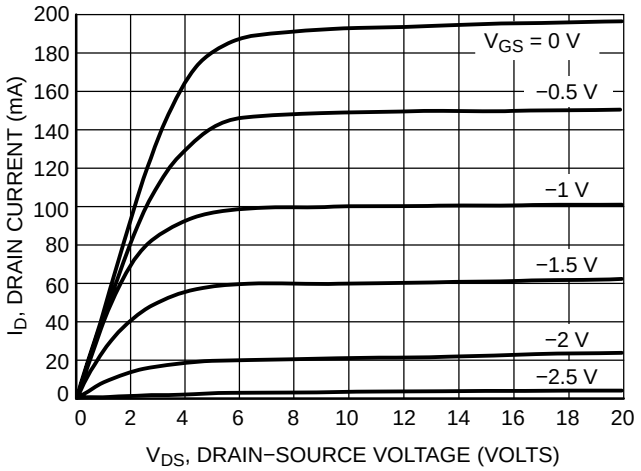


Figure 5. Output Characteristic
$V_{GS(off)}$ = −3.0 V

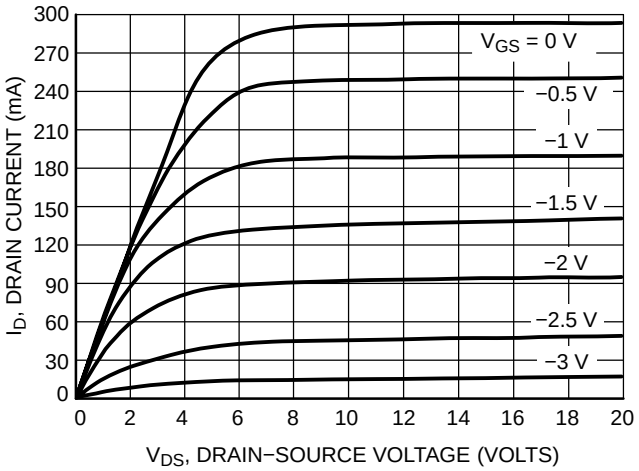


Figure 6. Output Characteristic
$V_{GS(off)}$ = −4.0 V

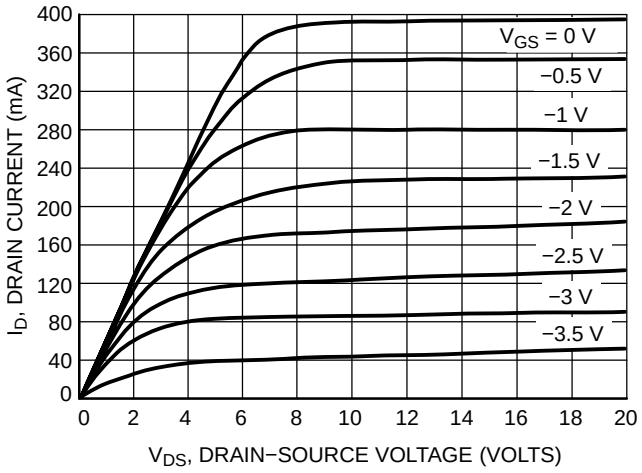
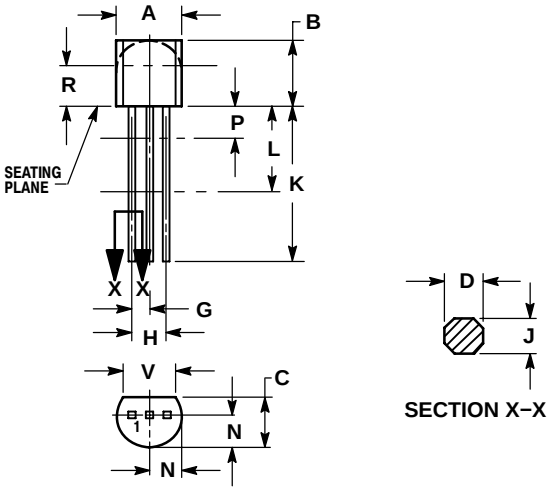


Figure 7. Output Characteristic
$V_{GS(off)}$ = −5.0 V

PACKAGE DIMENSIONS

TO−92 (TO−226)
CASE 29−11
ISSUE AL



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

ON Semiconductor Website: http://onsemi.com

Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.

J110/D