

Data Sheet



Description/Applications

The HSMP-383x series of general purpose PIN diodes are designed for two classes of applications. The first is attenuators where current consumption is the most important design consideration. The second application for this series of diodes is in switches where low capacitance is the driving issue for the designer.

The HSMP-386x series Total Capacitance (C_T) and Total Resistance (R_T) are typical specifications. For applications that require guaranteed performance, the general purpose HSMP-383x series is recommended.

A SPICE model is not available for PIN diodes as SPICE does not provide for a key PIN diode characteristic, carrier lifetime.

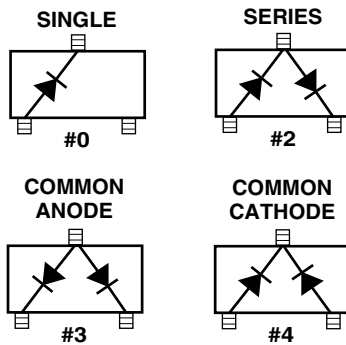
Features

- Diodes Optimized for:
Low Capacitance Switching
Low Current Attenuator
- Surface Mount SOT-23 Package
Single and Dual Versions
Tape and Reel Options Available
- Low Failure in Time (FIT) Rate^[1]
- Lead-free

Note:

1. For more information see the Surface Mount PIN Reliability Data Sheet.

Package Lead Code Identification (Top View)



Absolute Maximum Ratings^[1] $T_C = 25^\circ\text{C}$

Symbol	Parameter	Units	Absolute Maximum
I_F	Forward Current (1 ms Pulse)	Amp	1
P_t	Total Device Dissipation	mW ^[2]	250
P_{IV}	Peak Inverse Voltage	—	Same as V_{BR}
T_J	Junction Temperature	$^\circ\text{C}$	150
T_{STG}	Storage Temperature	$^\circ\text{C}$	-65 to 150

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. CW Power Dissipation at $T_{LEAD} = 25^\circ\text{C}$. Derate to zero at maximum rated temperature.

PIN General Purpose Diodes, Electrical Specifications $T_C = 25^\circ\text{C}$

Part Number HSMP-	Package Marking Code	Lead Code	Configuration	Minimum Breakdown Voltage V_{BR} (V)	Maximum Series Resistance R_S (Ω)	Maximum Total Capacitance C_T (pF)
3830	K0	0	Single	200	1.5	0.3
3832	K2	2	Series			
3833	K3	3	Common Anode			
3834	K4	4	Common Cathode			
Test Conditions				$V_R = V_{BR}$ Measure $I_R \leq 10 \mu\text{A}$	$I_F = 100 \text{ mA}$ $f = 100 \text{ MHz}$	$V_R = 50 \text{ V}$ $f = 1 \text{ MHz}$

Typical Parameters at $T_C = 25^\circ\text{C}$

Part Number HSMP-	Series Resistance R_S (Ω)	Carrier Lifetime τ (ns)	Reverse Recovery Time T_{rr} (ns)	Total Capacitance C_T (pF)
383x	20	500	80	0.20 @ 50 V
Test Conditions	$I_F = 1 \text{ mA}$ $f = 100 \text{ MHz}$	$I_F = 50 \text{ mA}$ $I_R = 250 \text{ mA}$	$V_R = 10 \text{ V}$ $I_F = 20 \text{ mA}$ 90% Recovery	

Typical Parameters at $T_C = 25^\circ\text{C}$ (unless otherwise noted), Single Diode

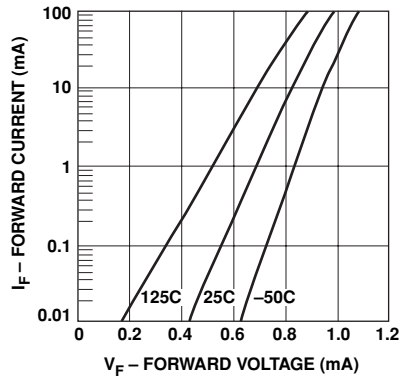


Figure 1. Forward Current vs. Forward Voltage.

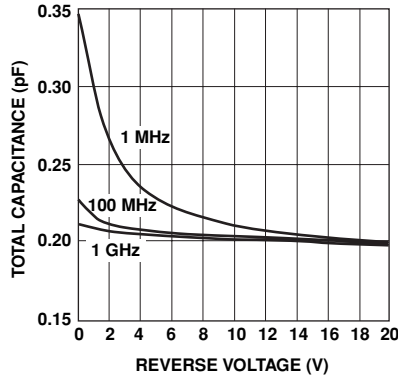


Figure 2. RF Capacitance vs. Reverse Bias.

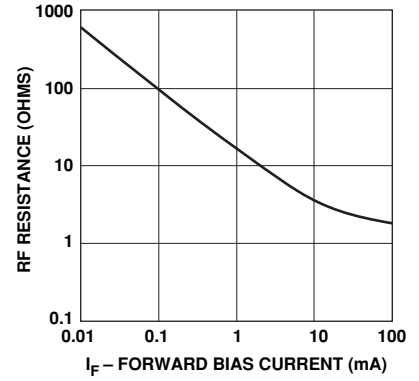


Figure 3. RF Resistance at 25C vs. Forward Bias Current.

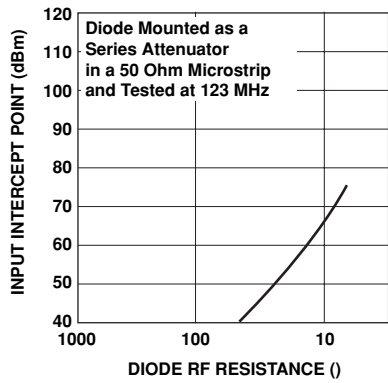


Figure 4. 2nd Harmonic Input Intercept Point vs. Diode RF Resistance for Attenuators.

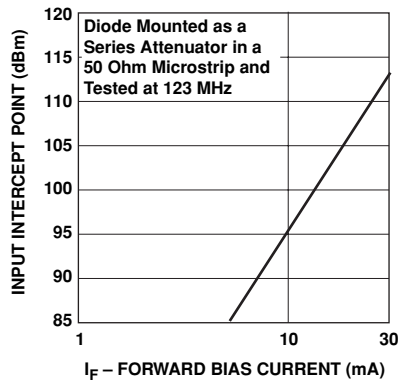


Figure 5. 2nd Harmonic Input Intercept Point vs. Forward Bias Current for Switches.

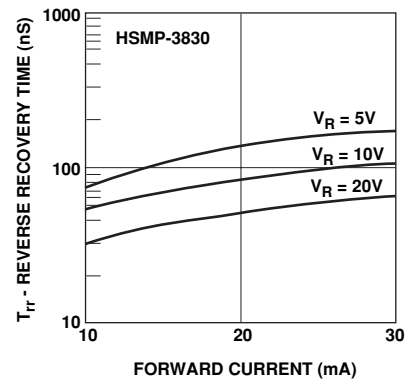


Figure 6. Reverse Recovery Time vs. Forward Current for Various Reverse Voltage.

Typical Applications for Multiple Diode Products

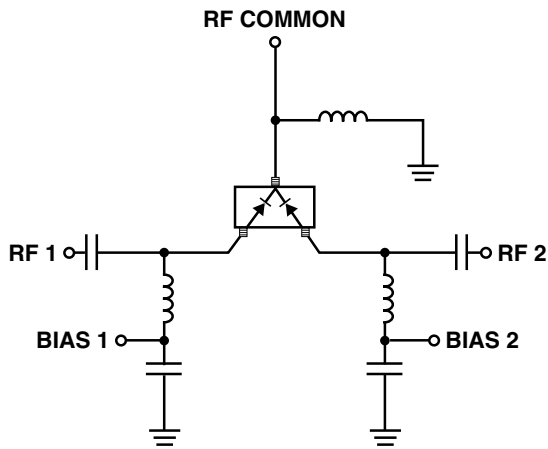


Figure 7. Simple SPDT Switch, Using Only Positive Current.

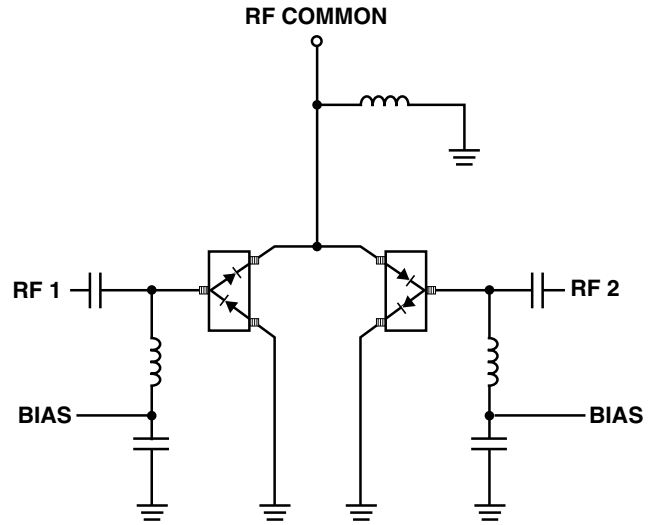


Figure 8. High Isolation SPDT Switch, Dual Bias.

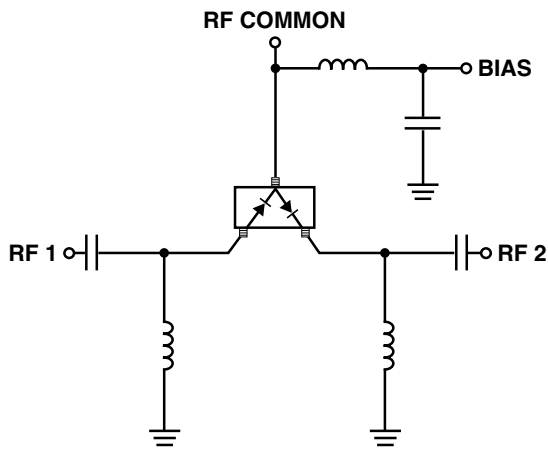


Figure 9. Switch Using Both Positive and Negative Current.

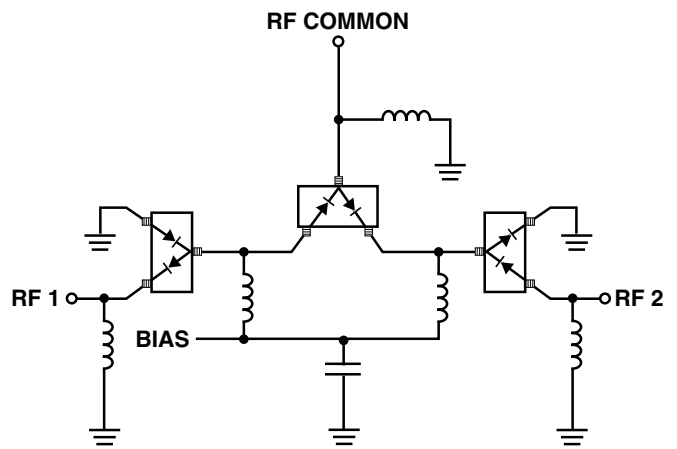


Figure 10. Very High Isolation SPDT Switch, Dual Bias.

Typical Applications for Multiple Diode Products (continued)

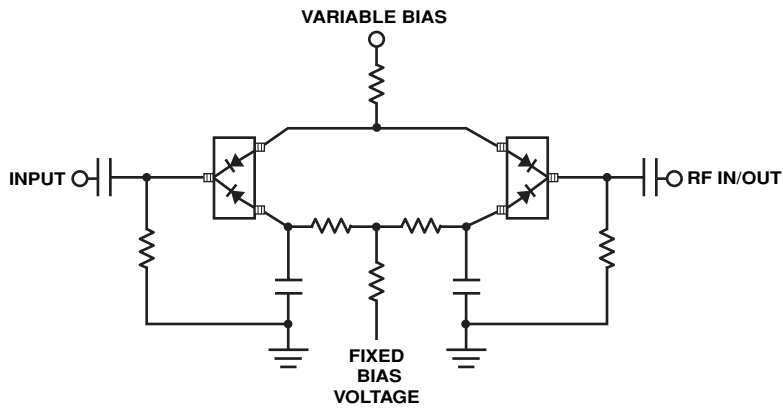


Figure 11. Four Diode π Attenuator. See AN1048 for details.

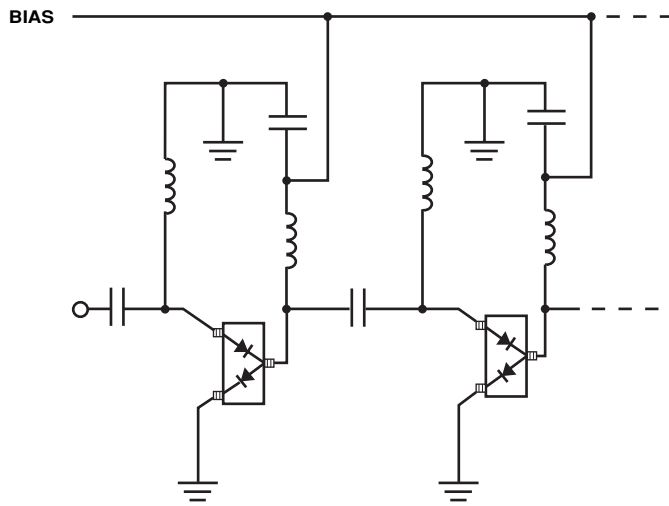
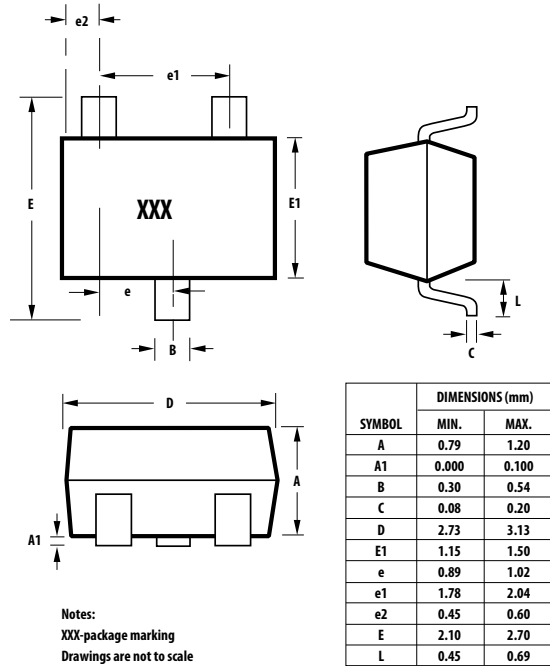
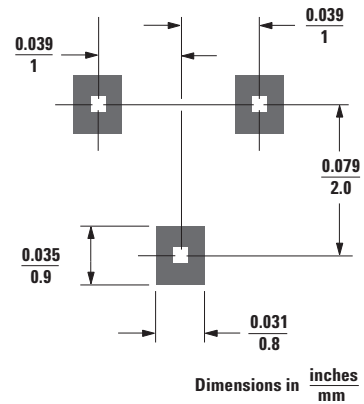


Figure 12. High Isolation SPST Switch (Repeat Cells as Required).

Package Dimensions Outline 23 (SOT-23)



Recommended PCB Pad Layout for Avago's SOT-23 Products

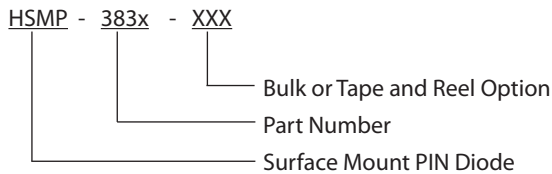


Package Characteristics

Lead MaterialAlloy 42
 Lead Finish Tin 100% (Lead-free option)
 Maximum Soldering Temperature 260°C for 5 seconds
 Minimum Lead Strength..... 2 pounds pull
 Typical Package Inductance 2 nH
 Typical Package Capacitance0.08 pF (opposite leads)

Ordering Information

Specify part number followed by option. For example:

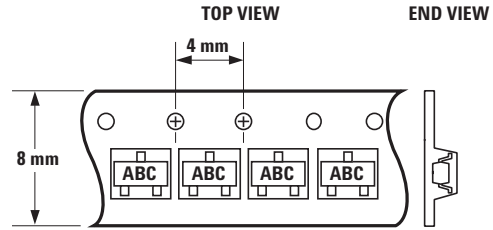
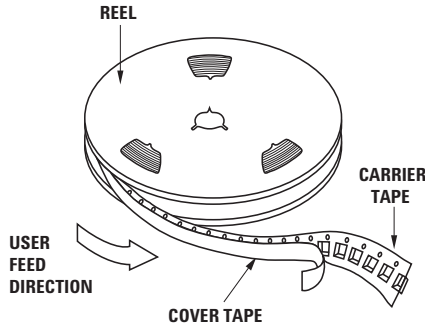


Profile Option Descriptions

- BLKG = Bulk
- TR1G = 3K pc. Tape and Reel, Device Orientation; See Figure 13
- TR2G = 10K pc. Tape and Reel, Device Orientation; See Figure 13

Tape and Reeling conforms to Electronic Industries RS-481, "Taping of Surface Mounted Components for Automated Placement."

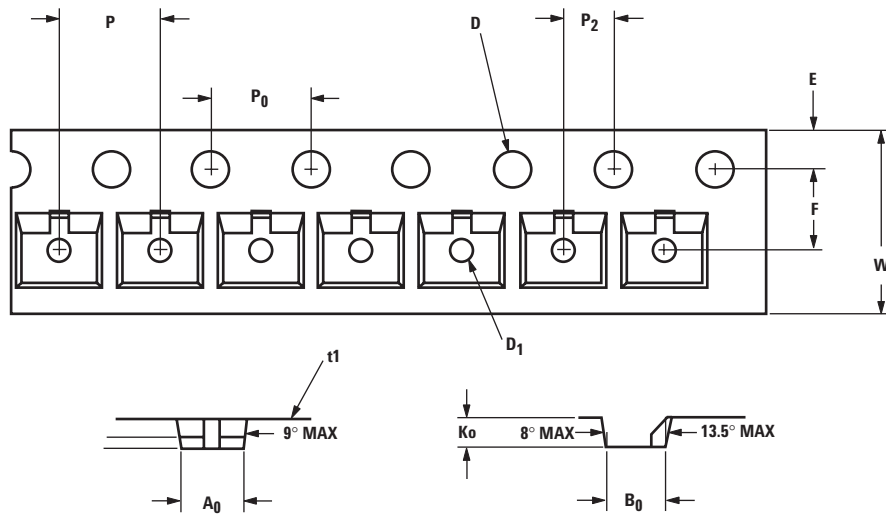
Device Orientation For Outlines SOT-23



Note: "AB" represents package marking code.
"C" represents date code.

Figure 13. Options -TR1, -TR2 for SOT-23 Packages.

Tape Dimensions and Product Orientation For Outline SOT-23



DESCRIPTION		SYMBOL	SIZE (mm)	SIZE (INCHES)
CAVITY	LENGTH	A ₀	3.15 ± 0.10	0.124 ± 0.004
	WIDTH	B ₀	2.77 ± 0.10	0.109 ± 0.004
	DEPTH	K ₀	1.22 ± 0.10	0.048 ± 0.004
	PITCH	P	4.00 ± 0.10	0.157 ± 0.004
	BOTTOM HOLE DIAMETER	D ₁	1.00 ± 0.05	0.039 ± 0.002
PERFORATION	DIAMETER	D	1.50 ± 0.10	0.059 ± 0.004
	PITCH	P ₀	4.00 ± 0.10	0.157 ± 0.004
	POSITION	E	1.75 ± 0.10	0.069 ± 0.004
CARRIER TAPE	WIDTH	W	8.00 + 0.30 - 0.10	0.315 + 0.012 - 0.004
	THICKNESS	t ₁	0.229 ± 0.013	0.009 ± 0.0005
DISTANCE BETWEEN CENTERLINE	CAVITY TO PERFORATION (WIDTH DIRECTION)	F	3.50 ± 0.05	0.138 ± 0.002
	CAVITY TO PERFORATION (LENGTH DIRECTION)	P ₂	2.00 ± 0.05	0.079 ± 0.002

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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