STL52DN4LF7AG

Automotive-grade dual N-channel 40 V, 9 mΩ typ., 18 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 DI

Datasheet - production data

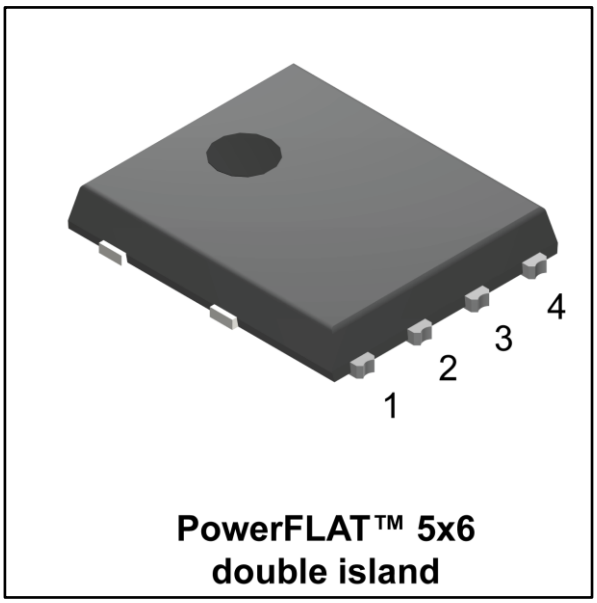
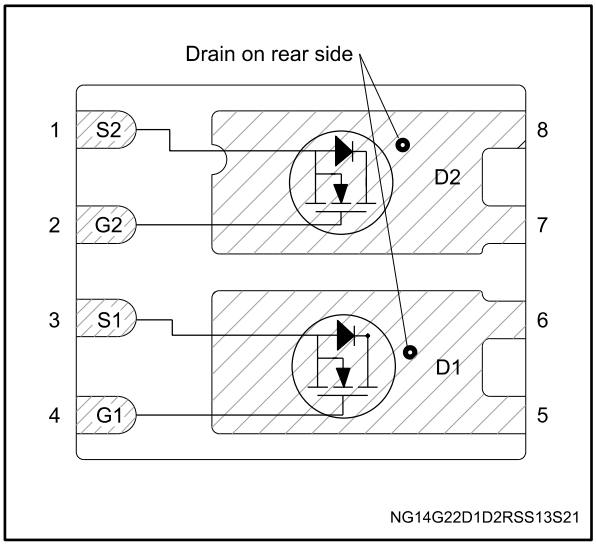


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STL52DN4LF7AG	40 V	16 mΩ	18 A

- AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STL52DN4LF7AG	52DN4LF7	PowerFLAT™ 5x6 double island	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	18	A
I_D (1)	Drain current (continuous) at T_c = 100 °C	18	A
I_{DM} (1)(2)	Drain current (pulsed)	72	A
P_{TOT}	Total dissipation at T_C = 25 °C	65	W
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operation junction temperature range		

Notes:

(1)Drain current is limited by package, the current capability of the silicon is 46 A at 25 °C and 33 A at 100 °C.

(2)Pulse width limited by safe operating area

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.3	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	32	

Notes:

(1)When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 s

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V V_{DS} = 40 V			10	µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 20 V, V_{DS} = 0 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 µA	1.5		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 6 A		9	16	mΩ
		V_{GS} = 4.5 V, I_D= 6 A		12	20	

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	500	-	pF
C_{oss}	Output capacitance		-	140	-	pF
C_{rss}	Reverse transfer capacitance		-	20	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 12 A, V_{GS} = 0 to 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	9.4	-	nC
Q_{gs}	Gate-source charge		-	1.6	-	nC
Q_{gd}	Gate-drain charge		-	2	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 32 V, I_D = 6 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	6.5	-	ns
t_r	Rise time		-	5	-	ns
$t_{d(off)}$	Turn-off delay time		-	48	-	ns
t_f	Fall time		-	14.5	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}(1)	Source-drain current		-		18	A
I_{SDM}(2)	Source-drain current (pulsed)		-		72	A
V_{SD}(3)	Forward on voltage	I_{SD} = 12 A, V_{GS} = 0 V	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs V_{DD} = 32 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	18		ns
Q_{rr}	Reverse recovery charge		-	7.5		nC
I_{RRM}	Reverse recovery current		-	0.8		A

Notes:

(1)Drain current is limited by package, the current capability of the silicon is 46 A at 25 °C.

(2) Pulse width limited by safe operating area.

(3)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

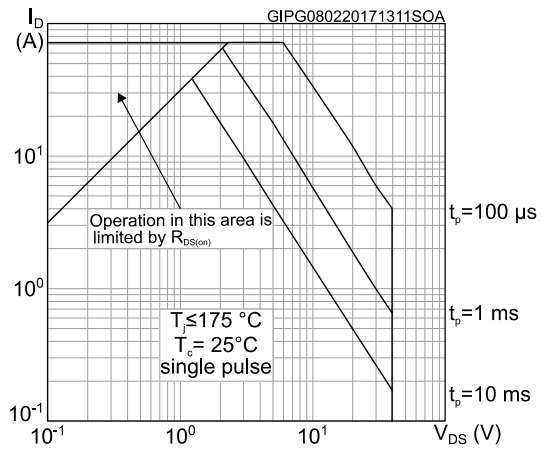


Figure 3: Thermal impedance

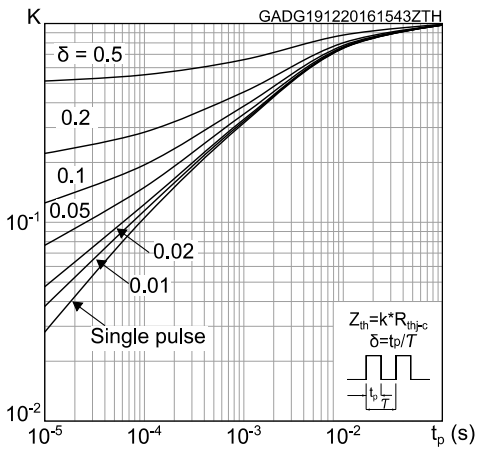


Figure 4: Output characteristics

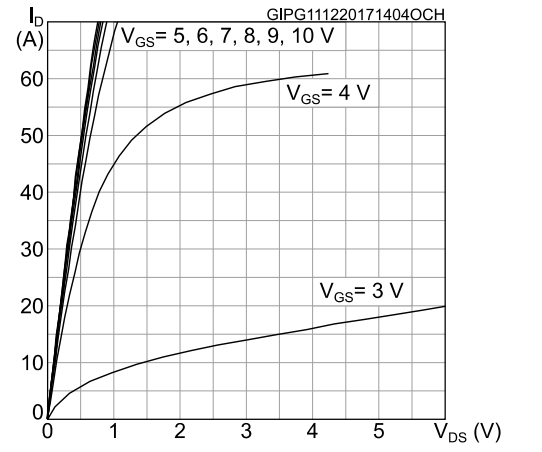


Figure 5: Transfer characteristics

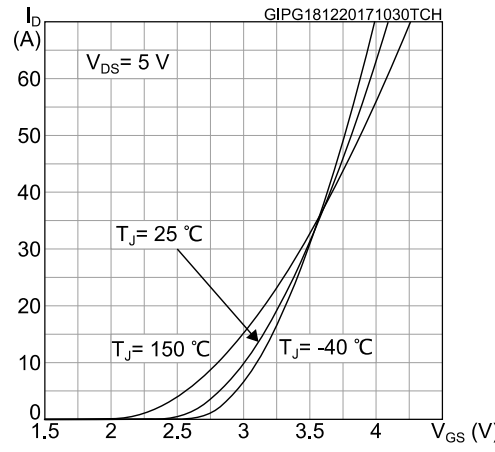


Figure 6: Gate charge vs gate-source voltage

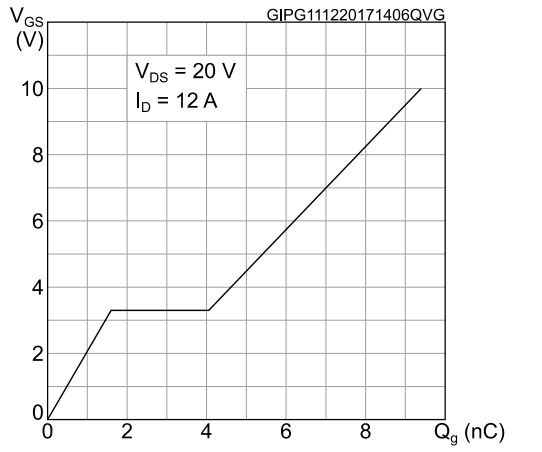


Figure 7: Static drain-source on-resistance

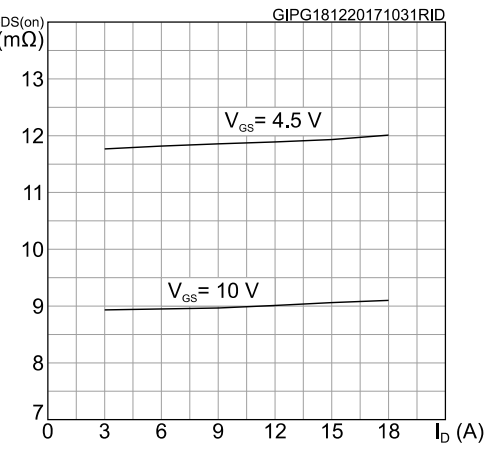


Figure 8: Capacitance variations

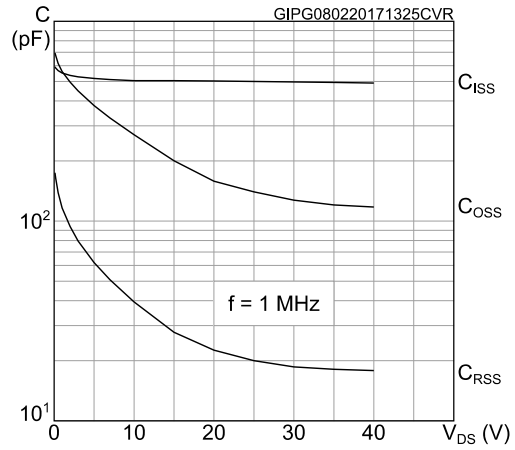


Figure 9: Normalized gate threshold voltage vs temperature

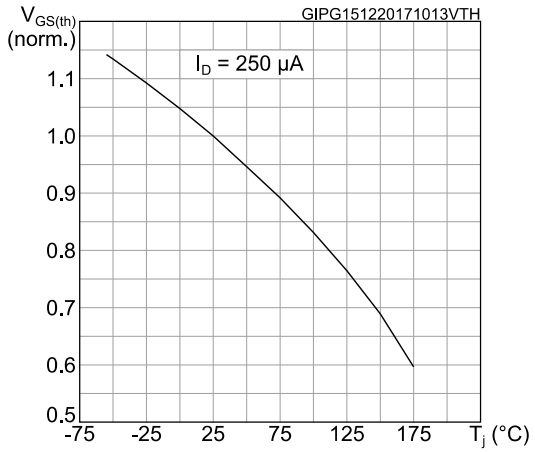


Figure 10: Normalized on-resistance vs temperature

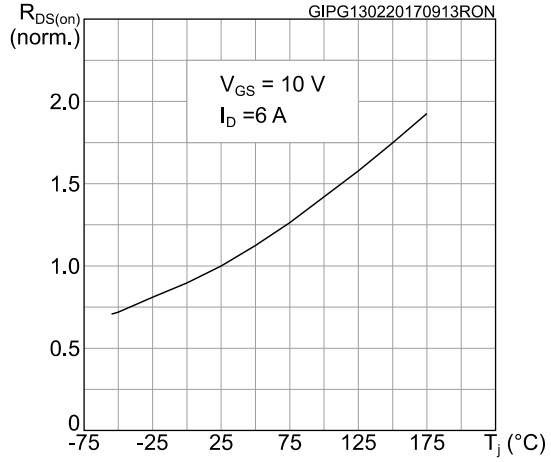


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

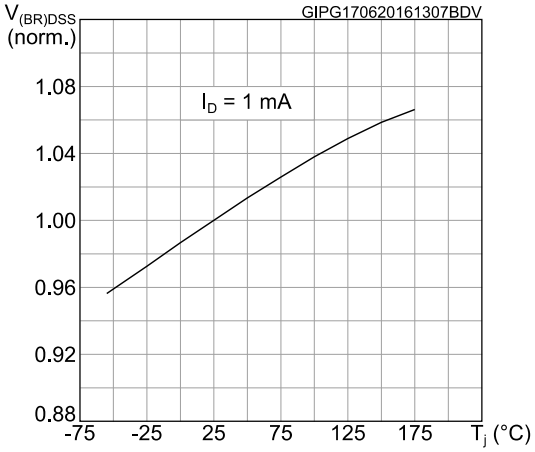
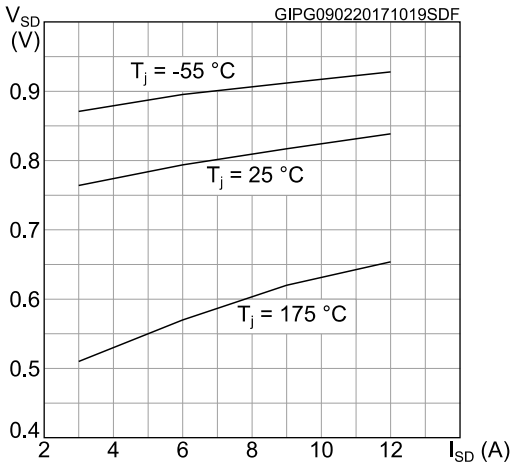


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

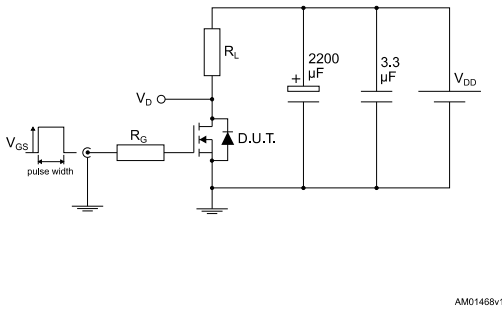


Figure 14: Test circuit for gate charge behavior

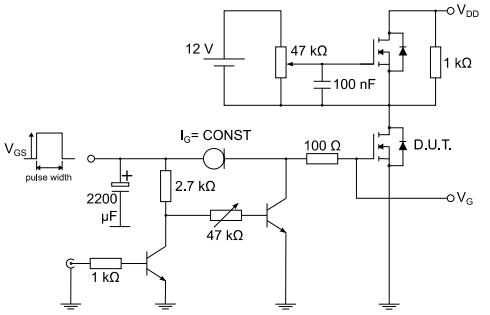


Figure 15: Test circuit for inductive load switching and diode recovery times

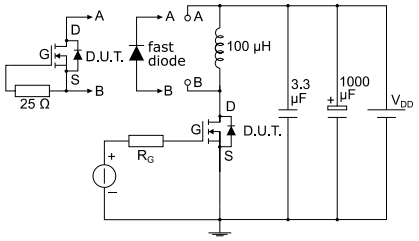


Figure 16: Unclamped inductive load test circuit

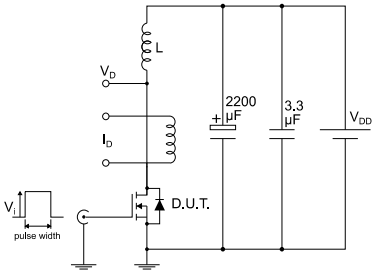


Figure 17: Unclamped inductive waveform

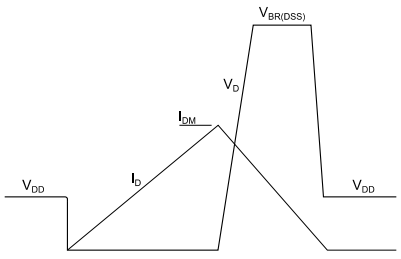
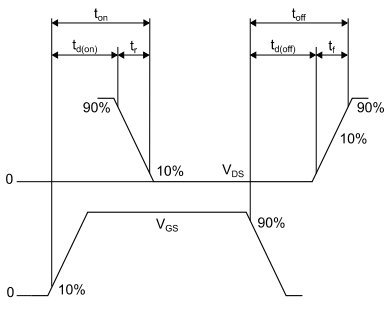


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 double island WF type R package information

Figure 19: PowerFLAT™ 5x6 double island WF type R package outline

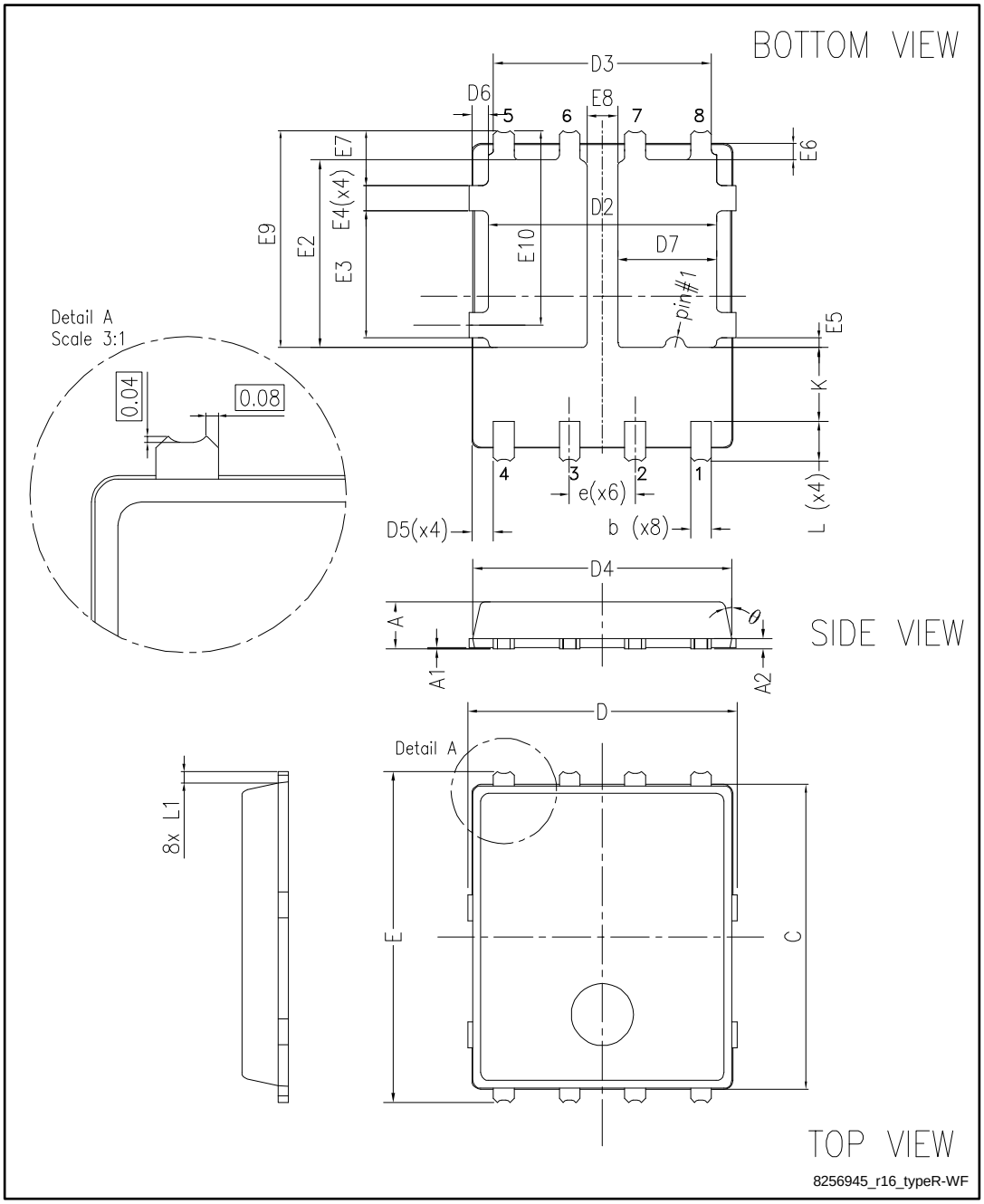
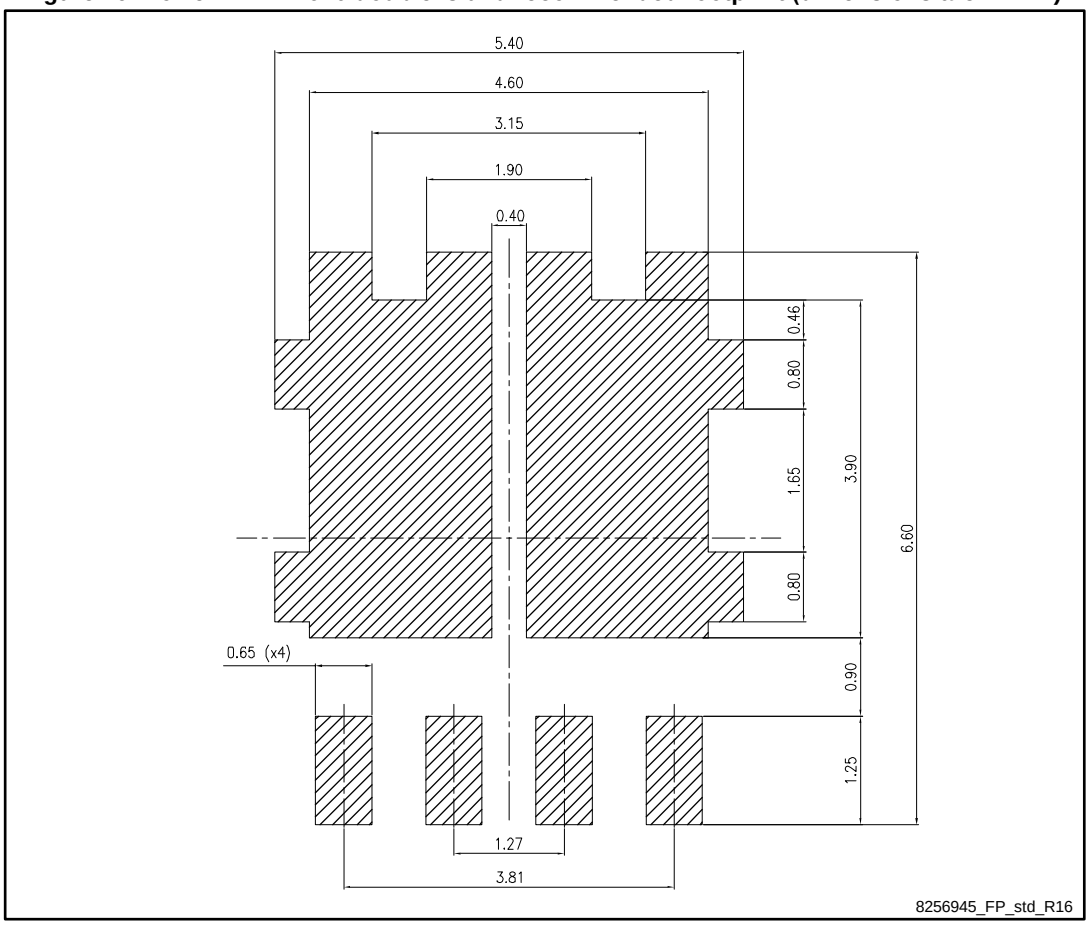


Table 8: PowerFLAT™ 5x6 double island WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
D7	1.68		1.98
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E8	0.55		0.75
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 double island recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

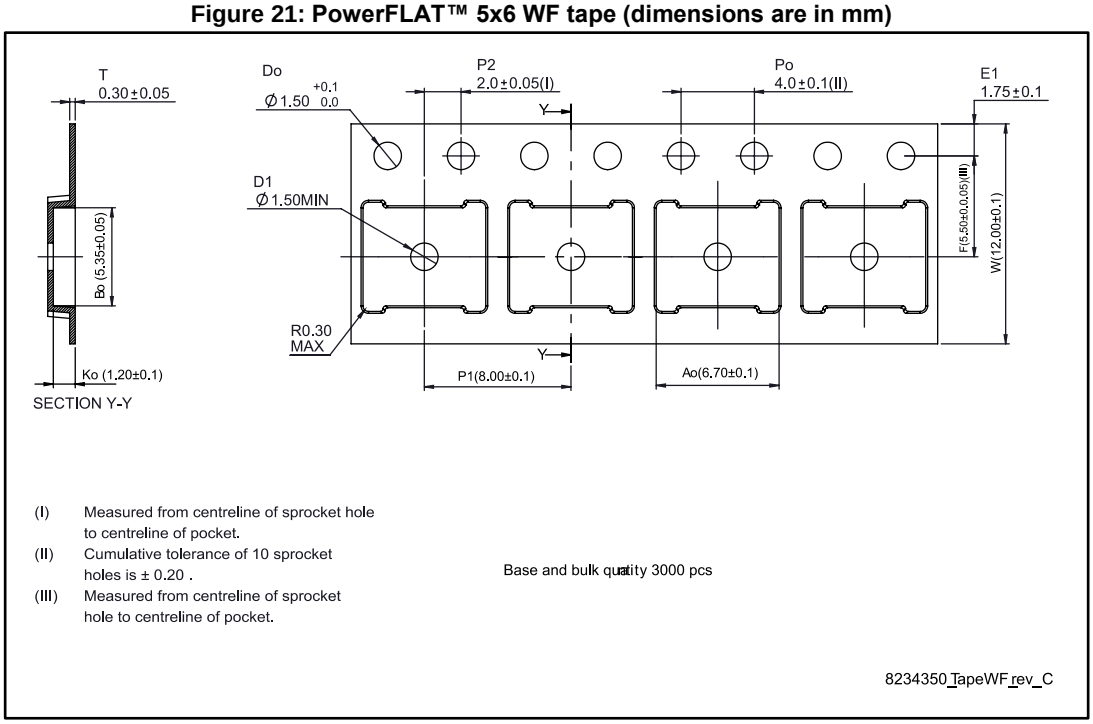


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

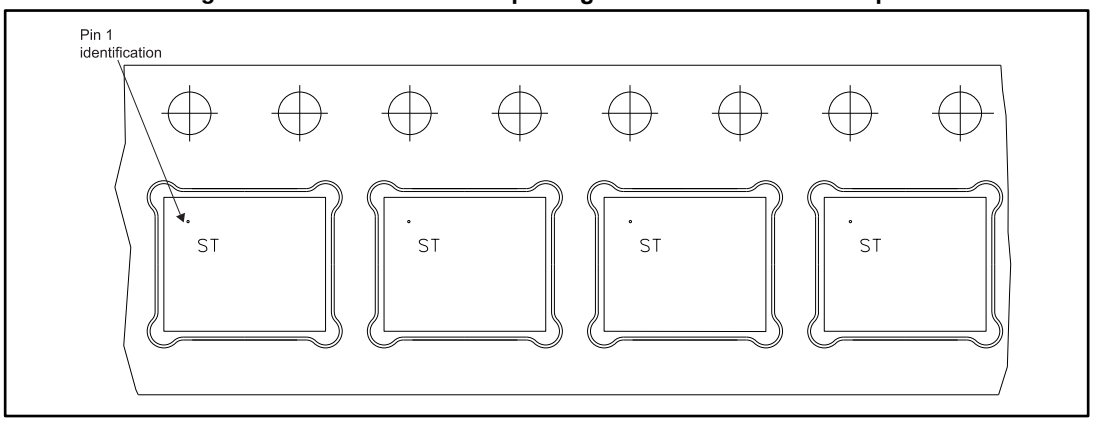
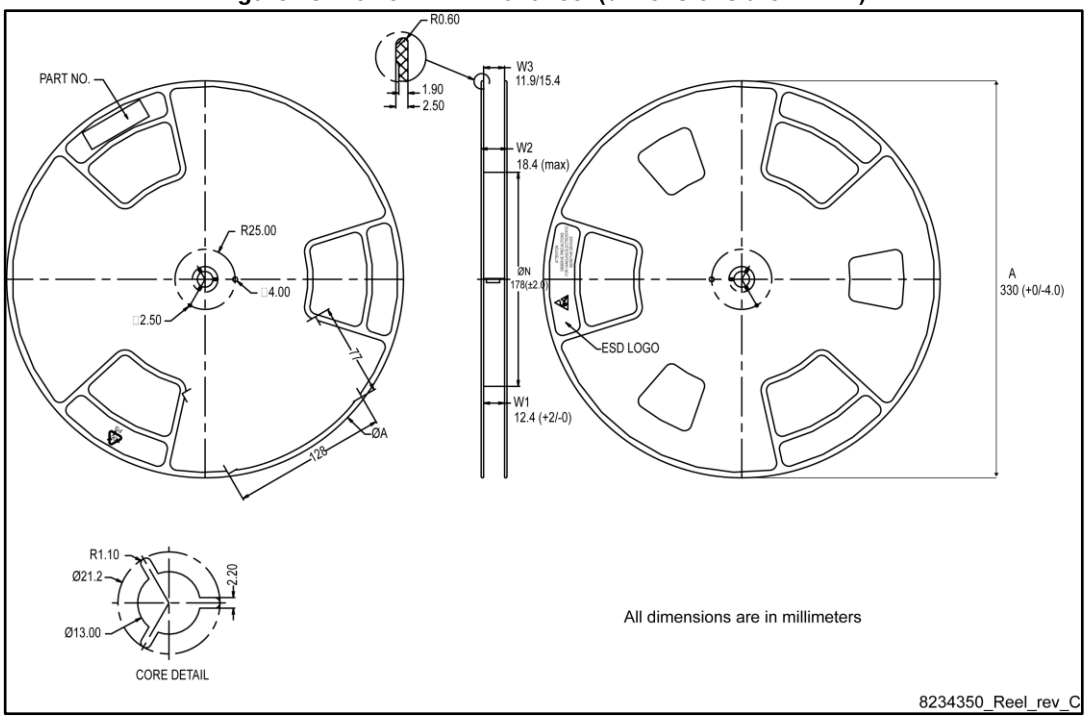


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
28-Apr-2016	1	First release.
20-Jun-2016	2	Updated *Figure 1: "Internal schematic diagram"* and *Section 7.1: "PowerFLAT™ 5x6 double island WF type R package information"* Minor text changes.
13-Sep-2016	3	Updated *Section 5: "Electrical characteristics"*
18-Dec-2017	4	Datasheet promoted from preliminary data to production data. Modified title. Modified *Table 4: "On/Off states"*, *Table 5: "Dynamic"*, *Table 6: "Switching times"* and *Table 7: "Source-drain diode"*. Added *Section 5.1: "Electrical characteristics (curves)"*. Minor text changes.

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