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# 20A User-Configurable Quad-Phase Buck Converter

# MAX77812

## General Description

The MAX77812 is a quad-phase high-efficiency step-down (buck) converter capable of delivering up to 20A of maximum current. Programmable startup/shutdown sequence and user-selectable phase configurations make the MAX77812 ideal for powering the latest generations of processors. With high-efficiency and small solution size, the MAX77812 is optimized for space constrained single-cell battery powered applications.

The MAX77812 uses an adaptive on-time PWM control scheme and it has SKIP and low-power SKIP modes for improved light-load efficiency. A programmable current limit reduces the overall solution footprint by optimizing inductors size. Differential sensing provides high output voltage accuracy, while enhanced transient response (ETR) allows fast output voltage adjustments to load transients. Programmable soft-start/stop and ramp-up/down slew rate provides control over an inrush current as the regulator transitions between operating states.

A 3.4MHz high-speed $I^2C$ or 30MHz SPI interface with dedicated logic inputs provide full configurability and control for system power optimization.

The MAX77812 is available in 3.408mm x 3.368mm, 64-bump 0.4mm pitch wafer-level package (WLP).

## Benefits and Features

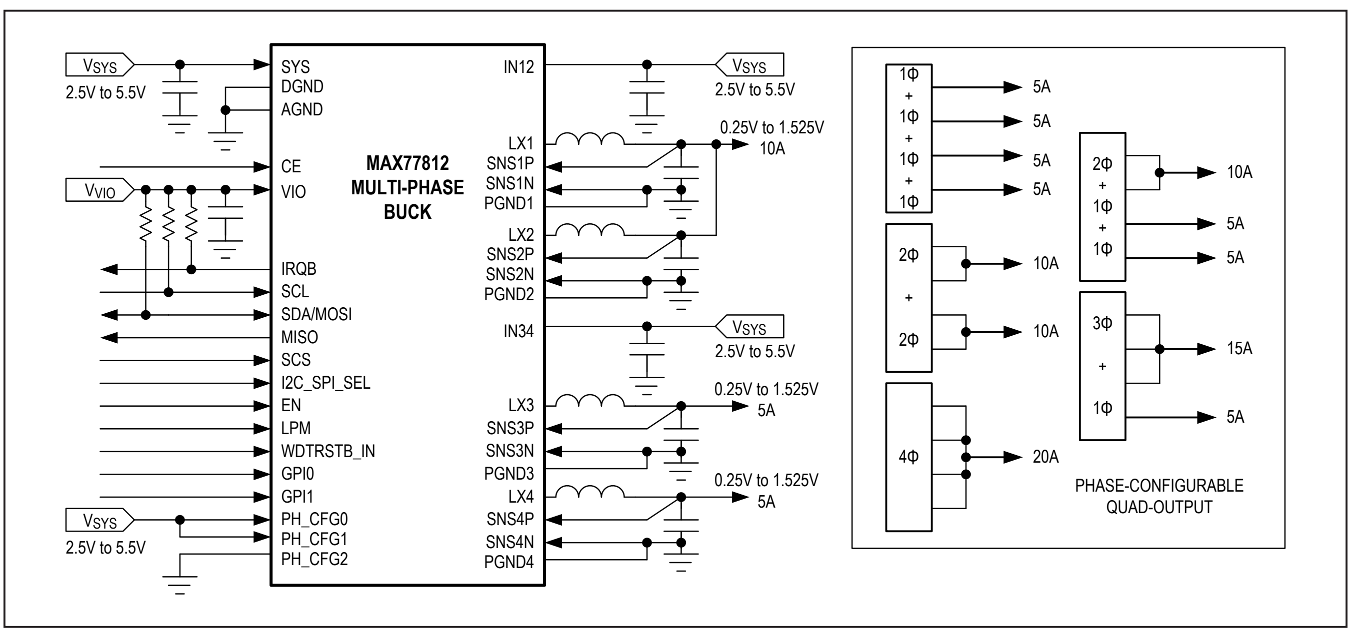
- 20A Maximum Output Current (5A per Phase)
- $V_{IN}$ Range: 2.5V to 5.5V
- $V_{OUT}$ Range: 0.250V to 1.525V with 5mV Steps
- ±0.5% Initial Output Accuracy with Differential Sensing
- 5 User-Selectable Phase Configurations
- 91% Peak Efficiency ($V_{IN}$ = 3.8V, $V_{OUT}$ = 1.1V)
- Auto (SKIP/PWM) and Forced PWM Modes
- Enhanced Load Transient Response
- Programmable Ramp-Up/Down Slew Rates
- Programmable Startup/Shutdown Sequence
- UVLO, Short-Circuit, and Thermal Protections
- 2 User-Programmable General-Purpose Inputs
- 3.4MHz High Speed $I^2C$ and 30MHz SPI Interface
- 3.408mm x 3.368mm, 64-Bump WLP Package

## Applications

- CPU/GPU, FPGAs, and DSPs Power Supply
- AR/VR Headsets and Game Consoles
- Li-ion Battery Powered Equipment
- Space Constrained Portable Electronics

***Ordering Information* appears at end of data sheet.**

## Typical Application Circuit




19-8541; Rev 12; 10/22

## Absolute Maximum Ratings

SYS, VIO to AGND.............................................-0.3V to +6.0V
DGND to AGND..................................................-0.3V to +0.3V
SCL, SDA/MOSI, MISO, SCS, IRQB, CE, EN, LPM, GPI0, GPI1,
WDTRSTB_IN to DGND..................... -0.3V to ($V_{VIO}$ + 0.3V)
PH_CFG0, PH_CFG1, PH_CFG2,
I2C_SPI_SEL to AGND ..................... -0.3V to ($V_{SYS}$ + 0.3V)
IN12, IN34 to PGNDx............................ -0.3V to ($V_{SYS}$ + 0.3V)
LX1/2/3/4 to PGNDx................................-0.3V to ($V_{IN\_}$ + 0.3V)
LX1/2/3/4 to PGNDx (Pulsed <10ns Voltage)......-3.0V to +7.0V
PGND1/2/3/4 to AGND........................................-0.3V to +0.3V
SNS1P, SNS2P, SNS3P, SNS4P to AGND ..-0.3V to ($V_{IN\_}$ + 0.3V)
SNS1N, SNS2N, SNS3N, SNS4N to AGND........-0.3V to +0.3V
Continuous Power Dissipation at $T_A$ = +70°C
(derate 26.17mW/°C above +70°C) .........................2094mW
Junction Temperature.................................................. +150°C
Storage Temperature Range........................... -65°C to +150°C
Soldering Temperature (reflow).....................................+260°C

**Note 1:** LXx node has internal clamp diodes to PGNDx and INx. Applications that give forward bias to these diodes should ensure that the total power loss does not exceed the power dissipation limit of IC package.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Recommended Operating Conditions

| PARAMETER | SYMBOL | CONDITION | TYPICAL RANGE | UNITS |
|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | 2.5 to 5.5 | V |
| Output Current Range | $I_{OUT}$ | For continuous operation at 5A (per phase), the junction temperature ($T_J$) is limited to +115°C. If the junction temperature is higher than +115°C, the expected lifetime at 5A continuous operation is reduced | 0 to 5 | A |
| Junction Temperature Range | $T_J$ | | -40 to +125 | °C |

**Note:** These limits are not guaranteed.

## Package Thermal Characteristics (Note 2)

WLP
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .......33.2°C/W

**Note 2:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

## Electrical Characteristics

### Top-Level Electrical Characteristics

($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{VIO}$ = +1.8V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **GLOBAL INPUT SUPPLY** | | | | | | |
| Operating Voltage Range | $V_{SYS}$ | | 2.5 | | 5.5 | V |
| Shutdown Supply Current | $I_{SHDN}$ | CE = low, $T_A$ = +25°C | | 2 | 5 | µA |
| Standby Current | $I_{STBY}$ | CE = high and all outputs are off, $T_A$ = +25°C | | 25 | | µA |

## Electrical Characteristics (continued)

### Top-Level Electrical Characteristics (continued)

($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{VIO}$ = +1.8V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| No Load Supply Current in Low Power Skip Mode | $I_{LP\_SKIP1}$ | 4-phase configuration (no switching) | | 120 | | µA |
| | $I_{LP\_SKIP2}$ | 3 + 1-phase configuration (no switching) | | 190 | | |
| | $I_{LP\_SKIP3}$ | 2 + 2-phase configuration (no switching) | | 190 | | |
| | $I_{LP\_SKIP4}$ | 2 + 1 + 1-phase configuration (no switching) | | 265 | | |
| | $I_{LP\_SKIP5}$ | 1 + 1 + 1 + 1-phase configuration (no switching) | | 340 | 510 | |
| No Load Supply Current in Skip Mode | $I_{SKIP1}$ | 4-phase configuration (no switching) | | 150 | | µA |
| | $I_{SKIP2}$ | 3 + 1-phase configuration (no switching) | | 250 | | |
| | $I_{SKIP3}$ | 2 + 2-phase configuration (no switching) | | 250 | | |
| | $I_{SKIP4}$ | 2 + 1 + 1-phase configuration (no switching) | | 350 | | |
| | $I_{SKIP5}$ | 1 + 1 + 1 + 1-phase configuration (no switching) | | 460 | 690 | |
| No Load Supply Current in Skip Mode with ETR | $I_{SKIP\_ETR1}$ | 4-phase configuration (no switching, ETR enabled) | | 180 | | µA |
| | $I_{SKIP\_ETR2}$ | 3 + 1-phase configuration (no switching, ETR enabled) | | 310 | | |
| | $I_{SKIP\_ETR3}$ | 2 + 2-phase configuration (no switching, ETR enabled) | | 310 | | |
| | $I_{SKIP\_ETR4}$ | 2 + 1 + 1-phase configuration (no switching, ETR enabled) | | 440 | | |
| | $I_{SKIP\_ETR5}$ | 1 + 1 + 1 + 1-phase configuration (no switching, ETR enabled) | | 580 | 870 | |
| **$V_{SYS}$ UNDERVOLTAGE LOCKOUT** | | | | | | |
| $V_{SYS}$ Undervoltage Lockout Threshold | $V_{UVLO\_R}$ | $V_{SYS}$ rising | 2.375 | 2.50 | 2.625 | V |
| | $V_{UVLO\_F}$ | $V_{SYS}$ falling (default) | | 2.15 | | |
| **THERMAL PROTECTION** | | | | | | |
| Thermal Protection Threshold | $T_{SHDN}$ | $T_J$ rising, 15°C hysteresis | | 165 | | °C |
| Thermal Interrupt at 120°C | $T_{INT120}$ | $T_J$ rising, 15°C hysteresis | | 120 | | °C |
| Thermal Interrupt at 140°C | $T_{INT140}$ | $T_J$ rising, 15°C hysteresis | | 140 | | °C |

## Electrical Characteristics (continued)

### Top-Level Electrical Characteristics (continued)

($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{VIO}$ = +1.8V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **LOGIC AND CONTROL INPUTS** | | | | | | |
| Input Low Level | $V_{IL}$ | PH_CFG0, PH_CFG1, PH_CFG2, I2C_SPI_SEL, $V_{SYS}$ ≤ 5.5V, $T_A$ = +25°C | | | 0.4 | V |
| | | CE, EN, LPM, GPI0, GPI1, WDTRSTB_IN, $T_A$ = +25°C | | | 0.3 x $V_{VIO}$ | |
| Input High Level | $V_{IH}$ | PH_CFG0, PH_CFG1, PH_CFG2, I2C_SPI_SEL, $V_{SYS}$ ≤ 5.5V, $T_A$ = +25°C | 1.2 | | | V |
| | | CE, EN, LPM, GPI0, GPI1, WDTRSTB_IN, $T_A$ = +25°C | 0.7 x $V_{VIO}$ | | | |
| Logic Input Leakage Current | $I_{LK}$ | PH_CFG0, PH_CFG1, PH_CFG2, I2C_SPI_SEL, $V_{SYS}$ = 5.5V, CE = 1.8V, $T_A$ = +25°C | -1 | +0.001 | +1 | µA |
| | | CE, EN, LPM, GPI0, GPI1, CE = 1.8V, $T_A$ = +25°C | -1 | +0.001 | +1 | |
| | | PH_CFG0, PH_CFG1, PH_CFG2, I2C_SPI_SEL, $V_{SYS}$ = 5.5V, CE = 1.8V, $T_A$ = +85°C (Note 4) | | 0.1 | | |
| | | CE, EN, LPM, GPI0, GPI1, CE = 1.8V, $T_A$ = +85°C (Note 4) | | 0.1 | | |
| $\overline{IRQ}$ Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 1mA | | | 0.4 | V |
| $\overline{IRQ}$ Output High Leakage | $I_{LK\_OH}$ | $T_A$ = +25°C | -1 | 0.001 | +1 | µA |
| | | $T_A$ = +85°C (Note 4) | | 0.1 | | |
| **INTERNAL PULL-UP/DOWN RESISTANCE** | | | | | | |
| WDTRSTB_IN Pullup Resistance | $R_{PU}$ | Pullup resistance to VIO | 400 | 800 | 1600 | kΩ |
| GPI0, GPI1, EN, LPM Pulldown Resistance | $R_{PD}$ | Pulldown resistance to DGND | 400 | 800 | 1600 | kΩ |

## Electrical Characteristics (continued)

### Quad-Phase Buck Electrical Characteristics

($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{OUTx}$ = 0.85V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Input Voltage Range | $V_{INx}$ | | 2.5 | | $V_{SYS}$ | V |
| Output Voltage Range | $V_{OUT}$ | Programmable with 8-bit resolution, 5mV/LSB | 0.25 | | 1.525 | V |
| **DC OUTPUT VOLTAGE ACCURACY** | | | | | | |
| Output Voltage Accuracy | $V_{ACC\_INIT}$ | Force PWM mode, differential remote sensing, $V_{OUT}$ ≥ 0.65V, $I_{OUT}$ = 0mA, $C_{OUT(EFF)}$ = 64µF, $T_A$ = +25°C | -0.5 | | +0.5 | % |
| | | Force PWM mode, differential remote sensing, 0.45V ≤ $V_{OUT}$ < 0.6V, $I_{OUT}$ = 0mA, $C_{OUT(EFF)}$ = 64µF, $T_A$ = +25°C | -6 | | +6 | mV |
| Load Regulation | | Forced PWM mode, differential remote sensing, $I_{OUT}$ = 0A to 5A, $C_{OUT(EFF)}$ = 64µF (Note 5) | | -0.001 | | V/A |
| Line Regulation | | Forced PWM mode, differential remote sensing, $V_{INx}$ = 2.5V to 5.5V, $V_{OUT}$ = Default, $I_{OUT}$ = 0mA, $C_{OUT(EFF)}$ = 64µF | -0.005 | | +0.005 | V/V |
| **AC OUTPUT VOLTAGE ACCURACY** | | | | | | |
| Line Transient Response | $V_{DROOP}$ | $V_{INx}$ = 3.4V to 2.9V to 3.4V, $t_{RISE}$ = $t_{FALL}$ = 10µs, $V_{OUT}$ = 1.1V, $I_{OUT}$ = 2A, L = 220nH (DCR = 9mΩ), $C_{OUT(EFF)}$ = 16µF (ESR = 5mΩ, ESL = 300pH) per phase (Note 5) | | 15 | | mV |
| Load Transient Response | $V_{DROOP}$ | SKIP/PWM mode, differential remote sensing, $V_{OUT}$ = 1.1V, $I_{OUT}$ = 0.1A to 4A (100A/µs), L = 220nH (DCR = 9mΩ), $C_{OUT(EFF)}$ = 16µF (ESR = 5mΩ, ESL = 300pH) per Phase (Note 5) | | 45 | | mV |

## Electrical Characteristics (continued)

### Quad-Phase Buck Electrical Characteristics (continued)

($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{OUTx}$ = 0.85V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **RAMP RATE** | | | | | | |
| Soft-Start Slew Rate | | B_SS_SR[2:0] = 000b (Note 6) | | 1.25 | | mV/µs |
| | | B_SS_SR[2:0] = 001b (Note 6) | | 2.5 | | |
| | | B_SS_SR[2:0] = 010b (Note 6) | | 5 | | |
| | | B_SS_SR[2:0] = 011b (Note 6) | | 10 | | |
| | | B_SS_SR[2:0] = 100b (default) (Note 6) | | 20 | | |
| | | B_SS_SR[2:0] = 101b (Note 6) | | 40 | | |
| | | B_SS_SR[2:0] = 110b or 111b (Note 6) | | 60 | | |
| Shutdown Slew Rate | | B_SD_SR[2:0] = 000b (Note 6) | | 1.25 | | mV/µs |
| | | B_SD_SR[2:0] = 001b (Note 6) | | 2.5 | | |
| | | B_SD_SR[2:0] = 010b (default) (Note 6) | | 5 | | |
| | | B_SD_SR[2:0] = 011b (Note 6) | | 10 | | |
| | | B_SD_SR[2:0] = 100b (Note 6) | | 20 | | |
| | | B_SD_SR[2:0] = 101b (Note 6) | | 40 | | |
| | | B_SD_SR[2:0] = 110b or 111b (Note 6) | | 60 | | |

## Electrical Characteristics (continued)

### Quad-Phase Buck Electrical Characteristics (continued)

($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{OUTx}$ = 0.85V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| DVS Ramp-Up Slew Rate | | B_RU_SR[2:0] = 000b (Note 6) | | 1.25 | | mV/µs |
| | | B_RU_SR[2:0] = 001b (Note 6) | | 2.5 | | |
| | | B_RU_SR[2:0] = 010b (Note 6) | | 5 | | |
| | | B_RU_SR[2:0] = 011b (Note 6) | | 10 | | |
| | | B_RU_SR[2:0] = 100b (default) (Note 6) | | 20 | | |
| | | B_RU_SR[2:0] = 101b (Note 6) | | 40 | | |
| | | B_RU_SR[2:0] = 110b or 111b (Note 6) | | 60 | | |
| DVS Ramp-Down Slew Rate | | B_RD_SR[2:0] = 000b (Note 6) | | 1.25 | | mV/µs |
| | | B_RD_SR[2:0] = 001b (Note 6) | | 2.5 | | |
| | | B_RD_SR[2:0] = 010b (default) (Note 6) | | 5 | | |
| | | B_RD_SR[2:0] = 011b (Note 6) | | 10 | | |
| | | B_RD_SR[2:0] = 100b (Note 6) | | 20 | | |
| | | B_RD_SR[2:0] = 101b (Note 6) | | 40 | | |
| | | B_RD_SR[2:0] = 110b or 111b (Note 6) | | 60 | | |
| Turn-On Delay Time | $t_{ON\_DLY1}$ | From EN signal to LXB switching with bias on (Note 6) | | 30 | | µs |
| | $t_{ON\_DLY2}$ | From EN signal to LXB switching with bias off (Note 5) | | 85 | | |

## Electrical Characteristics (continued)

### Quad-Phase Buck Electrical Characteristics (continued)

($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{OUTx}$ = 0.85V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER STAGE** | | | | | | |
| Maximum Output Current | $I_{OUT(MAX)}$ | RMS current per phase, $V_{IN}$ < 3.2V (Note 5) | | 4000 | | mA |
| | $I_{OUT(MAX)}$ | RMS current per phase, 3.2V ≤ $V_{IN}$ ≤ 5.5V (Note 5) | | 5000 | | |
| PMOS Peak Current Limit | $I_{PLIM}$ | Mx_ILIM[2:0] = 000b | | 3000 | | mA |
| | $I_{PLIM}$ | Mx_ILIM[2:0] = 001b | | 3600 | | |
| | $I_{PLIM}$ | Mx_ILIM[2:0] = 010b | | 4200 | | |
| | $I_{PLIM}$ | Mx_ILIM[2:0] = 011b | | 4800 | | |
| | $I_{PLIM}$ | Mx_ILIM[2:0] = 100b | | 5400 | | |
| | $I_{PLIM}$ | Mx_ILIM[2:0] = 101b (default) | 4800 | 6000 | 7200 | |
| | $I_{PLIM}$ | Mx_ILIM[2:0] = 110b | | 6600 | | |
| | $I_{PLIM}$ | Mx_ILIM[2:0] = 111b | 5200 | 7200 | 9200 | |
| NMOS Valley Current Limit | $I_{VLIM}$ | Mx_ILIM[2:0] = 000b | | 2000 | | mA |
| | $I_{VLIM}$ | Mx_ILIM[2:0] = 001b | | 2400 | | |
| | $I_{VLIM}$ | Mx_ILIM[2:0] = 010b | | 2800 | | |
| | $I_{VLIM}$ | Mx_ILIM[2:0] = 011b | | 3200 | | |
| | $I_{VLIM}$ | Mx_ILIM[2:0] = 100b | | 3600 | | |
| | $I_{VLIM}$ | Mx_ILIM[2:0] = 101b (default) | 3200 | 4000 | 4800 | |
| | $I_{VLIM}$ | Mx_ILIM[2:0] = 110b | | 4400 | | |
| | $I_{VLIM}$ | Mx_ILIM[2:0] = 111b | 3800 | 4800 | 5800 | |
| NMOS Negative Current Limit | $I_{NLIM}$ | Per phase | -2000 | -1500 | -1000 | mA |
| Switching Frequency | $f_{SW}$ | $V_{OUT}$ = default, Forced PWM mode | 1.6 | 2.0 | 2.8 | MHz |
| High-Side PMOS On-Resistance | $R_{DSON(PMOS)}$ | INx to LXx, $I_{LXx}$ = -150mA | | 32 | 70 | mΩ |
| Low-Side NMOS On-Resistance | $R_{DSON(NMOS)}$ | LXx to PGNDx, $I_{LXx}$ = 150mA | | 15 | 29 | mΩ |
| LX Active Discharge Resistance | $R_{AD\_LX}$ | Resistance from LXx to PGNDx, per phase, output disabled | | 100 | 200 | Ω |

## Electrical Characteristics (continued)

### Quad-Phase Buck Electrical Characteristics (continued)

($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{OUTx}$ = 0.85V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| LX Leakage Current | $I_{LKG\_LX}$ | $V_{LXx}$ = 0V or 5.5V, $T_A$ = +25°C | -1 | 0.1 | +1 | µA |
| | $I_{LKG\_LX}$ | $V_{LXx}$ = 0V or 5.5V, $T_A$ = +85°C (Note 4) | | 1 | | |
| Nominal Inductance | $L_{NOM}$ | (Note 5) | | 220 | | nH |
| Minimum Effective Output Capacitance | $C_{OUT(EFF\_MIN)}$ | 0µA < $I_{OUT}$ < 5000mA per phase (Note 5) | | 16 | | µF |
| **EFFICIENCY AND OUTPUT RIPPLE** | | | | | | |
| Peak Efficiency | $\eta_{PK}$ | L = 220nH (DCR = 9mΩ), $C_{OUT(EFF)}$ = 16µF (ESR = 5mΩ, ESL = 300pH) per Phase (Note 5) | | 90 | | % |
| Heavy Load Efficiency | $\eta_{HEAVY}$ | $I_{OUT}$ = 5A, L = 220nH (DCR = 9mΩ), $C_{OUT(EFF)}$ = 16µF (ESR = 5mΩ, ESL = 300pH) per Phase (Note 5) | | 75 | | % |
| Skip Mode Output Ripple | $V_{RIP\_SKIP}$ | Skip mode, $I_{OUT}$ = 0.1A, L = 220nH (DCR = 9mΩ), $C_{OUT(EFF)}$ = 16µF (ESR = 5mΩ, ESL = 300pH) per phase (Note 7) | | 10 | | $mV_{P-P}$ |
| FPWM Mode Output Ripple | $V_{RIP\_FPWM}$ | Forced PWM mode, differential remote sensing, $I_{OUT}$ = 0.1A, L = 220nH (DCR = 9mΩ), $C_{OUT(EFF)}$ = 16µF (ESR = 5mΩ, ESL = 300pH) per phase (Note 7) | | 5 | | $mV_{P-P}$ |
| **POWER OK COMPARATOR** | | | | | | |
| Output POK Trip Level | | Rising threshold | | 90 | | % |
| | | Falling threshold | | 85 | 90 | |

## Electrical Characteristics (continued)

### I²C Electrical Characteristics

($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{VIO}$ = +1.8V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| VIO Supply Voltage Range | $V_{VIO}$ | | 1.65 | 1.8 | $V_{SYS}$ | V |
| VIO Dynamic Supply Current | $I_{VIO}$ | $f_{SCL}$ = $f_{SDA}$ = 1MHz | | 50 | | µA |
| $V_{SYS}$ Dynamic Supply Current | $I_{SYS}$ | | | 5 | | µA |
| **SDA AND SCL I/O STAGES** | | | | | | |
| SCL, SDA Input High Voltage | $V_{IH}$ | | 0.7 x $V_{VIO}$ | | | V |
| SCL, SDA Input Low Voltage | $V_{IL}$ | | | | 0.3 x $V_{VIO}$ | V |
| SCL, SDA Input Hysteresis | $V_{HYS}$ | | | 0.05 x $V_{VIO}$ | | V |
| SCL, SDA Input Hysteresis in HS Mode | $V_{HYS\_HS}$ | | | 0.1 x $V_{VIO}$ | | V |
| SDA Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 5mA | | | 0.4 | V |
| SCL, SDA Input Capacitance | $C_I$ | | | 10 | | pF |
| SCL, SDA Input Leakage Current | $I_{LK}$ | $T_A$ = +25°C | -1 | +0.001 | +1 | µA |
| | | $T_A$ = +85°C (Note 4) | | 0.1 | | |
| **I²C-COMPATIBLE INTERFACE TIMING (STANDARD, FAST AND FAST MODE PLUS) (Note 5)** | | | | | | |
| Clock Frequency | $f_{SCL}$ | | 0 | | 1000 | kHz |
| Bus Free Time between STOP and START Condition | $t_{BUSF}$ | | 0.5 | | | µs |
| Hold Time (REPEATED) START Condition | $t_{HD\_START}$ | | 0.26 | | | µs |
| SCL Low Period | $t_{LOW}$ | | 0.5 | | | µs |
| SCL High Period | $t_{HIGH}$ | | 0.26 | | | µs |
| Setup Time REPEATED START Condition | $t_{SU\_START}$ | | 0.26 | | | µs |
| Data Hold Time | $t_{HD\_DATA}$ | Transmit mode | 0 | | 450 | ns |
| Data Setup Time | $t_{SU\_DATA}$ | | 50 | | | ns |
| SCL, SDA Receiving Rise Time | $t_{R\_REV}$ | | | | 120 | ns |
| SCL, SDA Receiving Fall Time | $t_{F\_REV}$ | | 20 x $V_{VIO}$/5.5 | | 120 | ns |

## Electrical Characteristics (continued)

### I2C Electrical Characteristics (continued)

($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{VIO}$ = +1.8V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SCL, SDA Transmitting Fall Time | $t_{F\_TRA}$ | | 20 x $V_{VIO}$/5.5 | | 120 | ns |
| Setup Time for STOP Condition | $t_{SU\_STOP}$ | | 0.26 | | | µs |
| Data Valid Time | $t_{VD\_DATA}$ | | | | 450 | ns |
| Data Valid Acknowledge Time | $t_{VD\_ACK}$ | | | | 450 | ns |
| Bus Capacitance | $C_B$ | | | | 550 | pF |
| Pulse Width of Suppressed Spikes | $t_{SP}$ | | | | 50 | ns |
| **I2C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, $C_B$ = 100pF) (Note 5)** | | | | | | |
| Clock Frequency | $f_{SCL}$ | | | | 3.4 | MHz |
| Hold Time (REPEATED) START Condition | $t_{HD\_START}$ | | 160 | | | ns |
| SCL LOW Period | $t_{LOW}$ | | 160 | | | ns |
| SCL HIGH Period | $t_{HIGH}$ | | 60 | | | ns |
| Setup Time REPEATED START Condition | $t_{SU\_START}$ | | 160 | | | ns |
| Data Hold Time | $t_{HD\_DATA}$ | | 0 | | 70 | ns |
| Data Setup Time | $t_{SU\_DATA}$ | | 10 | | | ns |
| SCL Rise Time | $t_{R\_SCL}$ | $T_A$ = +25°C | 10 | | 40 | ns |
| SCL Rise Time after REPEATED START Condition and after Acknowledge Bit | $t_{R\_SCL1}$ | $T_A$ = +25°C | 10 | | 40 | ns |
| SCL Fall Time | $t_{F\_SCL}$ | $T_A$ = +25°C | 10 | | 40 | ns |
| SDA Rise Time | $t_{R\_SDA}$ | $T_A$ = +25°C | 10 | | 40 | ns |
| SDA Fall Time | $t_{F\_SDA}$ | $T_A$ = +25°C | | | 40 | ns |
| Setup Time for STOP Condition | $t_{SU\_STOP}$ | | 160 | | | ns |
| Bus Capacitance | $C_B$ | | | | 100 | pF |
| Pulse Width of Suppressed Spikes | $t_{SP}$ | | 0 | | 10 | ns |

## Electrical Characteristics (continued)

### I²C Electrical Characteristics (continued)

($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{VIO}$ = +1.8V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **I²C-COMPATIBLE INTERFACE TIMING (HIGH-SPEED MODE, $C_B$ = 400pF) (Note 5)** | | | | | | |
| Clock Frequency | $f_{SCL}$ | | | | 1.7 | MHz |
| Hold Time (REPEATED) START Condition | $t_{HD\_START}$ | | 160 | | | ns |
| SCL Low Period | $t_{LOW}$ | | 320 | | | ns |
| SCL High Period | $t_{HIGH}$ | | 120 | | | ns |
| Setup Time REPEATED START Condition | $t_{SU\_START}$ | | 160 | | | ns |
| DATA Hold Time | $t_{HD\_DATA}$ | | 0 | | 150 | ns |
| DATA Setup Time | $t_{SU\_DATA}$ | | 10 | | | ns |
| SCL Rise Time | $t_{R\_SCL}$ | $T_A$ = +25°C | 20 | | 80 | ns |
| SCL Rise Time after REPEATED START Condition and after Acknowledge Bit | $t_{R\_SCL1}$ | $T_A$ = +25°C | 20 | | 80 | ns |
| SCL Fall Time | $t_{F\_SCL}$ | $T_A$ = +25°C | 20 | | 80 | ns |
| SDA Rise Time | $t_{R\_SDA}$ | $T_A$ = +25°C | 20 | | 80 | ns |
| SDA Fall Time | $t_{F\_SDA}$ | $T_A$ = +25°C | | | 80 | ns |
| Setup Time for STOP Condition | $t_{SU\_STOP}$ | | 160 | | | ns |
| Bus Capacitance | $C_B$ | | | | 400 | pF |
| Pulse Width of Suppressed Spikes | $t_{SP}$ | | 0 | | 10 | ns |

## Electrical Characteristics (continued)

### SPI Electrical Characteristics

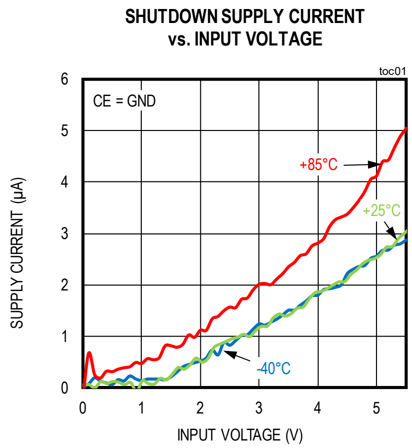
($V_{SYS}$ = $V_{INx}$ = +3.8V, $V_{VIO}$ = +1.8V, $T_A$ = $T_J$ = -40°C to +125°C, typical values are at $T_A$ = $T_J$ = +25°C)

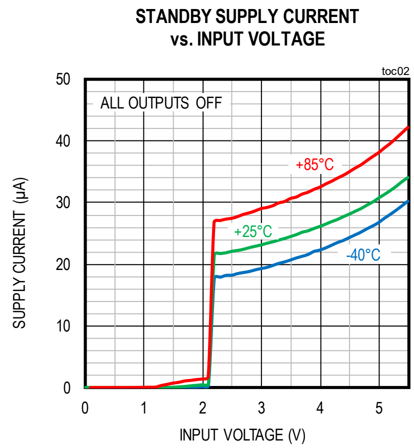
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY AND I/O STAGES** | | | | | | |
| VIO Supply Voltage Range | $V_{VIO}$ | | 1.65 | 1.8 | $V_{SYS}$ | V |
| Input Leakage Current (SCS, SCL, MOSI) | $I_{IH\_SPI}$, $I_{IL\_SPI}$ | $T_A$ = +25°C | -1 | +0.001 | +1 | µA |
| | | $T_A$ = +85°C (Note 4) | | 0.1 | | |
| Input Capacitance (SCS, SCL, MOSI) | $C_I$ | | | 10 | | pF |
| Input LOW Voltage (SCS, SCL, MOSI) | $V_{IL}$ | | | | 0.3 x $V_{VIO}$ | V |
| Input HIGH Voltage (SCS, SCL, MOSI) | $V_{IH}$ | | 0.7 x $V_{VIO}$ | | | V |
| Input Hysteresis (SCS, SCL, MOSI) | $V_{HYS}$ | | | 0.1 x $V_{VIO}$ | | |
| MISO Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 1mA | | | 0.2 | V |
| MISO Output High Voltage | $V_{OH}$ | $I_{OH}$ = 1mA | $V_{VIO}$ - 0.2 | | | V |
| MISO Leakage Current | $I_{LK\_HIZ}$ | High-impedance state, $T_A$ = +25°C | -1 | +0.001 | +1 | µA |
| | | High-impedance state, $T_A$ = +85°C (Note 4) | | 0.1 | | |
| **SPI INTERFACE TIMING (Note 5)** | | | | | | |
| SPI Operating Frequency | $f_{SCL}$ | | | 26 | 30 | MHz |
| MOSI Input Valid to SCL Rising Edge | $t_{SU\_MOSI}$ | | 10 | | | ns |
| MOSI Input Valid from SCL Rising Edge | $t_{HD\_MOSI}$ | | 10 | | | ns |
| MISO Valid from SCL Rising Edge | $t_{D\_MISO}$ | $C_L$ = 50pF | | 9 | | ns |
| MISO Rising/Falling Time | $t_R$, $t_F$ | $C_L$ = 20pF | | | 10 | ns |
| SCS Setup Time | $t_{SU\_SCS}$ | | 20 | | | ns |
| SCS Hold Time | $t_{HD\_SCS}$ | | 20 | | | ns |
| Minimum SCS High Pulse Width | $t_{SCS\_H(MIN)}$ | | 50 | | | ns |

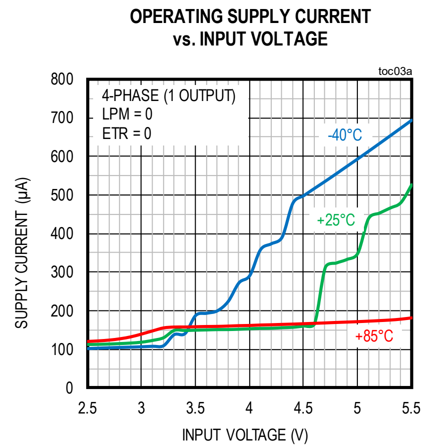
**Note 3:** Limits are 100% production tested at $T_A$ = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.
**Note 4:** Guaranteed by ATE characterization. Not directly tested in production.
**Note 5:** Guaranteed by design. Not production tested.
**Note 6:** Guaranteed by design. Production tested through scan.
**Note 7:** Internal design target.

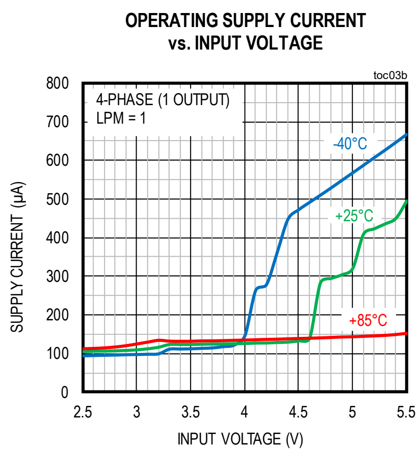
## Typical Operating Characteristics

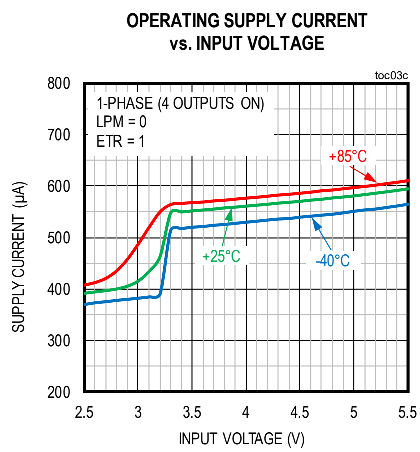
($V_{SYS}$ = 3.8V, $V_{OUT}$ = 0.85V, $I_{OUT}$ = 0A, CE = high, 4-Phase (1 Output), FPWM = 0, LPM = 0, ETR = 0, L = 220nH, $C_{OUT}$ = (22μF + 0.1μF + 2 × 4.3μF), $T_A$ = +25°C, unless otherwise noted.)

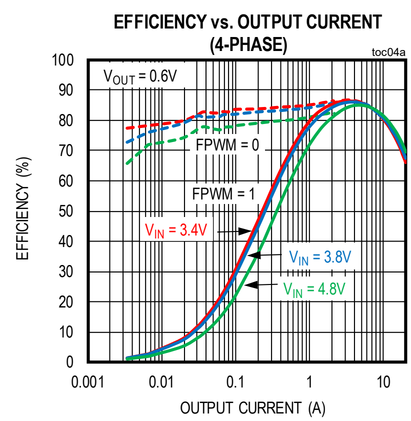


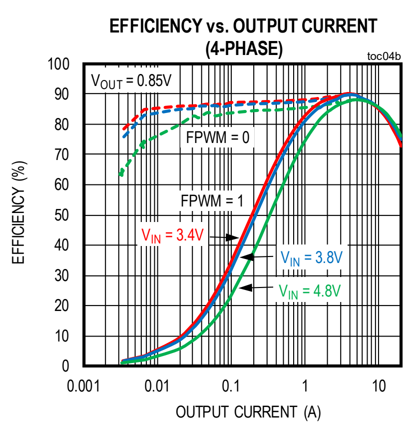



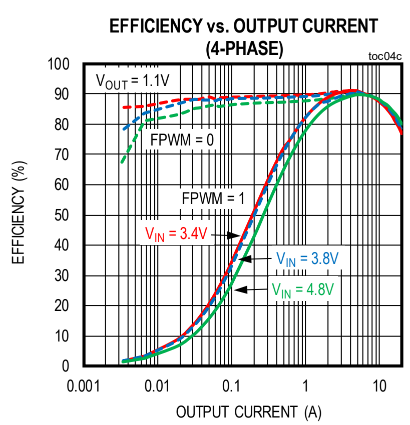



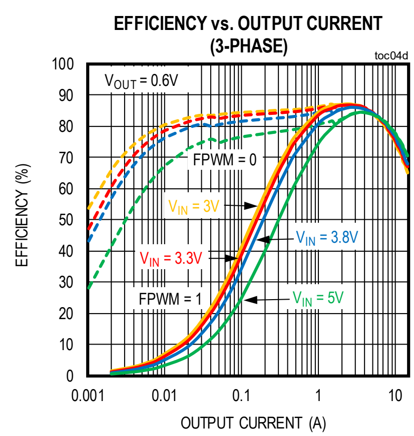



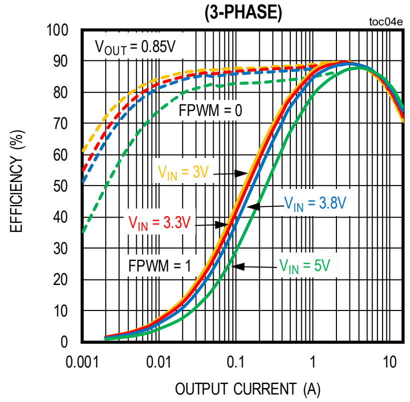



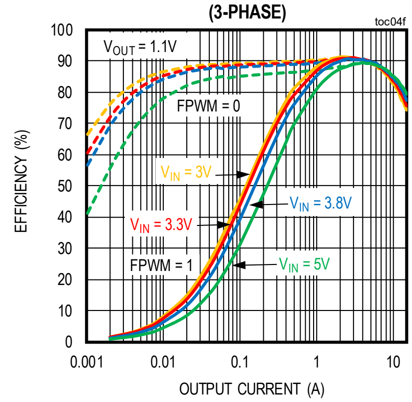
## Typical Operating Characteristics (continued)

($V_{SYS}$ = 3.8V, $V_{OUT}$ = 0.85V, $I_{OUT}$ = 0A, CE = high, 4-Phase (1 Output), FPWM = 0, LPM = 0, ETR = 0, L = 220nH, $C_{OUT}$ = (22μF + 0.1μF + 2 × 4.3μF), $T_A$ = +25°C, unless otherwise noted.)

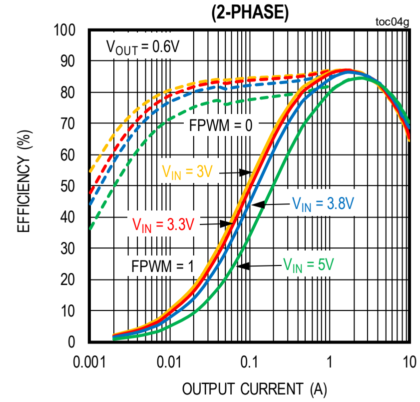
EFFICIENCY vs. OUTPUT CURRENT
(3-PHASE)



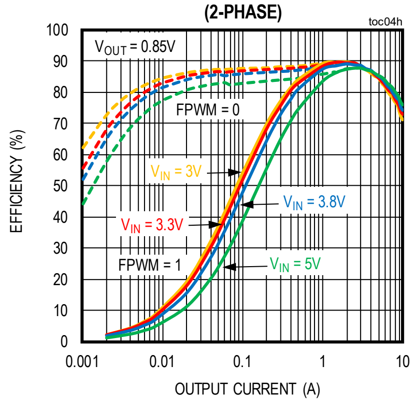

EFFICIENCY vs. OUTPUT CURRENT
(3-PHASE)



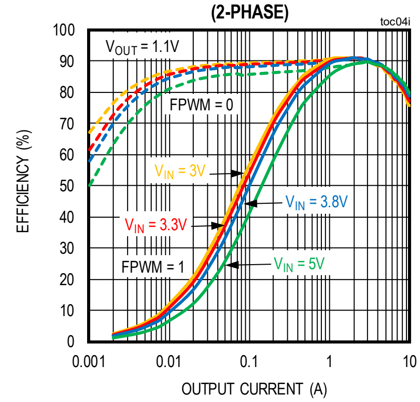

EFFICIENCY vs. OUTPUT CURRENT
(2-PHASE)



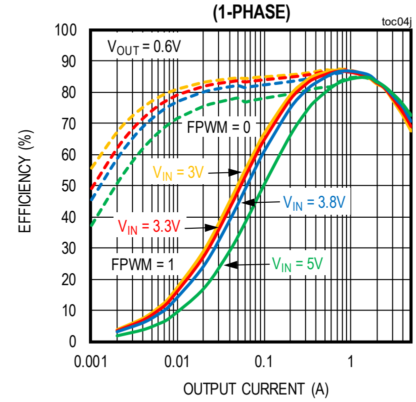

EFFICIENCY vs. OUTPUT CURRENT
(2-PHASE)



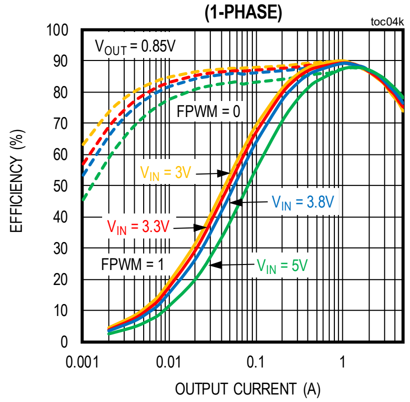

EFFICIENCY vs. OUTPUT CURRENT
(2-PHASE)



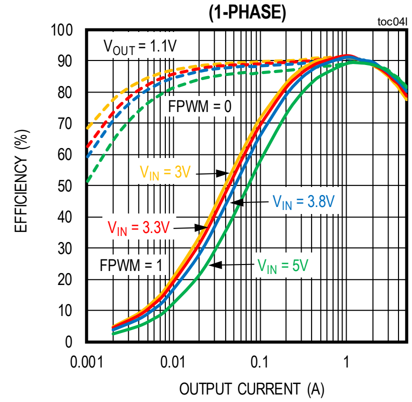

EFFICIENCY vs. OUTPUT CURRENT
(1-PHASE)



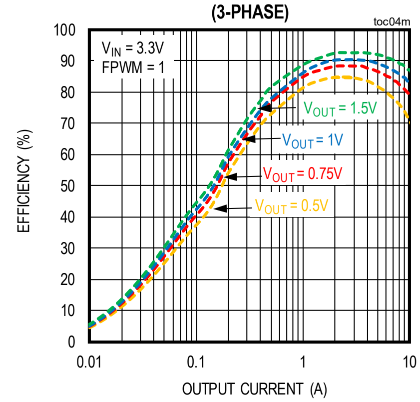

EFFICIENCY vs. OUTPUT CURRENT
(1-PHASE)




EFFICIENCY vs. OUTPUT CURRENT
(1-PHASE)



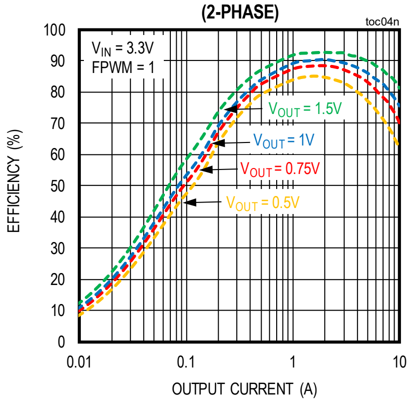

EFFICIENCY vs. OUTPUT CURRENT
(3-PHASE)



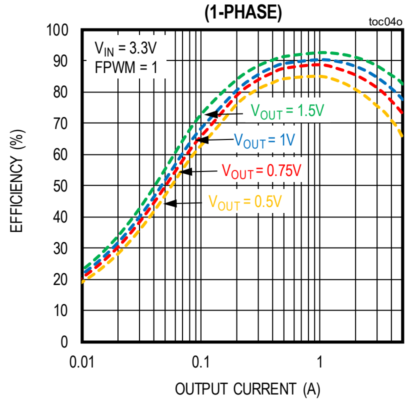
## Typical Operating Characteristics (continued)

($V_{SYS}$ = 3.8V, $V_{OUT}$ = 0.85V, $I_{OUT}$ = 0A, CE = high, 4-Phase (1 Output), FPWM = 0, LPM = 0, ETR = 0, L = 220nH, $C_{OUT}$ = (22µF + 0.1µF + 2 × 4.3µF), $T_A$ = +25°C, unless otherwise noted.)

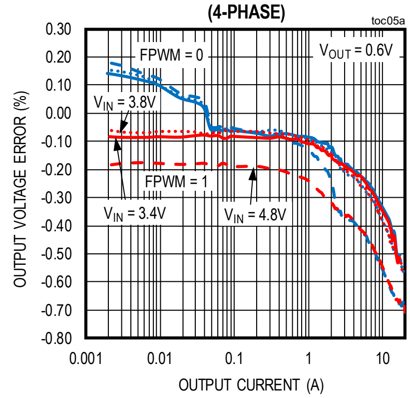
EFFICIENCY vs. OUTPUT CURRENT
(2-PHASE)



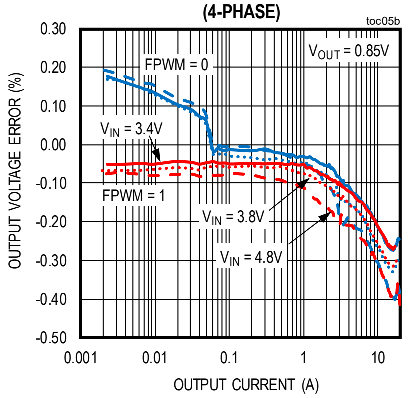

EFFICIENCY vs. OUTPUT CURRENT
(1-PHASE)



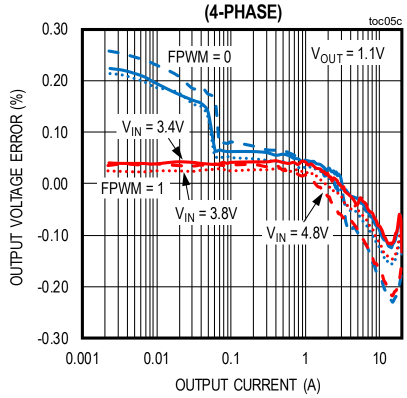

OUTPUT VOLTAGE vs. OUTPUT CURRENT
(4-PHASE)



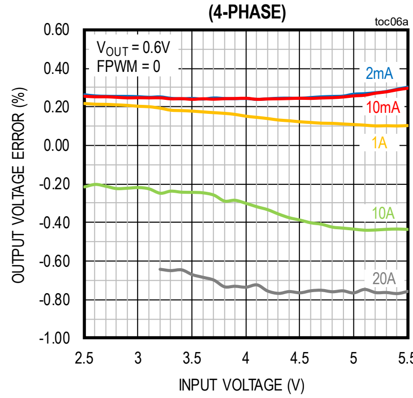

OUTPUT VOLTAGE vs. OUTPUT CURRENT
(4-PHASE)



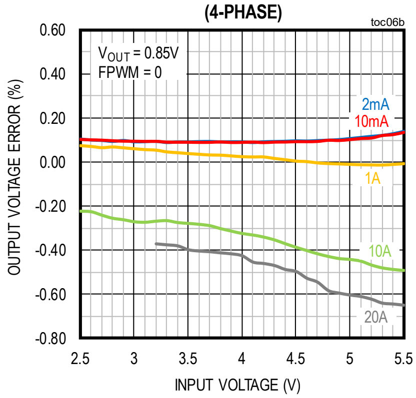

OUTPUT VOLTAGE vs. OUTPUT CURRENT
(4-PHASE)



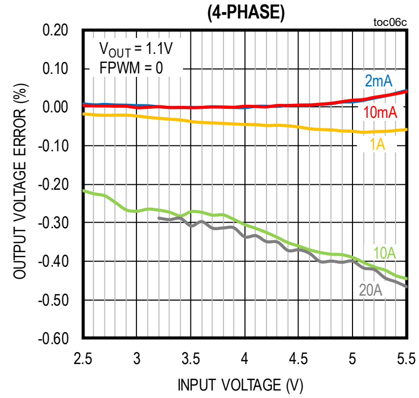

OUTPUT VOLTAGE vs. INPUT VOLTAGE
(4-PHASE)



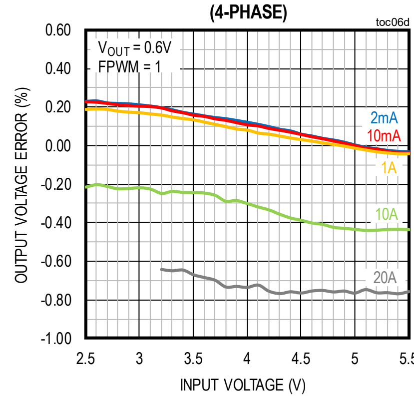

OUTPUT VOLTAGE vs. INPUT VOLTAGE
(4-PHASE)




OUTPUT VOLTAGE vs. INPUT VOLTAGE
(4-PHASE)

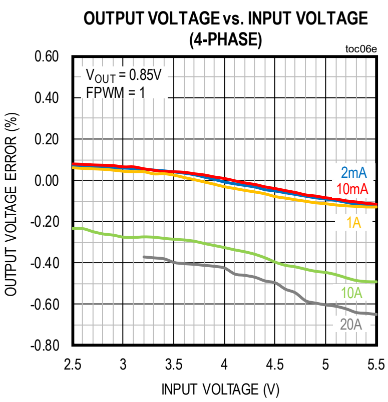


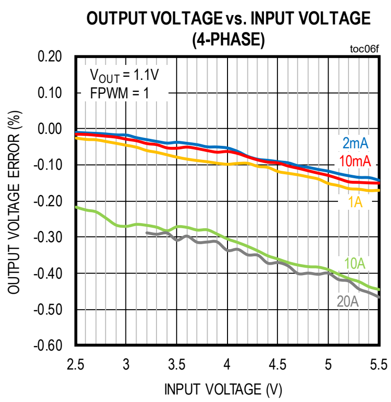

OUTPUT VOLTAGE vs. INPUT VOLTAGE
(4-PHASE)

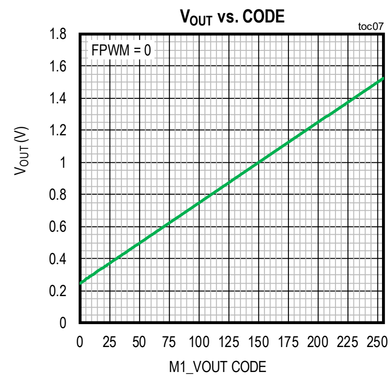


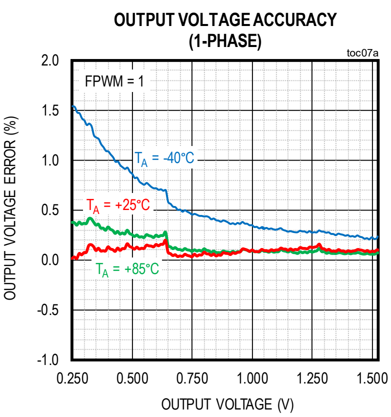
## Typical Operating Characteristics (continued)

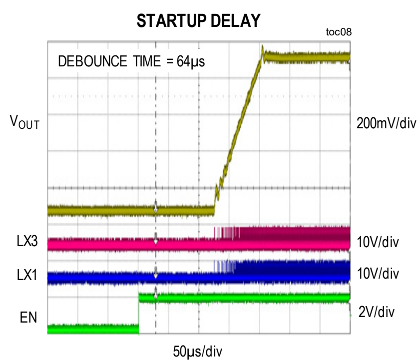
($V_{SYS}$ = 3.8V, $V_{OUT}$ = 0.85V, $I_{OUT}$ = 0A, CE = high, 4-Phase (1 Output), FPWM = 0, LPM = 0, ETR = 0, L = 220nH, $C_{OUT}$ = (22µF + 0.1µF + 2 × 4.3µF), $T_A$ = +25°C, unless otherwise noted.)

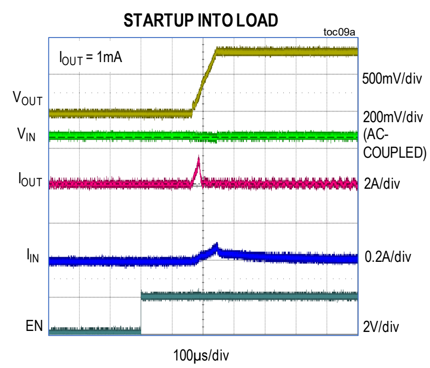


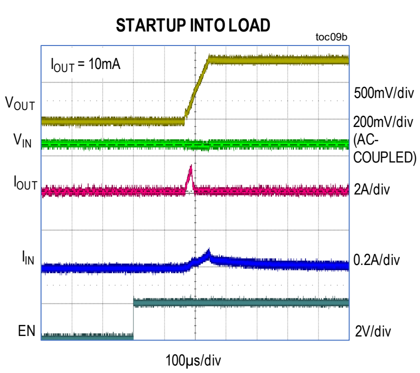



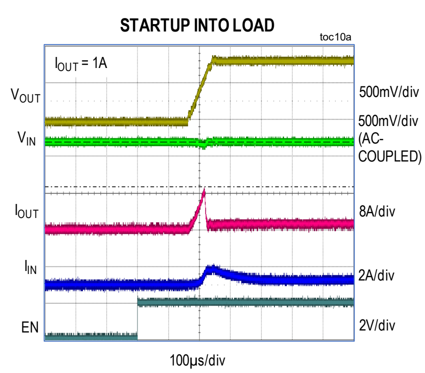



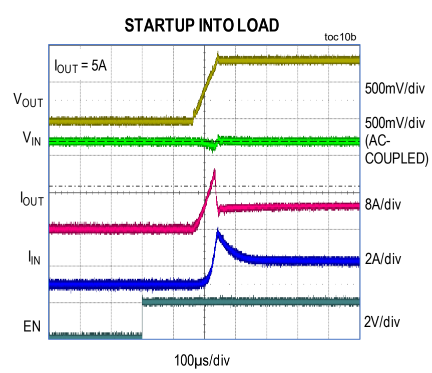



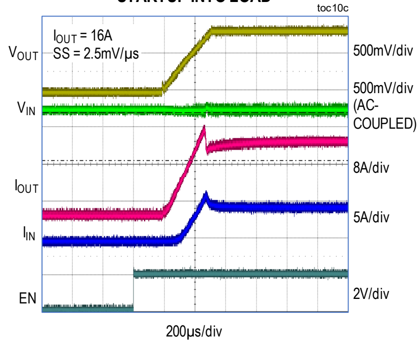



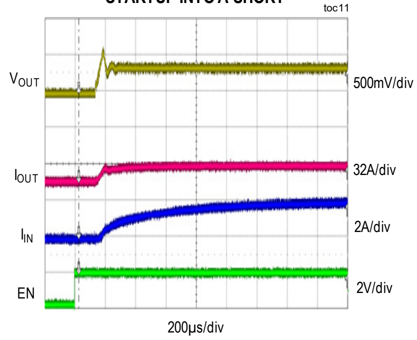
## Typical Operating Characteristics (continued)

($V_{SYS}$ = 3.8V, $V_{OUT}$ = 0.85V, $I_{OUT}$ = 0A, CE = high, 4-Phase (1 Output), FPWM = 0, LPM = 0, ETR = 0, L = 220nH, $C_{OUT}$ = (22μF + 0.1μF + 2 × 4.3μF), $T_A$ = +25°C, unless noted.)

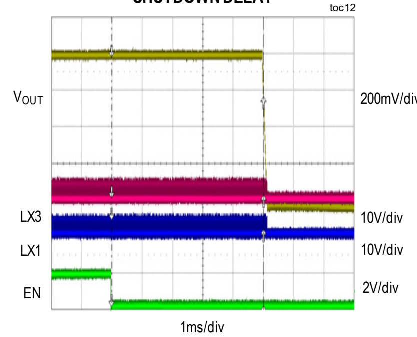
STARTUP INTO LOAD



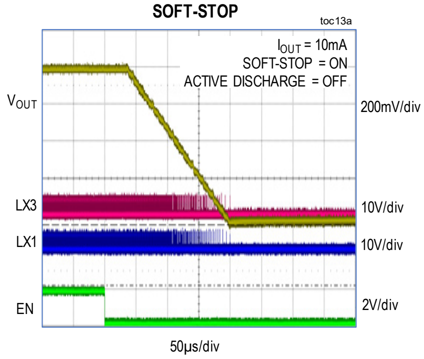

STARTUP INTO A SHORT



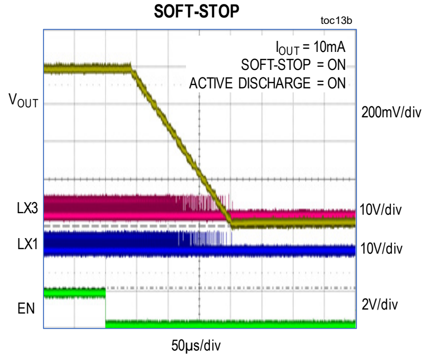

SHUTDOWN DELAY



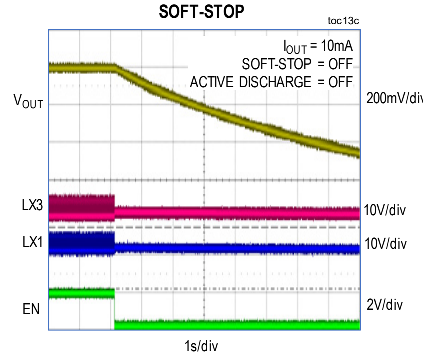

SOFT-STOP



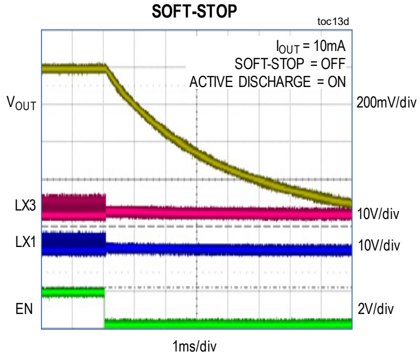

SOFT-STOP



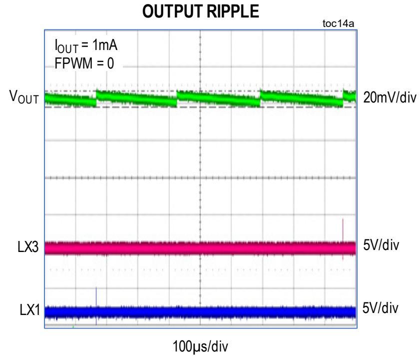

SOFT-STOP



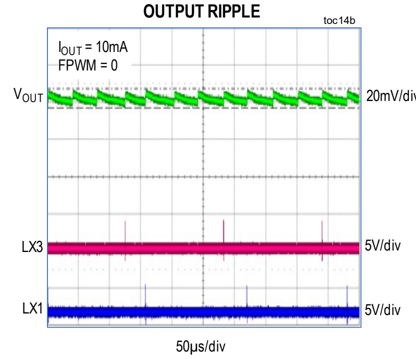

SOFT-STOP




OUTPUT RIPPLE

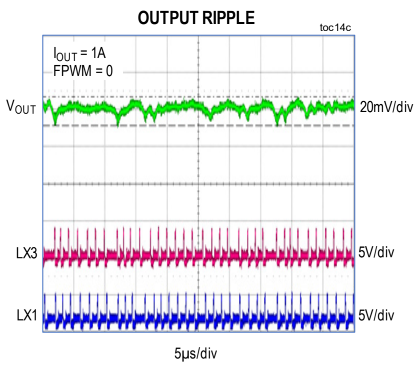


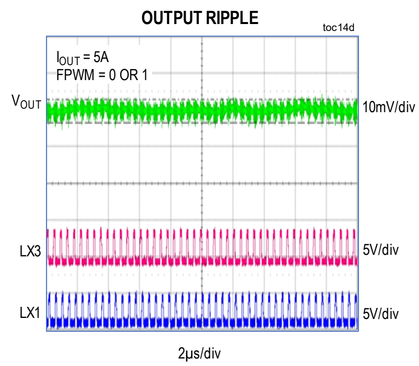

OUTPUT RIPPLE

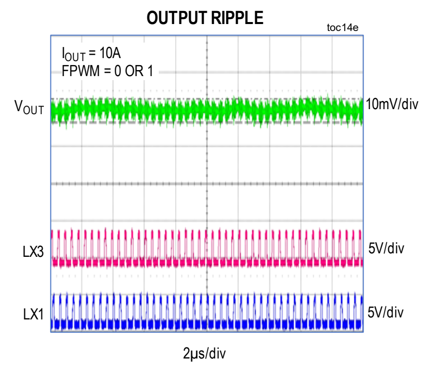


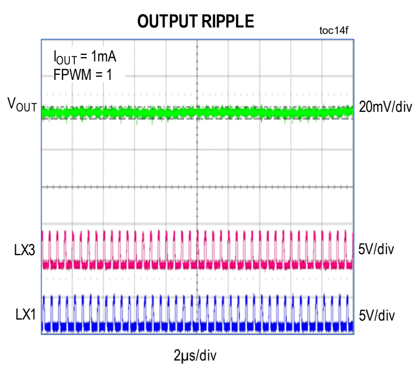
## Typical Operating Characteristics (continued)

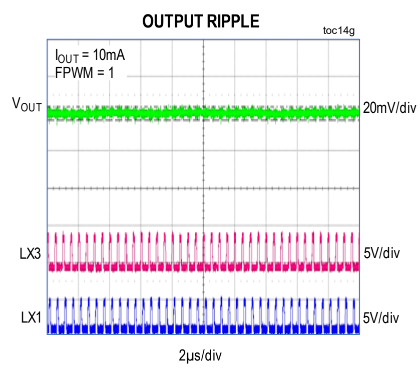
($V_{SYS}$ = 3.8V, $V_{OUT}$ = 0.85V, $I_{OUT}$ = 0A, CE = high, 4-Phase (1 Output), FPWM = 0, LPM = 0, ETR = 0, L = 220nH, $C_{OUT}$ = (22µF + 0.1µF + 2 × 4.3µF), $T_A$ = +25°C, unless otherwise noted.)

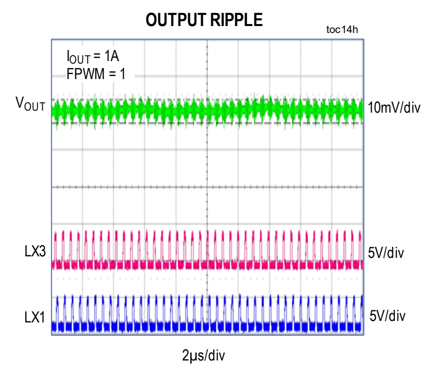


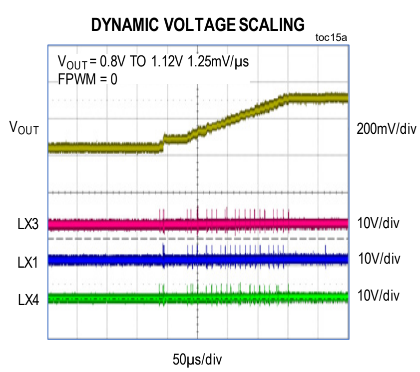



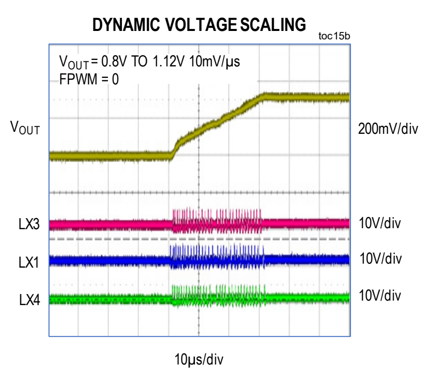



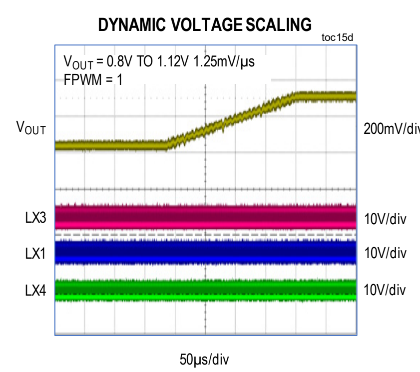



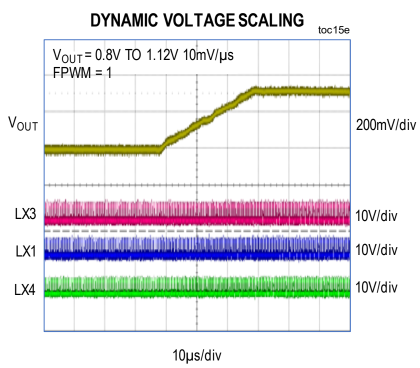



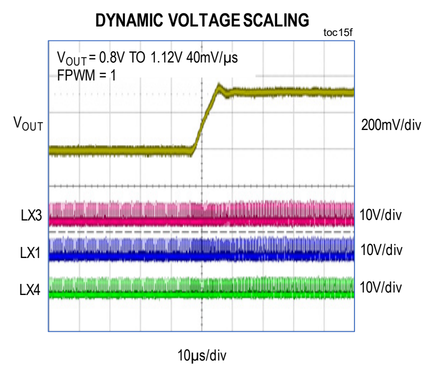



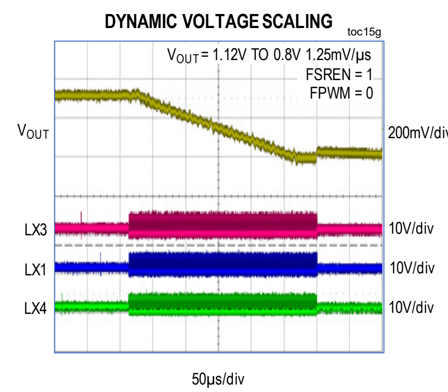



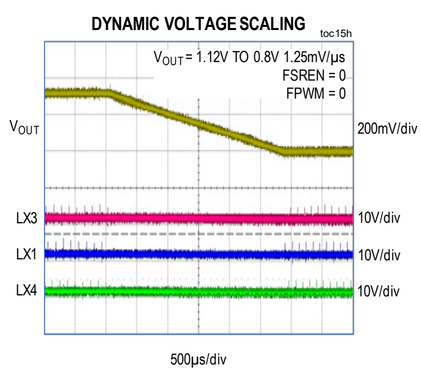
## Typical Operating Characteristics (continued)

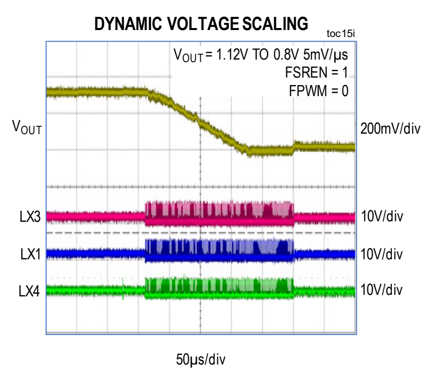
($V_{SYS}$ = 3.8V, $V_{OUT}$ = 0.85V, $I_{OUT}$ = 0A, CE = high, 4-Phase (1 Output), FPWM = 0, LPM = 0, ETR = 0, L = 220nH, $C_{OUT}$ = (22μF + 0.1μF + 2 × 4.3μF), $T_A$ = +25°C, unless otherwise noted.)

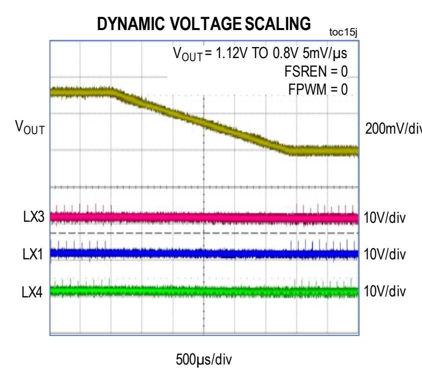


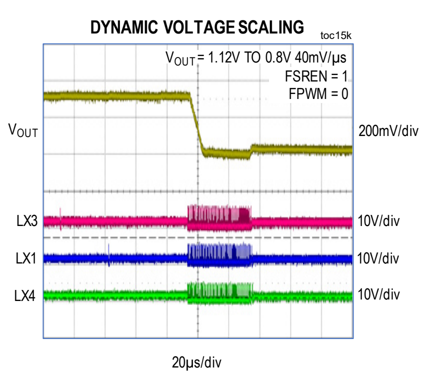



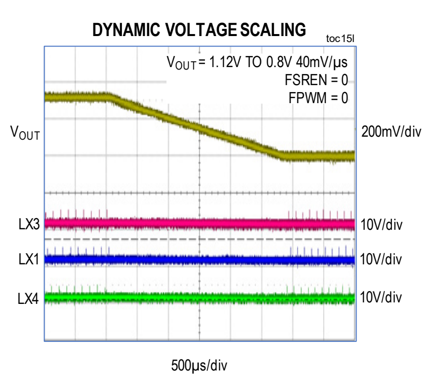



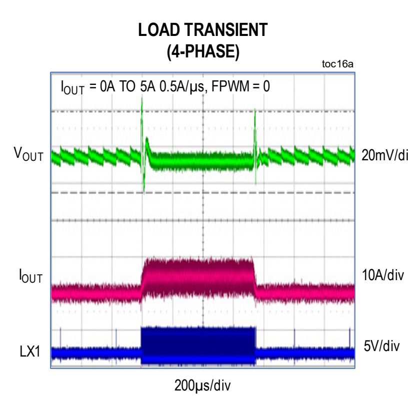



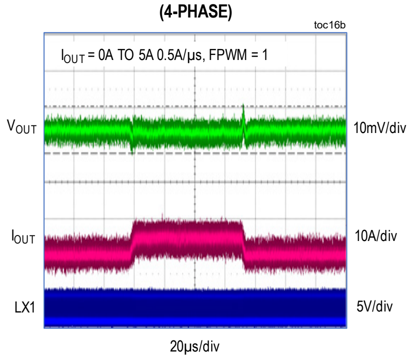



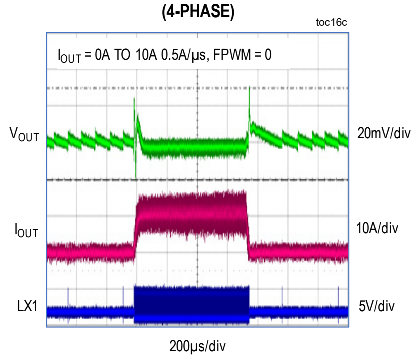
## Typical Operating Characteristics (continued)

($V_{SYS}$ = 3.8V, $V_{OUT}$ = 0.85V, $I_{OUT}$ = 0A, CE = high, 4-Phase (1 Output), FPWM = 0, LPM = 0, ETR = 0, L = 220nH, $C_{OUT}$ = (22µF + 0.1µF + 2 × 4.3µF), $T_A$ = +25°C, unless otherwise noted.)

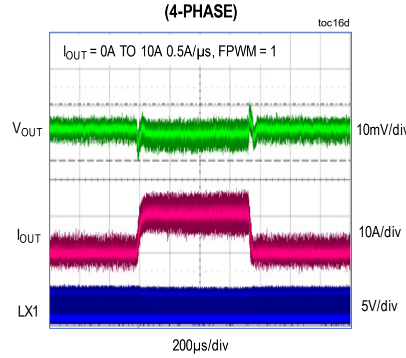
**LOAD TRANSIENT (4-PHASE)**



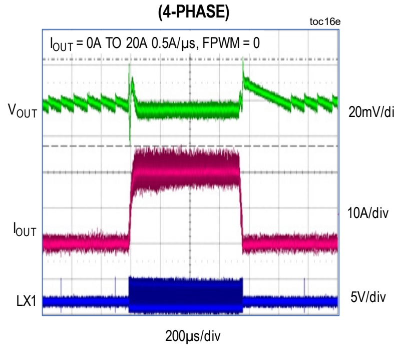

**LOAD TRANSIENT (4-PHASE)**




**LOAD TRANSIENT (4-PHASE)**




**LOAD TRANSIENT (4-PHASE)**

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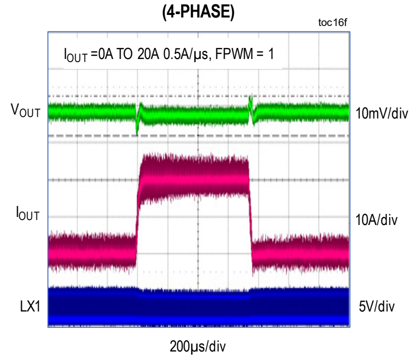
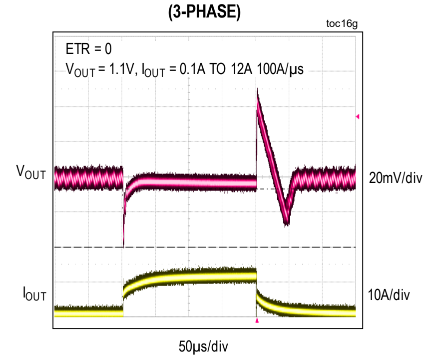



**LOAD TRANSIENT (3-PHASE)**

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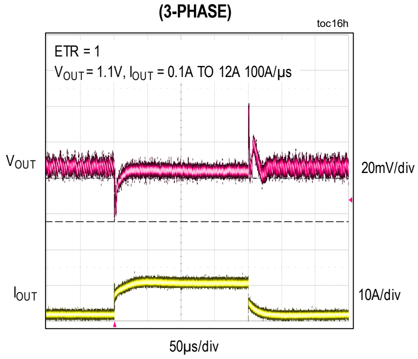
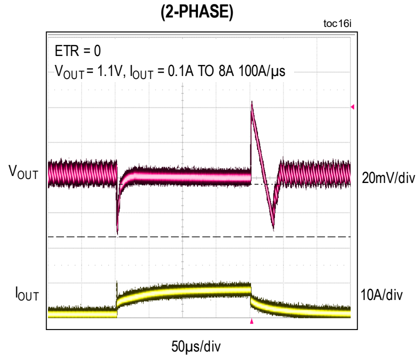
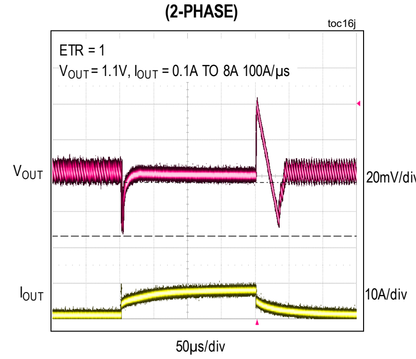



**LOAD TRANSIENT (2-PHASE)**

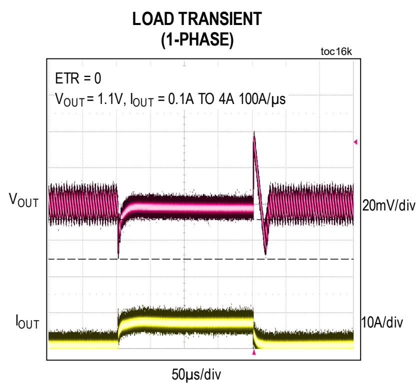


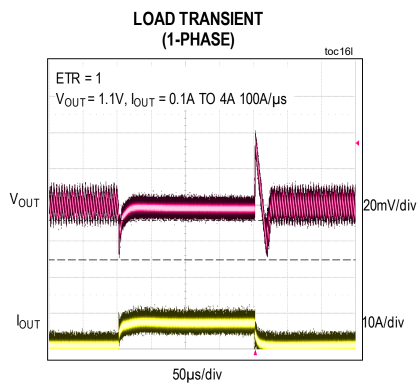

**LOAD TRANSIENT (2-PHASE)**

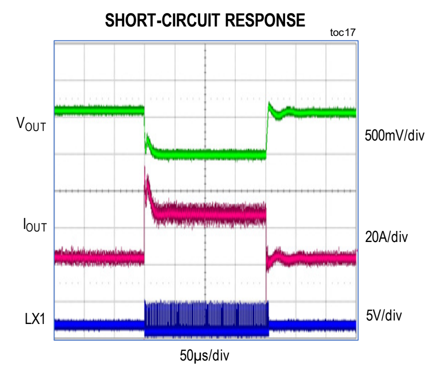


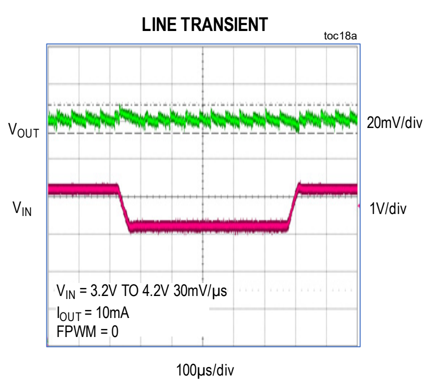
## Typical Operating Characteristics (continued)

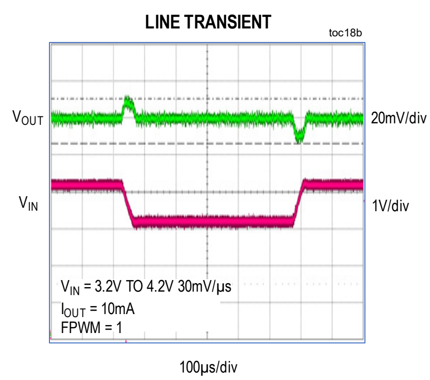
($V_{SYS}$ = 3.8V, $V_{OUT}$ = 0.85V, $I_{OUT}$ = 0A, CE = high, 4-Phase (1 Output), FPWM = 0, LPM = 0, ETR = 0, L = 220nH, $C_{OUT}$ = (22µF + 0.1µF + 2 × 4.3µF), $T_A$ = +25°C, unless otherwise noted.)

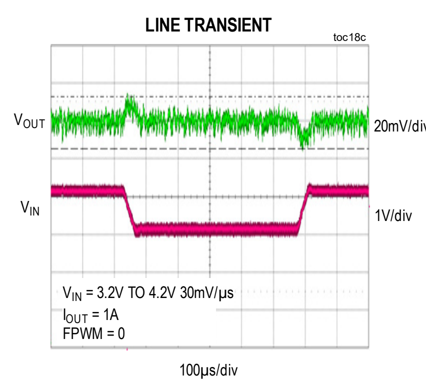


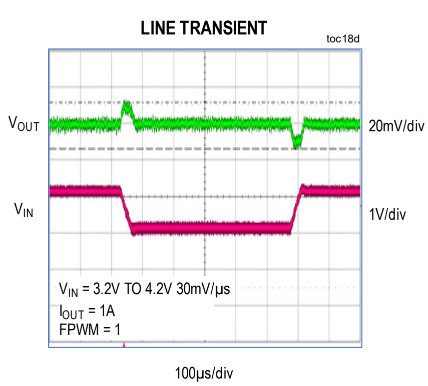



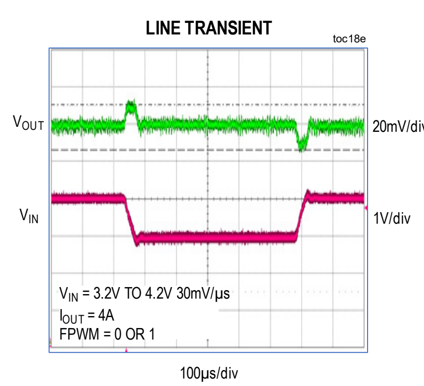



## Bump Configuration


**64 WLP (8 x 8 BUMP ARRAY, 0.4MM PITCH)**

***TOP VIEW = WAFER BACK-SIDE VIEW (BUMPS ARE NOT VIEWABLE)**

## Bump Description

| BUMP | NAME | FUNCTION |
|---|---|---|
| A1, B1, B2 | PGND1 | Phase1 Power Ground |
| A2, A3, B3 | LX1 | Phase1 Switch Node |
| A4, A5, B4, B5 | IN12 | Phase1/2 Input. Bypass to PGND1/2 with a 10μF capacitor. |
| A6, A7, B6 | LX2 | Phase2 Switch Node |
| A8, B7, B8 | PGND2 | Phase2 Power Ground |
| C1, C8, E5, E8, F1, F8 | AGND | Analog Ground |
| C2 | SNS1N | Phase1 Differential Negative Remote Sense Input |
| C3 | $\overline{\text{IRQ}}$ | Interrupt Output. A 100kΩ external pullup resistor to VIO is required. High impedance when CE = low. |
| C4 | SNS1P | Phase 1 Differential Positive Remote Sense Input |
| C5 | SNS2P | Phase 2 Differential Positive Remote Sense Input |
| C6 | EN | Global Enable Input (Active-High, Logically ORed with GLB_EN Function of GPIs). An 800kΩ internal pulldown resistance to DGND. If this pin is not used, leave it unconnected. |
| C7 | SNS2N | Phase 2 Differential Negative Remote Sense Input |
| D1 | SCL | $I^2C$ Clock Input. High impedance in off state. A 1.5kΩ~2.2kΩ of pullup resistor to VIO is required. |
| D2 | SCS | Active-Low SPI Chip Select |
| D3 | VIO | IO Supply Voltage Input. Bypass to DGND with a 0.1μF capacitor. |
| D4 | CE | Active-High Chip Enable Input.<br>CE = High (standby), $I^2C$ interface is enabled and regulators are ready to be turned on.<br>CE = Low (shutdown), all regulators are turned off and all Type-O registers are reset to their POR default values. |
| D5 | WDTRSTB_IN | Active-Low Watchdog Timer Reset Input. An 800kΩ internal pullup resistance to VIO. If this pin is not used, leave it unconnected. |
| D6 | LPM | Global Low Power Mode Input (Active-High, Logically ORed with GLB_LPM Function of GPIs). An 800kΩ internal pulldown resistance to DGND. If this pin is not used, leave it unconnected. |
| D7 | I2C_SPI_SEL | Serial Interface Selection Input. Latches at $V_{SYS}$ POR.<br>I2C_SPI_SEL = Low: $I^2C$<br>I2C_SPI_SEL = High ($V_{SYS}$): SPI |
| D8 | SYS | System (Battery) Voltage Input. Bypass to AGND with a 1μF capacitor. |
| E1 | SDA/MOSI | $I^2C$ Data I/O. High Impedance in Off State. A 1.5kΩ~2.2kΩ of pullup resistor to VIO is required. Configured as MOSI when SPI mode is selected. |
| E2 | MISO | SPI Data Output. High impedance in off state. |
| E3 | GPI0 | Active-High, General-Purpose Input. An 800kΩ internal pulldown resistance to DGND. If this pin is not used, leave it unconnected. |
| E4 | DGND | Digital Ground |

## Bump Description (continued)

| BUMP | NAME | FUNCTION |
|---|---|---|
| E6 | PH_CFG0 | Phase Configuration Selection Input. Latches at $V_{SYS}$ POR.<br>PH_CFG2 = low, PH_CFG1 = low, PH_CFG0 = low: 4 phase<br>PH_CFG2 = low, PH_CFG1 = low, PH_CFG0 = high ($V_{SYS}$): 3 + 1 phase<br>PH_CFG2 = low, PH_CFG1 = high ($V_{SYS}$), PH_CFG0 = low: 2 + 2 phase<br>PH_CFG2 = low, PH_CFG1 = high ($V_{SYS}$), PH_CFG0 = high ($V_{SYS}$): 2 + 1 + 1 phase<br>PH_CFG2 = high ($V_{SYS}$), PH_CFG1 = X, PH_CFG0 = X: 1 + 1 + 1 + 1 phase |
| E7 | PH_CFG2 | Phase Configuration Selection Input. Latches at $V_{SYS}$ POR.<br>PH_CFG2 = low, PH_CFG1 = low, PH_CFG0 = low: 4 phase<br>PH_CFG2 = low, PH_CFG1 = low, PH_CFG0 = high ($V_{SYS}$): 3 + 1 phase<br>PH_CFG2 = low, PH_CFG1 = high ($V_{SYS}$), PH_CFG0 = low: 2 + 2 phase<br>PH_CFG2 = low PH_CFG1 = high ($V_{SYS}$), PH_CFG0 = high ($V_{SYS}$): 2 + 1 + 1 phase<br>PH_CFG2 = high ($V_{SYS}$), PH_CFG1 = X, PH_CFG0 = X: 1 + 1 + 1 + 1 phase |
| F2 | SNS4N | Phase 4 Differential Negative Remote Sense Input |
| F3 | GPI1 | Active-High, General-Purpose Input. An 800kΩ internal pulldown resistance to DGND. If this pin is not used, leave it unconnected. |
| F4 | SNS4P | Phase 4 Differential Positive Remote Sense Input |
| F5 | SNS3P | Phase 3 Differential Positive Remote Sense Input |
| F6 | PH_CFG1 | Phase Configuration Selection Input. Latches at $V_{SYS}$ POR.<br>PH_CFG2 = low, PH_CFG1 = low, PH_CFG0 = low: 4 phase<br>PH_CFG2 = low, PH_CFG1 = low, PH_CFG0 = high ($V_{SYS}$): 3 + 1 phase<br>PH_CFG2 = low, PH_CFG1 = high ($V_{SYS}$), PH_CFG0 = low: 2 + 2 phase<br>PH_CFG2 = low, PH_CFG1 = high ($V_{SYS}$), PH_CFG0 = high ($V_{SYS}$): 2 + 1 + 1 phase<br>PH_CFG2 = high ($V_{SYS}$), PH_CFG1 = X, PH_CFG0 = X: 1 + 1 + 1 + 1 phase |
| F7 | SNS3N | Phase 3 Differential Negative Remote Sense Input |
| G1, G2, H1 | PGND4 | Phase 4 Power Ground |
| G3, H2, H3 | LX4 | Phase 4 Switch Node |
| G4, G5, H4, H5 | IN34 | Phase 3/4 Input. Bypass to PGND3/4 with a 10μF capacitor. |
| G6, H6, H7 | LX3 | Phase 3 Switch Node |
| G7, G8, H8 | PGND3 | Phase 3 Power Ground |

# Detailed Description

## Top-Level System Management

### System Faults

The MAX77812 monitors the system for the following faults:

- Undervoltage lockout
- VIO fault

#### Undervoltage Lockout

When the $V_{SYS}$ voltage falls below $V_{UVLO\_F}$ (2.15V typ), the MAX77812 enters into a shutdown state and UVLO forces the MAX77812 to a dormant state until $V_{SYS}$ voltage rises above the UVLO rising threshold (typically 2.5V). Once the $V_{SYS}$ voltage is higher than the UVLO rising threshold, the MAX77812 comes out of shutdown mode to be securely functional. The UVLO falling threshold is programmable through $I^2C$, but it must be set lower than UVLO rising threshold to avoid unexpected behaviors.

It is recommended to set the UVLO_F[2:0] register bits such that the UVLO falling threshold is at least 1.15V above the programmed output voltage setting.

#### VIO Fault

When the VIO supply falls below $V_{TH\_VIO\_OK}$ (1.0V typ), the MAX77812 immediately goes into a shutdown state and stays in this mode until IO supply rises beyond $V_{TH\_VIO\_OK}$ threshold.

### Thermal Protection

The MAX77812 has a centralized thermal protection circuit which monitors temperature on the die. If the die temperature exceeds +165°C ($T_{SHDN}$), the MAX77812 initiates a soft-stop for all the output(s) and all Type-O registers are reset to their POR default values. However, the MAX77812 should be able to communicate with the host processor through the serial interface as long as $V_{SYS}$ and $V_{VIO}$ supplies are within the operating range.

In case the die temperature drops by 15°C after the thermal protection occurs, the MAX77812 recovers to the normal state and the output(s) can be turned on again.

In addition to +165°C threshold, there are two additional comparators which trip at +120°C and +140°C. Interrupts are generated in the event the die temperature reaches +120°C or +140°C.

### Reset Conditions

#### Power-On Reset (POR)

When a valid system supply voltage is applied to the device, the MAX77812 goes into shutdown mode and stay there until CE goes high. As the $V_{SYS}$ voltage rises above POR threshold (≈ 1.60V), the internal reference and the integrated supply are enabled and the MAX77812 starts loading the default register values from the OTPs.

#### System Reset

When $V_{SYS}$ voltage drops below its POR threshold (≈ 1.50V), all Type-S1 registers are reset to their POR default values.

#### Off Reset

Off reset occurs by any power-off or shutdown events. This condition resets all Type-O registers to their POR default values.

#### Software Reset

All Type-O registers can be reset by writing ‘1’ to SW_RST bit in REG_RESET register. This bit clears to ‘0’ upon reset.

#### Watchdog Timeout Reset (WDTRSTB_IN)

In case the host processor fails to reset its watchdog timer for any system issues, WDTRSTB_IN signal goes low for about 100ms. When the MAX77812 detects that WDTRSTB_IN is low longer than its debounce timer (programmable by WDT_DEB[2:0]), the output voltage setting registers of all phases (Mx_VOUT[7:0]) reset to their POR default values and the output voltages return to their POR default values with given ramp-up/down slew rates.

### Chip Enable (CE)

When $V_{SYS}$ and $V_{VIO}$ supplies are valid, a logic-high on CE pin puts the MAX77812 into standby mode (enabled). In standby mode, all user registers are accessible through $I^2C$/SPI so that the host processor can overwrite the default output voltages of regulators and each regulator can be enabled by either $I^2C$/SPI or GPI input if applicable.

When CE pin goes high, the MAX77812 turns on the internal bias circuitry which takes typically 50μs to be settled. As soon as the bias is ready, all the regulators are allowed to be turned on via $I^2C$/SPI or EN pins. In case the regulators are enabled before the bias circuitry is ready, the regulators require longer time to startup.

When the CE pin is pulled low, the MAX77812 goes into shutdown mode (disabled) and turns off all the regulators regardless of EN pins. This event also resets all Type-O registers to their POR default values.

## Enable Control

Each master phase of the MAX77812 can be enabled and disabled by a corresponding enable register bit (EN_Mx), EN input and multifunction GPIs. The enable logic is an 'OR' logic of active enable logic signals. For example, the Master1 is enabled when EN_M1 bit, GLB_EN or M1_EN logic signal is set to '1'. When all active signals are '0', the corresponding master phase is turned off.

## Startup and Shutdown Sequence

The MAX77812 supports programmable startup and shutdown delay times between the master phases. The startup and shutdown sequence is initiated by either EN pin or GLB_EN function of GPIs. The startup and shutdown delay times between the master phases are programmable from 0ms to 62ms (32 steps).

The startup sequence is set by OTP bits as well as STUP_DLYx registers and the Master 1 is always turned on as soon as a startup sequence is initiated, while the shutdown sequence is programmable by SHDN_DLYx registers only and the delay times for all master phases are programmable.

If any master phase(s) is(are) turned on by EN_Mx bit or Mx_EN input before initiating startup or shutdown, global startup or shutdown sequence does not affect the master phase(s) already turned on or off.

Figure 1 shows a typical startup and shutdown sequence.

For more detailed information on programming the sequencer, refer to **Application Note 6826: *How to Program Startup and Shutdown Sequence with MAX77812***.

## Immediate Shutdown Events

The following events initiate an immediate shutdown:

- $V_{SYS}$ < SYS UVLO falling threshold ($V_{UVLO\_F}$)
- $V_{VIO}$ < VIO OK threshold ($V_{TH\_VIO\_OK}$)

The events in this category are associated with potentially hazardous system states. Powering down the host processor and resetting all Type-O registers help mitigate any issues that can occur due to these potentially hazardous conditions.

## Interrupt and Mask

The $\overline{IRQ}$ output is used to indicate to the host processor that the status on the MAX77812 has changed. The $\overline{IRQ}$ output asserts (goes low) anytime an unmasked interrupt bit is triggered. The host processor reads the interrupt source register (ADDR 0x01) and the interrupt registers that are indicated by the interrupt source register to see the cause of interrupt event. Note that the interrupt source register is cleared when the corresponding interrupt register group is read by the host processor.

All the interrupt events are edge-triggered. Therefore, the same interrupt is not generated repeatedly even though the interrupt condition persists.

Each interrupt register can be read at a time and all interrupt bits are clear-on-read bits. The $\overline{IRQ}$ output de-asserts (goes high) when all interrupt bits have been cleared. If an interrupt is captured during the read sequence, $\overline{IRQ}$ output is held low. When $\overline{IRQ}$ output is pulled low by an unmasked interrupt event, $\overline{IRQ}$ output stays low until the interrupt bit is cleared by the reading operation of the host processor or the corresponding interrupt mask bit is set to '1' (masked).

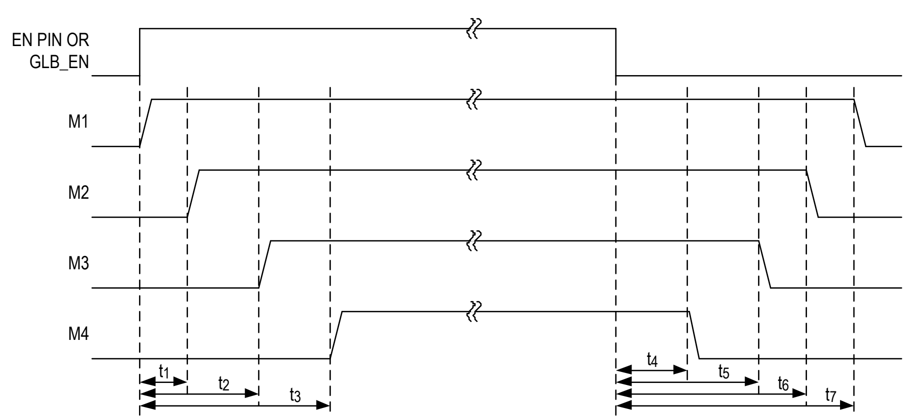



*Figure 1. Startup and Shutdown Sequence*

Each interrupt can be masked (disabled) by setting the corresponding interrupt mask register bit.

When the corresponding mask bit is set (masked), an interrupt bit is not set for an interrupt event. As a result, the $\overline{IRQ}$ output stays high. When the mask bit is cleared, an active interrupt event at the time of clearing the mask bit is captured, which results in pulling the $\overline{IRQ}$ output low.

Interrupt mask bits are set to '1' by default and are reset to the default values at power-off events.

### Status

In addition to interrupt bits, the MAX77812 has read-only STATUS bits. Those bits always represent the current status of the device. It is highly recommended that the host processor read STATUS bits whenever the MAX77812 is initialized by the host processor. These STATUS bits do not directly affect the state of interrupt bits.

## Quad-Phase Buck Regulator

The MAX77812 uses Maxim's proprietary Quick-PWM™ adaptive on-time control scheme. Adaptive on-time control provides fast response to load transients, inherent compensation to input voltage variation, and stable performance at low duty cycles. On-times (high-side MOSFET on) are controlled by the on-time generator circuit. This circuit calculates an on-time based on the input voltage ($V_{INx}$), the output voltage ($V_{OUTx}$), and the target switching frequency ($F_{SW}$). The on-time is modified (slightly shortened or lengthened) by the phase current balancing control circuit. Off-times (low-side MOSFET on) begin when the on-time ends. Shoot-through current from INx to PGNDx is avoided by introducing a brief period of dead-time between switching events when neither MOSFET is on. During the dead-time, the inductor current conducts through the intrinsic body diode of the low-side MOSFET.

The PWM comparator regulates VOUTx by modulating off-time. A compensation ramp is fed to the positive input of the PWM comparator and the negative input is a voltage proportional to the actual output voltage error added to the replicated AC current in the inductor. The PWM comparator begins an on-time (and resets the compensation ramp) when the error voltage plus replicated AC inductor current becomes greater than the ramp. When the calculated on-time expires, the off-time automatically begins. One PWM comparator is used to control all phases in multiphase configuration. The output is demultiplexed by a phase scheduler which controls the phase spacing of each switching stage (e.g., 2Φ is spaced 180º apart, 3Φ is spaced 120º, 4Φ is spaced 90°). Multiphase configurations permanently have all phases activated and always switches in sequence during steady-state operation (phases do not add or shed).

The switching frequency ($F_{SW}$) of the adaptive on-time BUCK is variable and heavily influenced by the instantaneous load. More on-time pulses in a given time (higher $F_{SW}$) is observed as load increases. Fewer on-times in a given time (lower $F_{SW}$) is observed as load decreases.

### Phase/Output Configurations

The MAX77812 supports user-programmable phase configuration by PH_CFG0, PH_CFG1 and PH_CFG2 input logic state. The input logic state is latched at the POR event.

All supported phase configurations are shown in Table 1. Refer to **Application Note 6804: *Guidelines for the MAX77812 User-Selectable Phase Configurations and How to Select Them*** for a concise summary of all the information regarding phase configurations found in this data sheet.

## Table 1. User-Programmable Phase/Output Configurations

| PH_CFG2 | PH_CFG1 | PH_CFG0 | PHASE CONFIGURATION |
|---|---|---|---|
| Low | Low | Low | 1 Output: 4-Phase (Master 1) |
| Low | Low | High | 2 Outputs: 3-phase (Master 1) + 1-phase (Master 4) |
| Low | High | Low | 2 Outputs: 2-phase (Master 1) + 2-phase (Master 3) |
| Low | High | High | 3 Outputs: 2-phase (Master 1) + 1-phase (Master 3) + 1-phase (Master 4) |
| High | X | X | 4 Outputs: 1-phase (Master 1) + 1-phase (Master 2) + 1-phase (Master 3) + 1-phase (Master 4) |

Based on the selected phase configuration, the phase selector generates the TON signals to each power stage with different phase interleaving schemes and the master phases are assigned as shown in Figure 2.

Note that only registers for the master phase(s) are activated and the slave phase(s) are controlled by the corresponding master phase(s).

## SKIP/Forced PWM Operation

In normal operating mode, buck automatically transitions from skip mode to fixed frequency operation as the load current increases. For operating modes where lowest output ripple is required, Forced PWM switching behavior can be enabled by writing ‘1’ to Mx_FPWM bit.

## Low Power Mode

Each master includes LPM (low power mode) operation to minimize the quiescent current when the host processor is in sleep state. In LPM, the ETR (enhanced transient response), ADT (adaptive dead-time control), and $\overline{POK}$ comparator (POK = high) are disabled so that load transient response of the buck regulators are derated as the trade-off. The LPM of each master can be enabled independently by Mx_LPM bits.

## Startup and Soft-Start

When starting up buck regulator, the bias circuitry must be enabled and provided with adequate time to settle. The bias circuitry is guaranteed to settle within 250μs, at which time, the buck regulators power-up sequence can commence. Note that attempting to implement a power-up sequence before the BIASOK signal is generated results in all enabled regulators starting up at the same time.

The buck regulator supports starting into a prebiased output. For example, if the output capacitor has an initial voltage of 0.4V when the regulator is enabled, the regulator gracefully increases the capacitor voltage to the required target voltage such as 1.0V. This is unlike other regulators without the start into prebias feature where they can force the output capacitor voltage to 0V before the soft-start ramp begins.

The buck regulator supports programmable soft-start rate from 1.25mV/μs to 60mV/μs. The controlled soft-start rate and buck regulator current limit (ILIM_PEAK) limit the input inrush current to the output capacitor (IINRUSH). IINRUSH = min (ILIM_PEAK & COUT x dv/dt). Note that the input current of the buck regulator is lower than the inrush current to the output capacitor by the ratio of output to input voltage.

## Output Voltage Setting

The output voltage is programmable from 0.25V to 1.525V in 5mV steps to allow fine adjustment to the processor supply voltage under light load conditions to minimize power loss within the processor. Each master phase have three output voltage control registers. Mx_VOUT[7:0] register is for normal operation and Mx_VOUT_D[7:0] and Mx_VOUT_S[7:0] are used for voltage selection function by GPIx. See the *Multifunction GPIs* section. The default output voltages are set by an OTP option at the factory. The default output voltages can be overwritten by changing the contents in Mx_VOUT[7:0] register prior to enabling the regulator. It is recommended to maintain at least 1.15V of headroom between $V_{SYS}$ and the programmed output voltage setting.

For some applications, an output voltage higher than 1.525V is required. The MAX77812 supports higher output voltage with the addition of an external voltage-divider network. For more details, refer to ***Application Note 6823: Generating a Higher Output Voltage than 1.525V Using the MAX77812***.

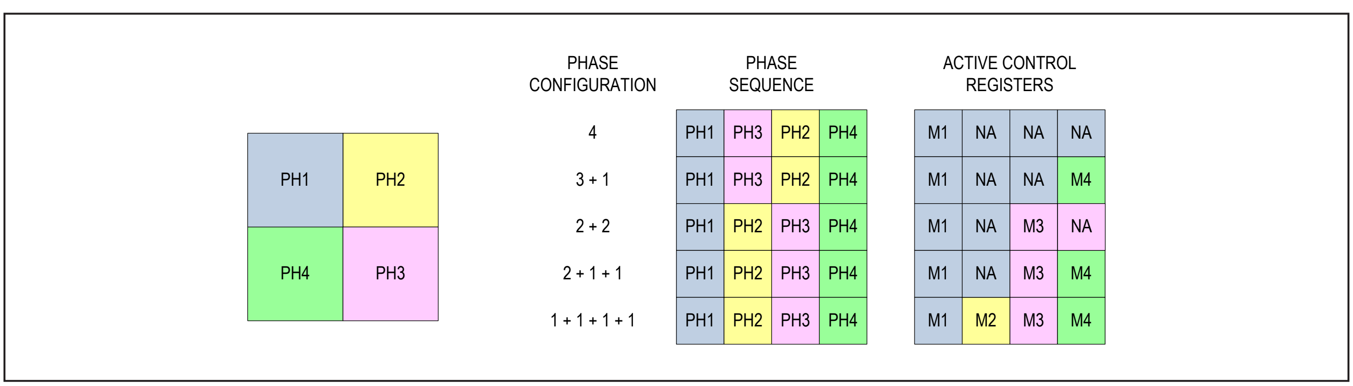



*Figure 2. Buck Phase Configuration*

### Changing Output Voltage During Operation

In a typical smartphone or tablet application, there are several power domains in which the operating frequency of the processor is increased or decreased (DVFS). When the operating frequency needs to be changed, it is expected that the buck regulator responds to a command to change the output voltages to new target values quickly. The high peak current limit, coupled with low inductance and small output capacitance, allows the buck regulator to respond to a positive step change in output voltage and settle to the new target value quickly. The buck regulator provides programmable ramp-up slew rates to accommodate different requirements.

For a negative step change in output voltage, the settling time is not critical. In Forced PWM mode (either Mx_FPWM bit or Mx_FSREN bit is enabled), the negative inductor current through NMOS discharges energy from the output capacitor, which helps the output voltage to decrease to the new target value faster. In skip mode, the negative inductor current is not allowed so that the output voltage settling time is dependent on the load current and the output capacitance.

### Output Voltage Slew Rate Control

The buck regulator supports programmable slew rate control feature when increasing and decreasing the output voltage. The ramp-up slew rate can be set to 1.25mV/µs, 2.5mV/µs, 5mV/µs, 10mV/µs, 20mV/µs 40mV/µs or 60mV/µs independently via B_RU_SR[2:0] bits, while the ramp-down slew rate is programmable to 1.25mV/µs, 2.5mV/µs, 5mV/µs, 10mV/µs, 20mV/µs 40mV/µs or 60mV/µs through B_RD_SR[2:0].

### Remote Output Voltage Sensing

All phases support differential remote output voltage sensing feature for improving point of load regulation. Differential feedback (SNSxP and SNSxN) enables voltage sensing directly at the point of load, ensuring best voltage regulation at the load, regardless of power plane impedances.

### Output Active Discharge

BUCK provides an internal 100Ω resistor for output active discharge function. If the active discharge function is enabled (Mx_AD = 1), the internal resistor discharges the energy stored in the output capacitor to PGNDx whenever the regulator is disabled.

Either the regulator remains enabled or the active discharge function is disabled (Mx_AD = 0), the internal resistor is disconnected from the output. If the active discharge function is disabled, the output voltage decays at a rate that is determined by the output capacitance and the load current when the regulator is turned off.

### Enhanced Transient Response

The MAX77812 features the enhanced transient response (ETR) function to improve the output-voltage transient responses with very fast load changes. When enabled, the ETR function monitors the output voltage and detects high dv/dt undershoot and overshoot separately.

When the negative ETR (NETR) is detected during output-voltage undershoot, the buck controllers turn on all master and slave phases assigned to the same output at the same time (in-phase) until the NETR is de-asserted. This allows the multi-phase buck converters (no significant impact on single-phase buck) to pump up energy to the output in order to recover from the undershoot quickly.

When the positive ETR (PETR) is detected, the buck controllers turn off the corresponding low-side MOSFETs to discharge excessive energy stored in the inductors, which results in suppressing output-voltage overshoot. When the PETR is released, the buck controllers operate in FPWM mode for about 5ms before returning to normal operation.

Both NETR and PETR functions are enabled by default, but they can be turned off to reduce quiescent current by clearing the B_NETR_EN and B_PETR_EN bits in the GLB_CFG3 register.

### Inductor Selection

The buck regulator is optimized for 220nH to 470nH inductors. The lower the inductor DCR, the higher the buck efficiency is. Users need to trade off inductor size with DCR value and choose a suitable inductor for the buck.

### Inductor Current Limit

A cycle-by-cycle current limit provides overcurrent protection by monitoring the current in the high-side and low-side MOSFETs. The peak current limit ($I_{PLIM}$) triggers during on-time and prevents the inductor current from running away. If $I_{PLIM}$ trips, the on-time ends and the low-side MOSFET turns on to reduce the inductor current until it hits the valley current limit ($I_{VLIM}$). Once the current falls to $I_{VLIM}$, normal operation resumes. Note that the buck output current is limited to $(I_{PLIM} + I_{VLIM})/2$. For more detailed information, refer to **Application Note 6820: *How Overcurrent Protections Works in the MAX77812***.

### Input and Output Capacitor Selection

The input capacitor, $C_{IN}$, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the device. The impedance of $C_{IN}$ at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications a 10μF capacitor is sufficient.

The output capacitor, $C_{OUT}$, is required to keep the output voltage ripple small and to ensure regulation loop stability. $C_{OUT}$ must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. The recommended minimum output capacitance per phase is 22μF.

### Unused Outputs

Follow these guidelines when the application has unused buck outputs:

- Connected unused inputs (INx) to SYS.
- Leave unused LXx pins unconnected (open).
- Connect unused SNSxN and PGNDx pins to ground.
- Connect unused SNSxP pins to either input or ground, depending on the state of the unused output in the application:
  - If the unused output can be enabled at any point in the application, either by the global enable input pin (EN) or a GPIx set to be a global enable, **connect the unused SNSxP to INx**.
  - If the unused output is disabled by default and will never be enabled, **connect the unused SNSxP to ground**.

Do not confuse unused outputs with unused phases. Phases configured under a master controller in a multiphase configuration must connect according to Table 1.

If possible, do not enable unused outputs. An unused output with a floating LX pin might try switching the LX node indefinitely (depending on the SNSxP connection), which wastes supply current.

### PCB Trace Resistance

The evaluation kit (and the typical PCB on which the MAX77812 is expected to be designed in) utilize 1/3oz. Cu, which is plated up to 0.5oz. 0.5oz. Cu has a typical resistance of 1mΩ per square.

### Power-OK ($\overline{POK}$)

The $\overline{POK}$ comparator is active whenever the regulator is enabled, soft-start has finished, and the regulator is not in low-power mode. The Mx_$\overline{POK}$ bits are ‘0’ by default and assert to ‘1’ if the output falls below the output POK trip falling threshold level while the output is enabled.

## Table 2. Suggested Inductors

| MFGR. | SERIES | NOMINAL INDUCTANCE (nH) | TYPICAL DC RESISTANCE (mΩ) | CURRENT RATING (A) -30% (ΔL/L) | CURRENT RATING [A] ΔT = +40°C RISE | DIMENSIONS L x W x H (mm) |
|---|---|---|---|---|---|---|
| Cyntec | HMLE20161B-R22MDR | 220 | 13 | 5.8 | 5.3 | 2.0 x 1.6 x 1.2 |
| TOKO | DFE201610-E-R24N | 240 | 16 | 7.0 | 5.5 | 2.0 x 1.6 x 1.0 |
| ALPS | GLULMR2201A | 220 | 9 | 6.5 | 7.0 | 2.5 X 2.0 X 1.2 |

## Table 3. Suggested Capacitors

| MFGR. | SERIES | NOMINAL CAPACITANCE (μF) | RATED VOLTAGE (V) | TEMPERATURE CHARACTERISTICS | CASE SIZE (Imperial) | DIMENSIONS L x W x H (mm) |
|---|---|---|---|---|---|---|
| Murata | GRM188R60J106ME84 | 10 ±20% | 6.3 | X5R | 0603 | 1.6 x 0.8 x 0.8 |
| Murata | GRM188R60J226MEA0 | 22 ±20% | 6.3 | X5R | 0603 | 1.6 x 0.8 x 0.8 |

### Table 4. Multifunction GPI Configurations

| GPIx_FUNC[3:0] | FUNCTION | REMARK |
|---|---|---|
| 0000b | GLB_EN | Global Enable (Master 1 through Master 4) |
| 0001b | M1_EN | Master 1 Enable |
| 0010b | M2_EN | Master 2 Enable |
| 0011b | M3_EN | Master 3 Enable |
| 0100b | M4_EN | Master 4 Enable |
| 0101b | GLB_VSEL | Global Voltage Selection (Master 1 through Master 4) |
| 0110b | M1_VSEL | Master 1 Voltage Selection |
| 0111b | M2_VSEL | Master 2 Voltage Selection |
| 1000b | M3_VSEL | Master 3 Voltage Selection |
| 1001b | M4_VSEL | Master 4 Voltage Selection |
| 1010b | GLB_LPM | Global Low Power Mode Select (Master 1 through Master 4) |
| 1011b | M1_LPM | Master 1 Low Power Mode Enable |
| 1100b | M2_LPM | Master 2 Low Power Mode Enable |
| 1101b | M3_LPM | Master 3 Low Power Mode Enable |
| 1110b | M4_LPM | Master 4 Low Power Mode Enable |
| 1111b | No function | — |

## Multifunction GPIs

### General Description

The MAX77812 has two general purpose inputs (GPI0 and GPI1) that can be configured as the enable of regulators, the output voltage selection, the low power mode control and no function. The function of these two inputs is programmable through $I^2C$/SPI (GPI_FUNC register) on the fly. **Application Note 6822: *How to Use Multi-Function GPIs?*** provides an in-depth look at programming the GPIs for their various functions.

### Enable Control by GPI

When the GPIx are configured as output enable pins, the enable logic of a specific regulator is an 'OR' logic of the GPIx and the corresponding enable register bit (Mx_EN). For example, if GPI0_FUNC[3:0] = 0001b, the buck Master 1 enable is controlled by GPI0 and M1_EN bit.

In case the two GPIs are configured as the same enable function (i.e., GPI0_FUNC[3:0] = GPI1_FUNC[3:0] = 0010b), those inputs are ORed with M2_EN bit. GLB_EN function (GPI0_FUNC[3:0] = 0000b) allows the host processor to enable all the masters in sequence based on STUP_DLYx registers. Note that M1 thru M4 are defined by PH_CFG0, PH_CFG1 and PH_CFG2 inputs.

### Voltage Selection by GPI

The buck has two additional output voltage control registers (Mx_VOUT_D[7:0] and Mx_VOUT_S[7:0]) besides one (Mx_VOUT[7:0]) for normal operation. Those two additional registers are for storing the default output voltage and the system sleep mode output voltage for a specific host processor.

When GPIx are configured as voltage selection pins, the output voltage of a specific regulator is set by Mx_VOUT_D[7:0] and Mx_VOUT_S[7:0] registers based on the input logic. For example, if GPI0_FUNC[3:0] = 0101b, the output voltages of all the masters are set by Mx_VOUT_D[7:0] and Mx_VOUT_S[7:0] when GPI0 = high and GPI0 = low, respectively. In case the two GPIs are configured as the same voltage selection function, those inputs are ORed. During the output voltage transition, the ramp-up/down slew rate is controlled by B_RU_SR[2:0] and B_RD_SR[2:0]. Note that M1 thru M4 are defined by PH_CFG0, PH_CFG1 and PH_CFG2 inputs.

### Low Power Mode by GPI

When GPIx are configured as low power mode enable pins, the low power mode enable logic of a specific regulator is an 'OR' logic of GPIx and the corresponding enable register bit (Mx_LPM). For example, if GPI0_FUNC[3:0] = 1011b, the buck Master 1 low power mode enable is controlled by GPI0 and M1_LPM bit.

In case the two GPIs are configured as the same enable function (i.e., GPI0_FUNC[3:0] = GPI0_FUNC[3:0] = 1100b), those inputs are ORed with M2_LPM bit. GLB_LPM function (GPI0_FUNC[3:0] = 1010b) allows the host processor to enable low power mode of all the masters at the same time. Note that M1 thru M4 are defined by PH_CFG0, PH_CFG1, and PH_CFG2 inputs.

## I2C Serial Interface

### General Description

The I2C-compatible 2-wire serial interface is used for regulator on/off control, setting output voltages, and other functions. See the *Register Map* section for details.

The I2C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I2C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

### System Configuration

The I2C bus is a multimaster bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 3 shows an example of a typical I2C system. A device on I2C bus that sends data to the bus in called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. When the MAX77812 I2C-compatible interface is operating, it is a slave on I2C bus and it can be both a transmitter and a receiver.

### Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

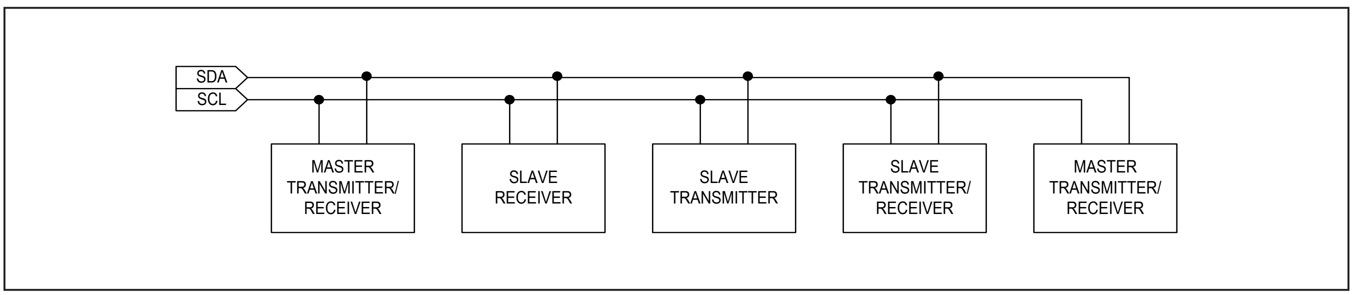



*Figure 3. Functional Logic Diagram for Communications Controller*

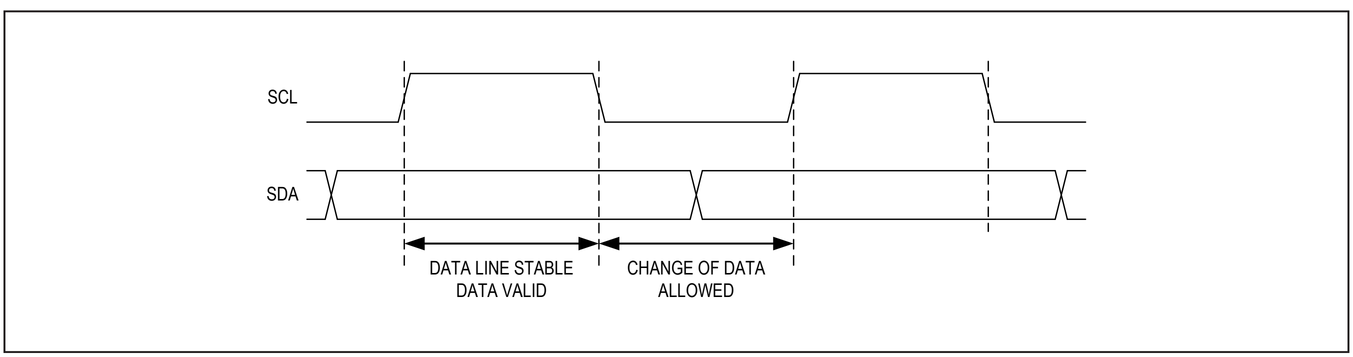



*Figure 4. I2C Bit Transfer*

### START and STOP Conditions

When I2C serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to the MAX77812. The master terminates transmission by issuing a NOT ACKNOWLEDGE followed by a STOP condition.

A STOP condition frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

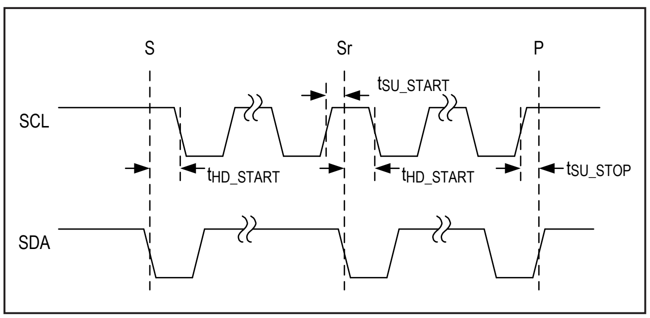



*Figure 5. I2C Start Stop*

When a STOP condition or incorrect address is detected, the MAX77812 internally disconnects SCL from I2C serial interface until the next START condition, minimizing digital noise and feedthrough.

### Acknowledge

Both the I2C bus master and the MAX77812 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a NOT ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

### Slave Address

The I2C slave address is set by buck phase configuration as shown in Table 5. If two MAX77812 devices with the same phase configuration need to be connected to the same I2C bus, contact a Maxim representative.

## Table 5. I2C Slave Address

| PH_CFG2 | PH_CFG1 | PH_CFG0 | SLAVE ADDRESS (7-BIT) | SLAVE ADDRESS (WRITE) | SLAVE ADDRESS (READ) |
|---|---|---|---|---|---|
| **MAX77812EWB+, MAX77812AEWB+, MAX77812BEWB+, MAX77812CEWB+, MAX77812DEWB+** | | | | | |
| Low | Low | Low | 011 0000 | 0x60 (0110 0000) | 0x61 (0110 0001) |
| Low | Low | High | 011 0001 | 0x62 (0110 0010) | 0x63 (0110 0011) |
| Low | High | Low | 011 0010 | 0x64 (0110 0100) | 0x65 (0110 0101) |
| Low | High | High | 011 0011 | 0x66 (0110 0110) | 0x67 (0110 0111) |
| High | X | X | 011 0100 | 0x68 (0110 1000) | 0x69 (0110 1001) |
| **MAX77812FEWB+** | | | | | |
| Low | Low | Low | 011 1000 | 0x70 (0111 0000) | 0x71 (0111 0001) |
| Low | Low | High | 011 1001 | 0x72 (0111 0010) | 0x73 (0111 0011) |
| Low | High | Low | 011 1010 | 0x74 (0111 0100) | 0x75 (0111 0101) |
| Low | High | High | 011 1011 | 0x76 (0111 0110) | 0x77 (0111 0111) |
| High | X | X | 011 1100 | 0x78 (0111 1000) | 0x79 (0111 1001) |

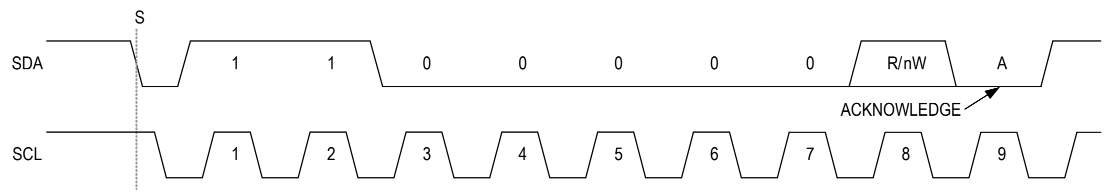



*Figure 6. Slave Address Byte Example*

## Clock Stretching

In general, the clock signal generation for I2C bus is the responsibility of the master device. I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX77812 does not use any form of clock stretching to hold down the clock line.

## General Call Address

The MAX77812 does not implement the I2C specification general call address. If the MAX77812 sees general call address (00000000b), it does not issue an ACKNOWLEDGE (A).

## Communication Speed

The MAX77812 provides an I2C 3.0-compatible (3.4MHz) serial interface.

- I2C Revision 3 Compatible Serial Communications Channel
  - 0Hz to 100kHz (Standard Mode)
  - 0Hz to 400kHz (Fast Mode)
  - 0Hz to 1MHz (Fast Mode Plus)
  - 0Hz to 3.4MHz (High-speed Mode)
- Does not utilize I2C Clock Stretching

Operating in standard mode, fast mode and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds the pullup resistance must be decreased to maintain a reasonable time constant. See the *Pullup Resistor Sizing* section of the I2C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitance of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor is dissipating power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation ($V^2/R$).

Operating in high-speed mode requires some special considerations. For the full list of considerations, see the I2C 3.0 specification. The major considerations with respect to the MAX77812 are:

- I2C bus master use current source pullups to shorten the signal rise times.
- I2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition, the MAX77812 inputs filters are set for standard mode, fast mode, or fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *Protocols* section.

### Communication Protocols

The MAX77812 supports both writing and reading from its registers.

#### Writing to a Single Register

Figure 7 shows the protocol for I2C master device to write one byte of data to the MAX77812. This protocol is the same as SMBus specification's write byte protocol.

The write byte protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

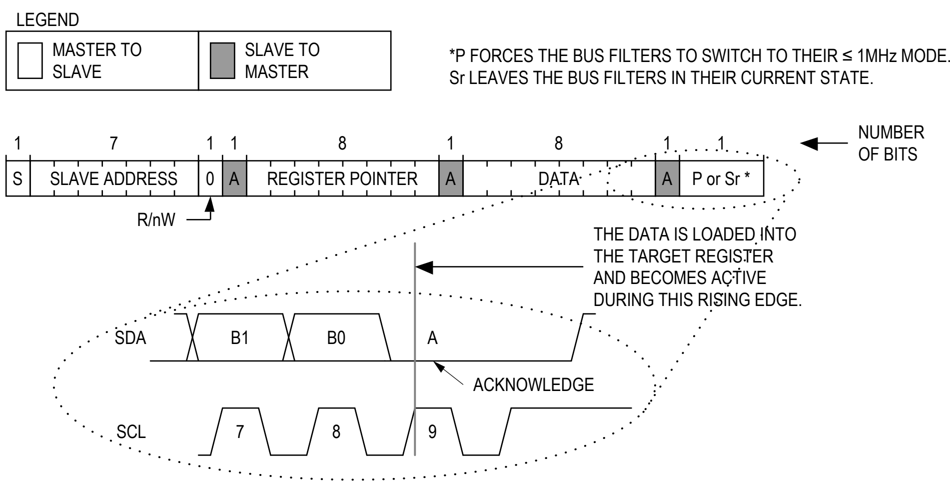



*Figure 7. Writing to a Single Register with Write Byte Protocol*

### Writing to Sequential Registers

Figure 8 shows the protocol for writing to a sequential registers. This protocol is similar to the write byte protocol, except the master continues to write after it receives the first byte of data. When the master is done writing it issues a STOP or REPEATED START

The writing to sequential registers protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit ($R/\overline{W}$ = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8) Steps 6 to 7 are repeated as many times as the master requires.
9) During the last acknowledge related clock pulse, the master issues an ACKNOWLEDGE (A).
10) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

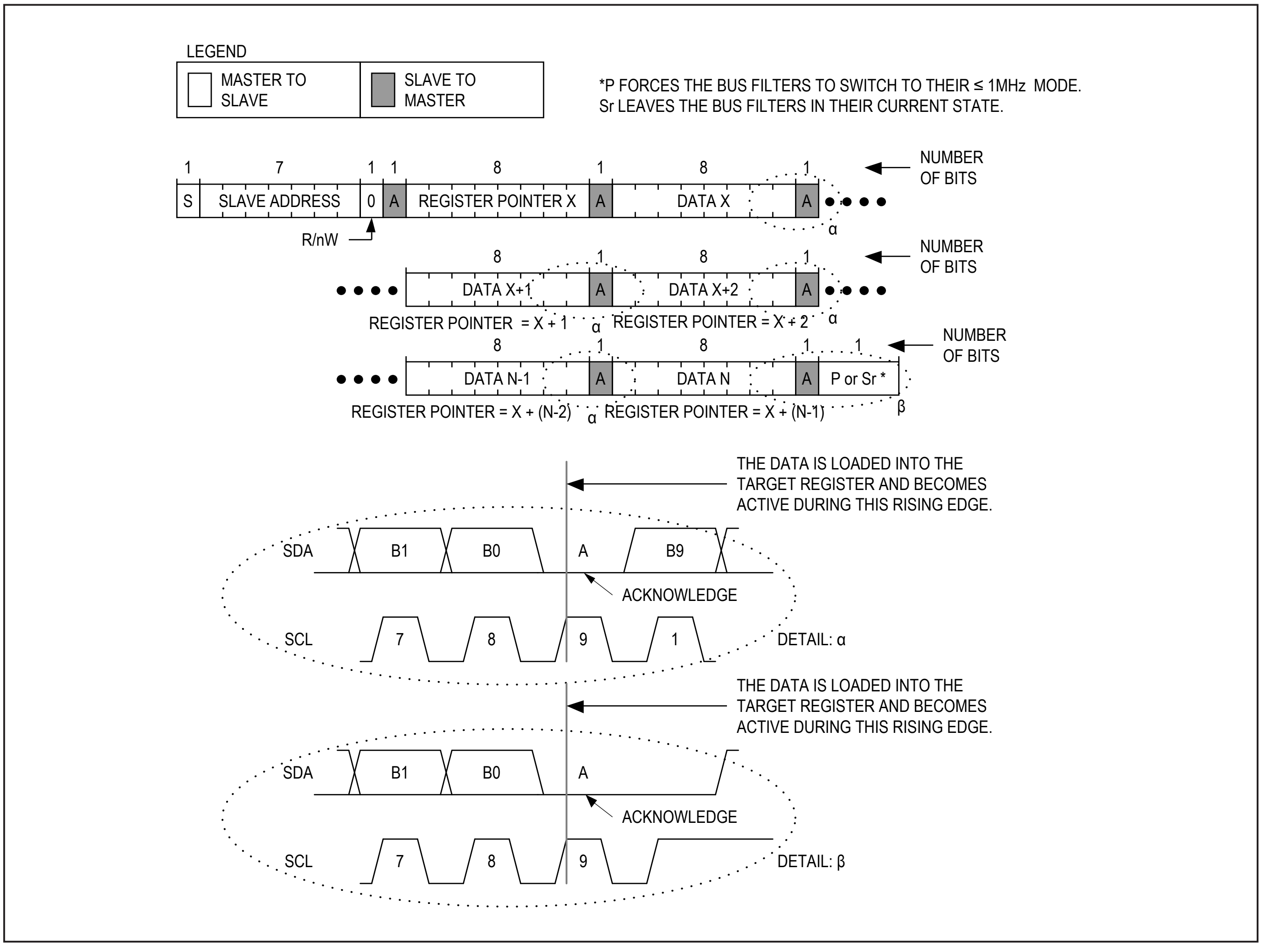



*Figure 8. Writing to Sequential Registers "X" to "N"*

### Writing Multiple Bytes using Register-Data Pairs

Figure 9 shows the protocol for I2C master device to write multiple bytes to the MAX77812 using register-data pairs. This protocol allows I2C master device to address the slave only once and then send data to multiple registers in a random order. Registers may be written continuously until the master issues a STOP condition.

The "Multiple Byte Register-Data Pair" protocol is as follows:

1) The master sends a START command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA LOW.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data will become active.
8) Steps 4 to 7 are repeated as many times as the master requires.
9) The master sends a STOP condition.

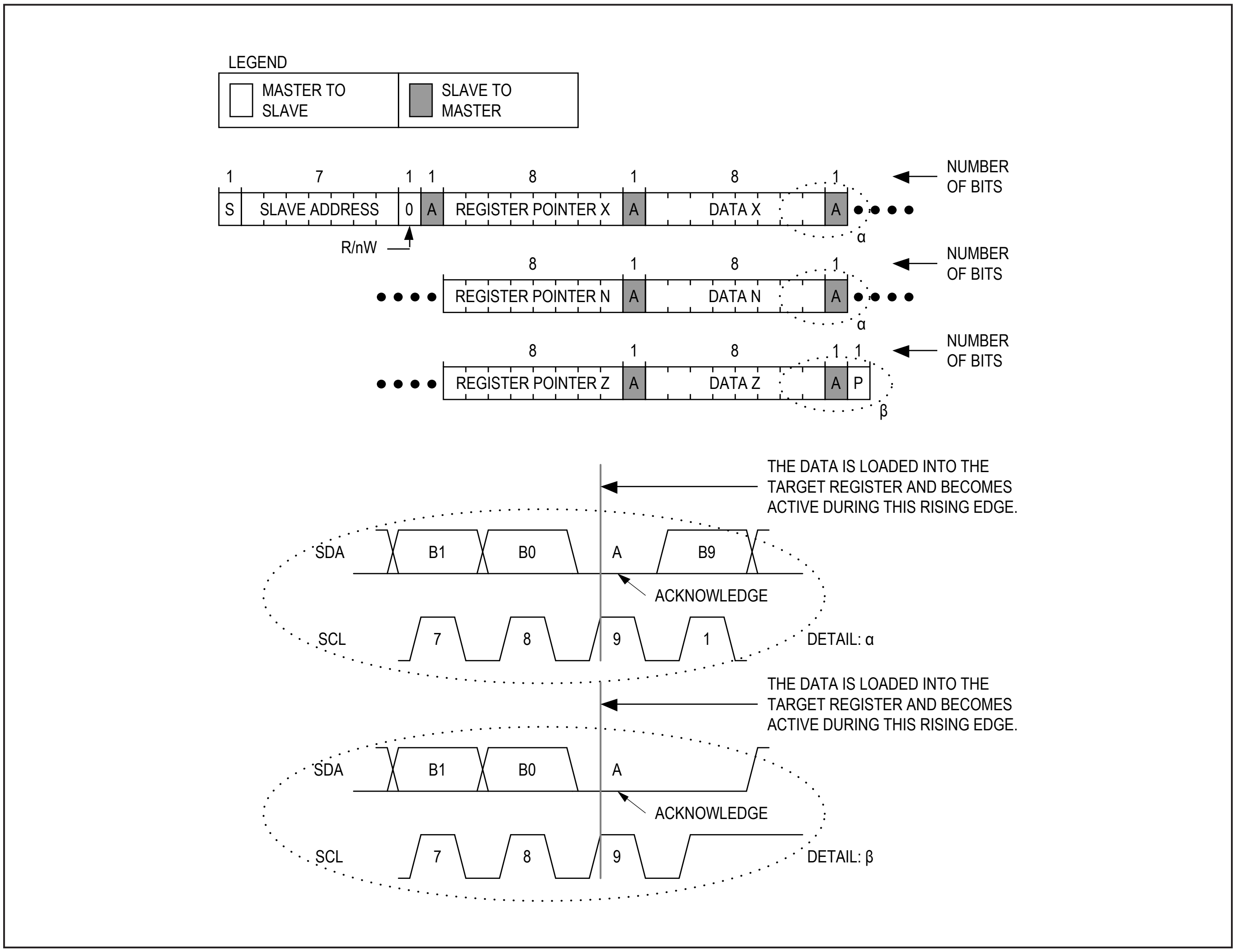



*Figure 9. Writing to Multiple Registers with Multiple Byte Register Data Pairs Protocol*

### Reading from a Single Register

$I^2C$ master device reads one byte of data to the MAX77812. This protocol is the same as SMBus specification's read byte protocol.

The read byte protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit ($R/\overline{W}$ = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit ($R/\overline{W}$ = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues a NOT ACKNOWLEDGE (nA).
11) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus. input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Note that every time the MAX77812 receives a STOP, its register pointer is set to 0x00. If reading register 0x00 after a STOP has been issued, steps 1 to 6 in the above algorithm can be skipped.

### Reading from Sequential Registers

Figure 10 shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data. When the master has all the data it requires, it issues a NOT ACKNOWLEDGE (nA) and a STOP (P) to end the transmission.

The continuous read from sequential registers protocol is as follows:

1) The master sends a START command (S).
2) The master sends the 7-bit slave address followed by a write bit ($R/\overline{W}$ = 0).
3) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START command (Sr).
7) The master sends the 7-bit slave address followed by a read bit ($R/\overline{W}$ = 1).
8) The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9) The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
10) The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11) Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12) The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

Note that every time the MAX77812 receives a STOP its register pointer is set to 0x00. If reading register 0x00 after a STOP has been issued, steps 1 to 6 in the above algorithm can be skipped.

### Engaging HS Mode for Operation Up to 3.4MHz

Figure 11 shows the protocol for engaging HS mode operation. HS mode operation allows for a bus operating speed up to 3.4MHz.

The engaging HS mode protocol is as follows:

1) Begin the protocol while operating at a bus speed of 1MHz or lower.
2) The master sends a START command (S).
3) The master sends the 8-bit master code of 00001xxxb where xxxb are don't care bits.
4) The addressed slave issues a NOT ACKNOWLEDGE (nA).
5) The master can now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master can continue to issue high-speed read/write operations until a STOP (P) is issued. Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation.

The MAX77812 I2C supports the HS mode extension feature. The HS extension feature keeps the high-speed operation even after STOP condition. This eliminates the needs of HS master code issued by the I2C master controller when the I2C master controller wants to stay in HS mode for multiple read/write cycles.

As shown in the state diagram, the HS extension mode can be enabled by setting HS_EXT bit in I2C_CFG register (ADDR 0x15) from LS mode only (entering HS extension mode from HS mode is not supported).

## SPI Slave Controller

The serial interface includes a SPI slave controller and the selection between I2C and SPI slave controller is done by I2C_SPI_SEL input pin. The SPI slave controller requires a reset every time before the SPI master controller starts a new frame. This can be done by setting SCS (SPI chip select, active low) input high for more than 50ns. When SCS is held high, the MISO output is in a high-impedance state.

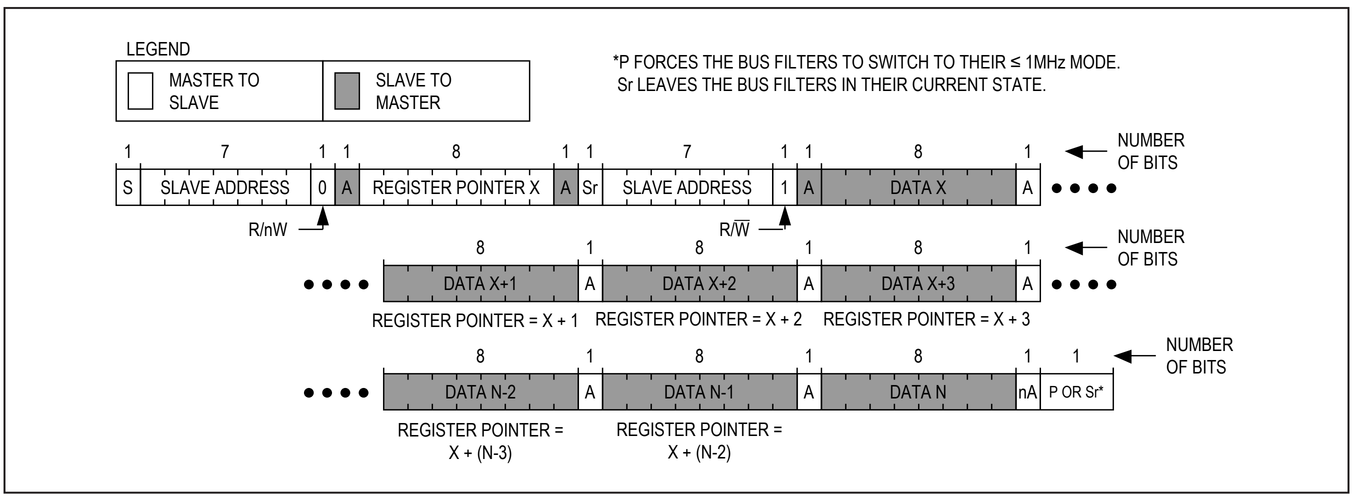



*Figure 10. Reading Continuously from Sequential Registers "X" to "N"*

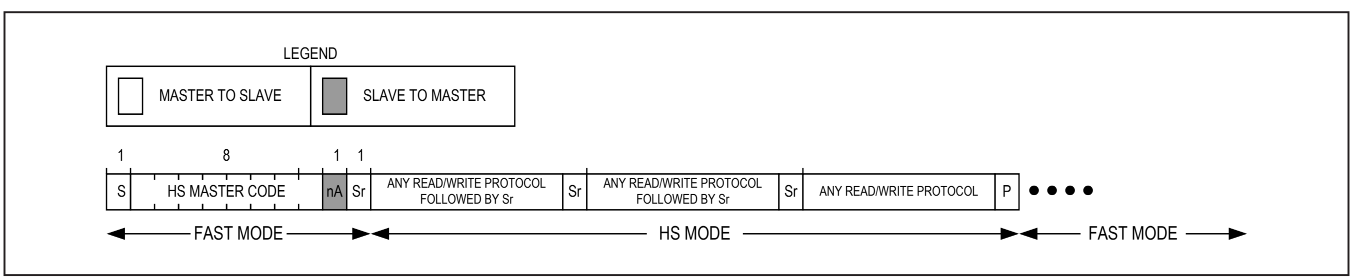



*Figure 11. Engaging HS Mode*

## Features

The SPI slave controller has following features:

- Slave Only
- Single Read/Write Support
- Multiple Read/Write Support
- Up to 30MHz (26MHz typ)

## General Description

The SPI slave controller works with CKPOL = 0, CKPHA = 0 setting in the SPI master controller. In other words, idle state of SCL is low and the SPI controller samples data in the rising edge of SCL. Besides single read/write cycle, the SPI salve controller also supports multiple read/write cycles.

Figure 13, Figure 14, and Figure 15 show single and multiple read/write frame structures.

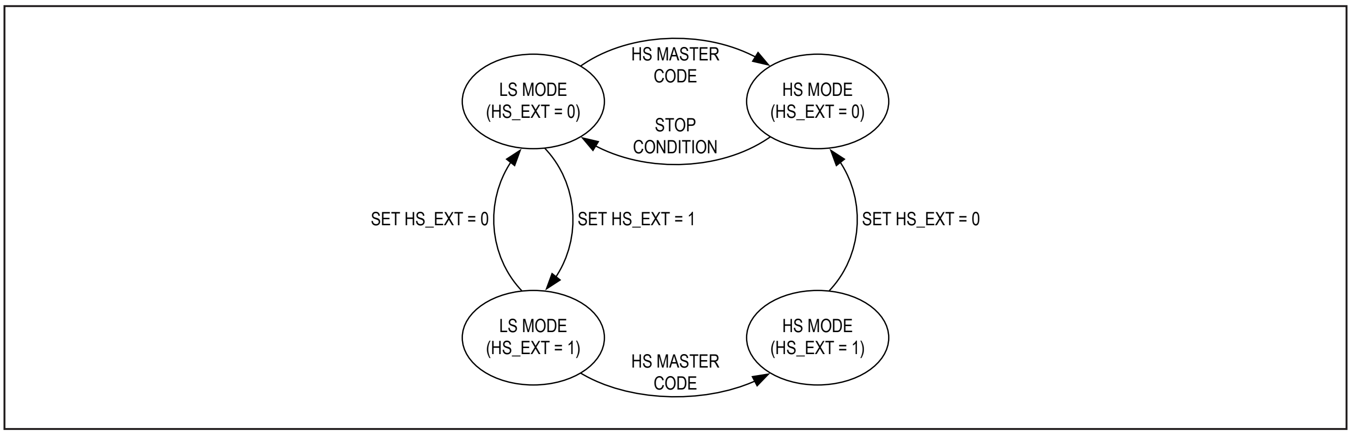



*Figure 12. I2C Operating Mode State Diagram*

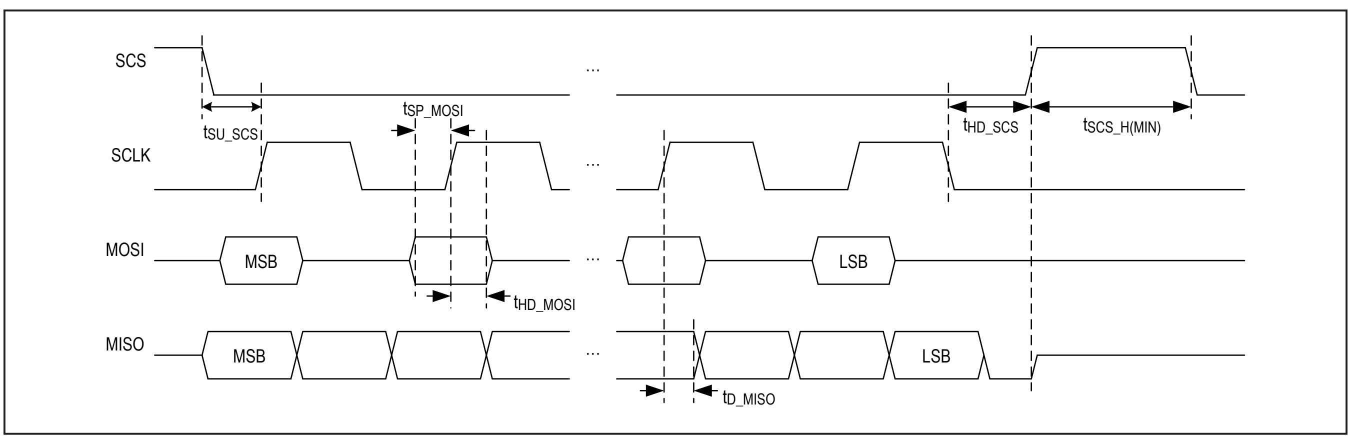



*Figure 13. SPI Timing Diagram*

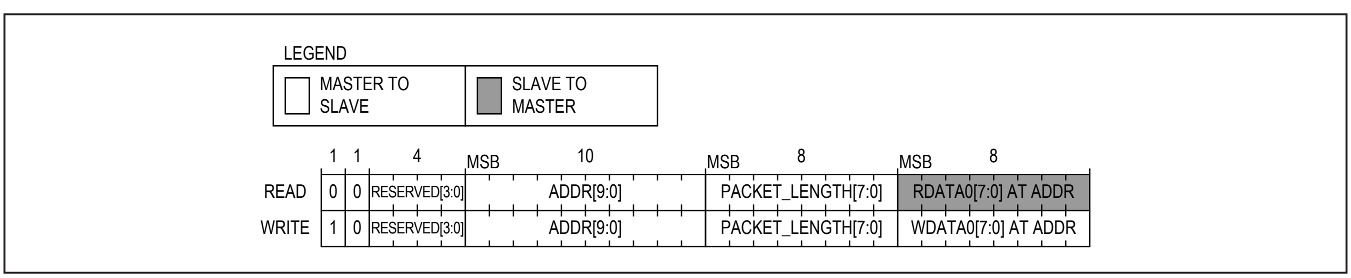



*Figure 14. SPI Single Read/Write Frame Structure*

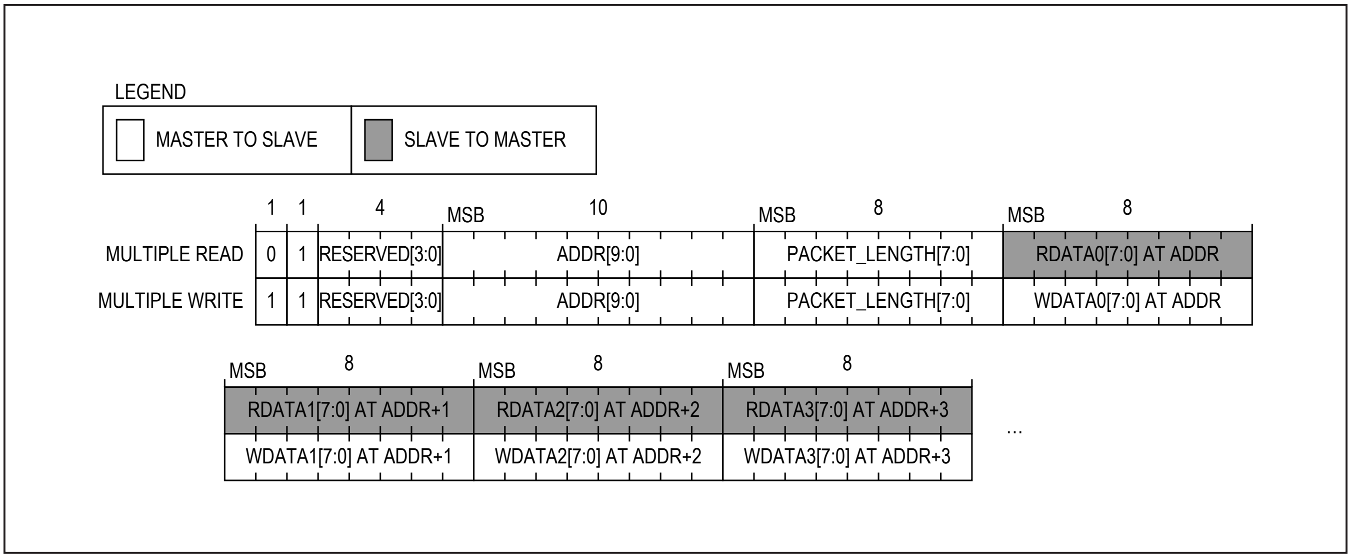



*Figure 15. SPI Multiple Read/Write Frame Structure*

## Frame Structure

### Read/Write Bit (R/$\overline{W}$)

The first bit indicates either read (0) or write (1) frame.

### Single/Multiple Bit (S/M)

The second bit determines either single read/write frame (0) or multiple read/write frame (1).

### Reserved Bits (RESERVED[3:0])

There are 4 reserved bits followed by read/write and single/multiple bits. The MAX77812 SPI slave controller ignores those bits.

### Address Bits (ADDR[9:0])

The SPI master controller loads 10 address bits on MOSI, however, the MAX77812 has only 8-bit address bus so that the SPI slave controller ignores attempt to access to overflowed addresses (beyond 0xFF).

### Packet Length Bits (PACKET_LENGTH[7:0])

The length of single read/write frame is organized as 32-bit (packet length bits are ignored).

For multiple read/write frame, PACKET_LENGTH[7:0] bits determine the number of data bytes. The total length of the multiple read/write frame is ‘32 + 8 x n’ bits, where ‘n’ is the packet length.

### Data Bits (RDATA[7:0]/WDATA[7:0])

The SPI slave controller has 8-bit data bus. While the slave controller is loading data onto MISO, it ignores the data on MOSI. When MISO is inactive, it is held low by the SPI slave controller.

## Multiple Write Cycles

Figure 16 is the timing diagram of multiple write cycle. The first data (WDATA0[7:0]) is written at ADDR[9:0] if the address is valid. For the next data byte, the register address automatically increases by one. The total number of data bytes are determined by PACKET_LENGTH[7:0] and the MAX77812 slave controller ignores the any data bytes beyond the total number of data bytes (PACKET_LENGTH[7:0] + 1). While the SPI master controller is writing data onto MOSI, the SPI controller keeps MISO to a low state.

### Multiple Read Cycles

The timing diagram of multiple read cycle is shown in Figure 17. The first data (RDATA0[7:0]) is read at ADDR[9:0] if the address is valid. For the next data byte, the register address automatically increases by one. The total number of data bytes are determined by PACKET_LENGTH[7:0] and the MAX77812 slave controller stops loading data beyond the total number of data bytes (PACKET_LENGTH[7:0] + 1). While the SPI master controller is writing data onto MOSI, the MAX77812 SPI controller keeps MISO to a low state. When the SPI slave controller loads the data on MISO, the data on MOSI are ignored (don't care) by the SPI slave controller.

In case the SPI master controller tries to read nonexisting registers, the MAX77812 SPI slave controller returns zero values (MISO = low).

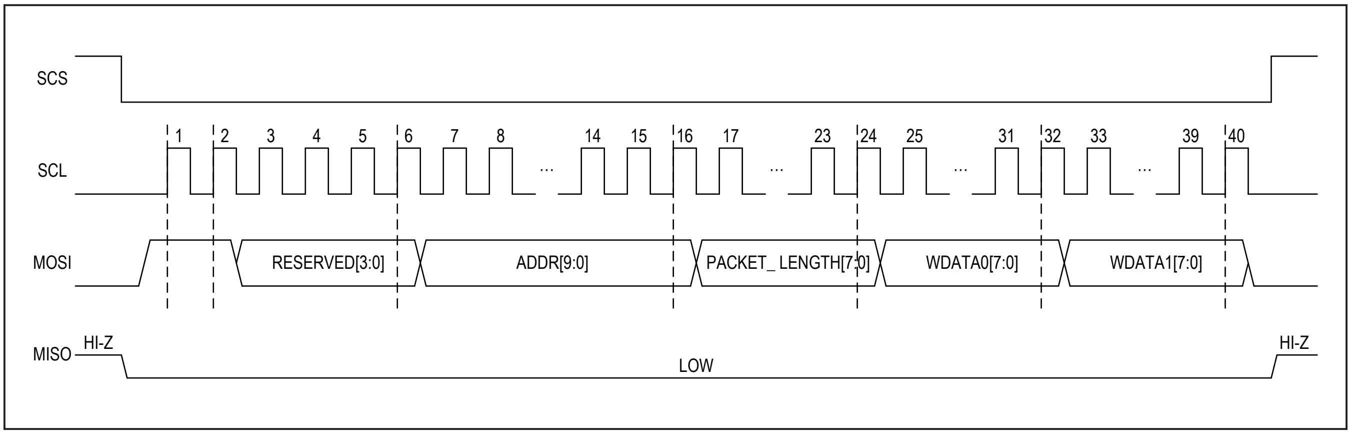



*Figure 16. SPI Multiple Write Cycle*

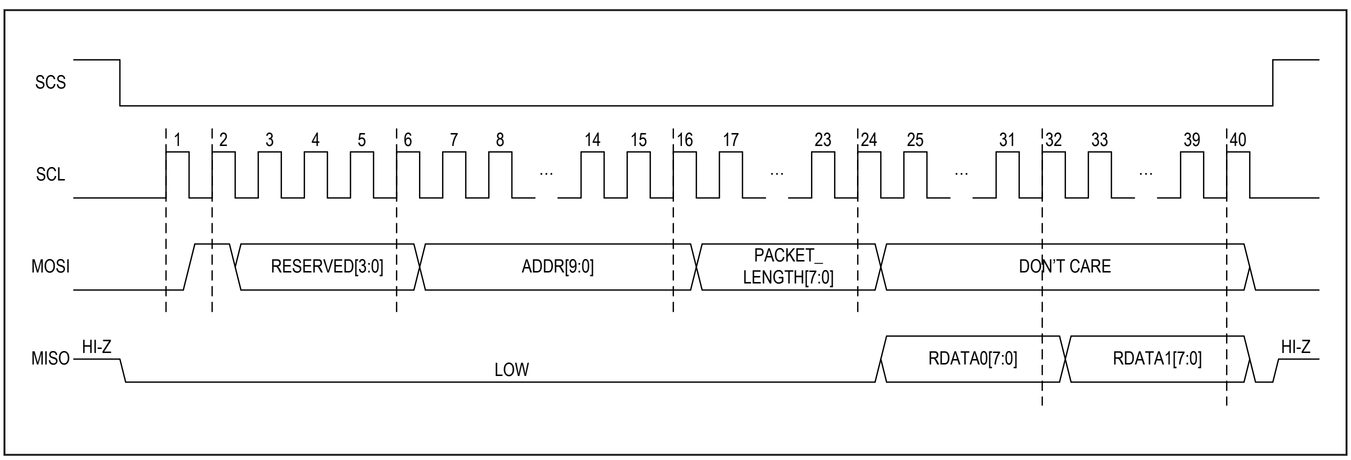



*Figure 17. SPI Multiple Read Cycle*

## PMIC Registers

### Register Reset Conditions

Type-S1: Registers are reset when $V_{SYS}$ < POR (≈1.50V)

Type-O: Registers are reset when $V_{SYS} < V_{UVLO\_F}$ or $V_{VIO} < V_{TH\_VIO\_OK}$ or CE = low or TOK = low or SW_RST = 1.

## Register Map

| ADDR | REGISTER NAME | RESET TYPE | R/W | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | RESET VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | REG_RESET | Type-O | W/C | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | SW_RST | 0x00 |
| 0x01 | INT_SRC | Type-O | R | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | BUCK_INT | TOPSYS_INT | 0x00 |
| 0x02 | INT_SRC_M | Type-O | R/W | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | BUCK_INT_M | TOPSYS_INT_M | 0x02 |
| 0x03 | TOPSYS_INT | Type-S1 | R/C | RESERVED | RESERVED | RESERVED | WDTRSTB_INT | UVLO_INT | TSHDN_INT | TJCT_140C_INT | TJCT_120C_INT | 0x00 |
| 0x04 | TOPSYS_INT_M | Type-O | R/W | RESERVED | RESERVED | RESERVED | WDTRSTB_M | UVLO_M | TSHDN_M | TJCT_140C_M | TJCT_120C_M | 0x13 |
| 0x05 | TOPSYS_STAT | Type-O | R | RESERVED | RESERVED | RESERVED | RESERVED | UVLO | TSHDN | TJCT_140C | TJCT_120C | — |
| 0x06 | EN_CTRL | Type-O | R/W | EN_M4_LPM | EN_M4 | EN_M3_LPM | EN_M3 | EN_M2_LPM | EN_M2 | EN_M1_LPM | EN_M1 | 0x00 |
| 0x07 | STUP_DLY1 | Type-O | R/W | DLY_STEP | RESERVED | RESERVED | M2_STUP_DLY[4:0] | | | | | 0x00 |
| 0x08 | STUP_DLY2 | Type-O | R/W | RESERVED | RESERVED | RESERVED | M3_STUP_DLY[4:0] | | | | | 0x00 |
| 0x09 | STUP_DLY3 | Type-O | R/W | RESERVED | RESERVED | RESERVED | M4_STUP_DLY[4:0] | | | | | 0x00 |
| 0x0A | SHDN_DLY1 | Type-O | R/W | RESERVED | RESERVED | RESERVED | M1_SHDN_DLY[4:0] | | | | | 0x00 |
| 0x0B | SHDN_DLY2 | Type-O | R/W | RESERVED | RESERVED | RESERVED | M2_SHDN_DLY[4:0] | | | | | 0x00 |
| 0x0C | SHDN_DLY3 | Type-O | R/W | RESERVED | RESERVED | RESERVED | M3_SHDN_DLY[4:0] | | | | | 0x00 |
| 0x0D | SHDN_DLY4 | Type-O | R/W | RESERVED | RESERVED | RESERVED | M4_SHDN_DLY[4:0] | | | | | 0x00 |
| 0x0E | WDTRSTB_DEB | Type-O | R/W | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | WDT_DEB[2:0] | | | 0x02 |
| 0x0F | GPI_FUNC | Type-O | R/W | GPI1_FUNC[3:0] | | | | GPI0_FUNC[3:0] | | | | 0x43 |
| 0x10 | GPI_DEB1 | Type-O | R/W | LPM_DEB[2:0] | | | | EN_DEB[2:0] | | | | 0x11 |
| 0x11 | GPI_DEB2 | Type-O | R/W | GPI1_DEB[2:0] | | | | GPI0_DEB[2:0] | | | | 0x11 |
| 0x12 | GPI_PD_CTRL | Type-O | R/W | RESERVED | RESERVED | RESERVED | RESERVED | LPM_PD | EN_PD | GPI1_PD | GPI0_PD | 0x0F |
| 0x13 | PROT_CFG | Type-O | R/W | TSHDN_EN | RESERVED | RESERVED | RESERVED | RESERVED | UVLO_F[2:0] | | | 0x82 |
| 0x15 | I2C_CFG | Type-O | R/W | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | PAIR | HS_EXT | 0x00 |
| 0x16 – 0x1F | RESERVED | | | | | | | | | | | |

## Register Map (continued)

| ADDR | REGISTER NAME | RESET TYPE | R/W | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 | RESET VALUE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x20 | BUCK_INT | Type-S1 | R/C | RESERVED | RESERVED | RESERVED | RESERVED | M4_POKn_INT | M3_POKn_INT | M2_POKn_INT | M1_POKn_INT | 0x00 |
| 0x21 | BUCK_INT_M | Type-O | R/W | RESERVED | RESERVED | RESERVED | RESERVED | M4_POKn_M | M3_POKn_M | M2_POKn_M | M1_POKn_M | 0x0F |
| 0x22 | BUCK_STAT | Type-O | R | RESERVED | RESERVED | RESERVED | RESERVED | M4_POKn | M3_POKn | M2_POKn | M1_POKn | - |
| 0x23 | M1_VOUT | Type-O | R/W | M1_VOUT[7:0] | | | | | | | | 0x50 |
| 0x24 | M2_VOUT | Type-O | R/W | M2_VOUT[7:0] | | | | | | | | 0x50 |
| 0x25 | M3_VOUT | Type-O | R/W | M3_VOUT[7:0] | | | | | | | | 0x46 |
| 0x26 | M4_VOUT | Type-O | R/W | M4_VOUT[7:0] | | | | | | | | 0x46 |
| 0x27 | M1_VOUT_D | Type-O | R/W | M1_VOUT_D[7:0] | | | | | | | | 0x78 |
| 0x28 | M2_VOUT_D | Type-O | R/W | M2_VOUT_D[7:0] | | | | | | | | 0x78 |
| 0x29 | M3_VOUT_D | Type-O | R/W | M3_VOUT_D[7:0] | | | | | | | | 0x78 |
| 0x2A | M4_VOUT_D | Type-O | R/W | M4_VOUT_D[7:0] | | | | | | | | 0x78 |
| 0x2B | M1_VOUT_S | Type-O | R/W | M1_VOUT_S[7:0] | | | | | | | | 0x1E |
| 0x2C | M2_VOUT_S | Type-O | R/W | M2_VOUT_S[7:0] | | | | | | | | 0x1E |
| 0x2D | M3_VOUT_S | Type-O | R/W | M3_VOUT_S[7:0] | | | | | | | | 0x1E |
| 0x2E | M4_VOUT_S | Type-O | R/W | M4_VOUT_S[7:0] | | | | | | | | 0x1E |
| 0x2F | M1_CGF | Type-O | R/W | M1_AD | M1_ILIM[2:0] | | | RESERVED | | M1_FPWM | M1_FSREN | 0xD1 |
| 0x30 | M2_CGF | Type-O | R/W | M2_AD | M2_ILIM[2:0] | | | RESERVED | | M2_FPWM | M2_FSREN | 0xD1 |
| 0x31 | M3_CGF | Type-O | R/W | M3_AD | M3_ILIM[2:0] | | | RESERVED | | M3_FPWM | M3_FSREN | 0xD1 |
| 0x32 | M4_CGF | Type-O | R/W | M4_AD | M4_ILIM[2:0] | | | RESERVED | | M4_FPWM | M4_FSREN | 0xD1 |
| 0x33 | GLB_CFG1 | Type-O | R/W | RESERVED | B_SD_SR[2:0] | | | RESERVED | B_SS_SR[2:0] | | | 0x24 |
| 0x34 | GLB_CFG2 | Type-O | R/W | RESERVED | B_RD_SR[2:0] | | | RESERVED | B_RU_SR[2:0] | | | 0x24 |
| 0x35 | GLB_CFG3 | Type-O | R/W | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | B_PETR_EN | B_NETR_EN | 0x5F |
| 0x36 - 0xFF | RESERVED | | | | | | | | | | | |

**R/W: Read and write*

*R: Read only*

*R/C: Read and clear*

*W/C: Write and clear*

## REG_RESET Register Reset Control Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x00 | W/C | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:1 | RESERVED | 0000 000 | | |
| 0 | SW_RST | 0 | Type-O Register Reset Control<br>1: Reset all Type-O registers to their POR default values.<br>This bit clears to ‘0’ upon reset. | |

## INT_SRC Interrupt Source Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x01 | R | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:2 | RESERVED | 0000 00 | | |
| 1 | BUCK_INT | 0 | 1: Interrupt event on BUCK is detected | |
| 0 | TOPSYS_INT | 0 | 1: Interrupt event on TOPSYS is detected | |

## INT_SRC_M Interrupt Source Mask Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x02 |
|---|---|---|---|---|
| 0x02 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:4 | RESERVED | 0000 00 | | |
| 1 | BUCK_INT_M | 1 | 0: Enable BUCK_INT<br>1: Mask BUCK_INT | |
| 0 | TOPSYS_INT_M | 0 | 0: Enable TOPSYS_INT<br>1: Mask TOPSYS_INT | |

## TOPSYS_INT TOPSYS Interrupt Register

| ADDRESS | MODE | | TYPE: S1 | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x03 | R/C | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:5 | RESERVED | 000 | | |
| 4 | WDTRSTB_INT | 0 | 1: WDTRSTB interrupt has triggered. | |
| 3 | UVLO_INT | 0 | 1: UVLO interrupt has triggered. | |
| 2 | TSHDN_INT | 0 | 1: TSHDN interrupt has triggered. | |
| 1 | TJCT_140C_INT | 0 | 1: TJCT_140C interrupt has triggered. | |
| 0 | TJCT_120C_INT | 0 | 1: TJCT_120C interrupt has triggered. | |

## TOPSYS_INT_M TOPSYS Interrupt Mask Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x13 |
|---|---|---|---|---|
| 0x04 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:5 | RESERVED | 000 | | |
| 4 | WDTRSTB_M | 1 | 0: Enable WDTRSTB_INT.<br>1: Mask WDTRSTB_INT. | |
| 3 | UVLO_M | 0 | 0: Enable UVLO_INT.<br>1: Mask UVLO_INT. | |
| 2 | TSHDN_M | 0 | 0: Enable TSHDN_INT.<br>1: Mask TSHDN_INT. | |
| 1 | TJCT_140C_M | 1 | 0: Enable TJCT_140C_INT.<br>1: Mask TJCT_140C_INT. | |
| 0 | TJCT_120C_M | 1 | 0: Enable TJCT_120C_INT.<br>1: Mask TJCT_120C_INT. | |

## TOPSYS_STAT TOPSYS Status Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: N/A |
|---|---|---|---|---|
| 0x05 | R | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:4 | RESERVED | — | | |
| 3 | UVLO | — | 0: $V_{SYS} \geq V_{UVLO\_F}$<br>1: $V_{SYS} < V_{UVLO\_F}$ | |
| 2 | TSHDN | — | 0: Junction Temperature ($T_{JCT}$) ≤ +165°C<br>1: Junction Temperature ($T_{JCT}$) > +165°C | |
| 1 | TJCT_140C | — | 0: Junction Temperature ($T_{JCT}$) ≤ +140°C<br>1: Junction Temperature ($T_J$CT) > +140°C | |
| 0 | TJCT_120C | — | 0: Junction Temperature ($T_{JCT}$) ≤ +120°C<br>1: Junction Temperature ($T_{JCT}$) > +120°C | |

## EN_CTRL Regulator Enable Control Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x06 | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7 | EN_M4_LPM | 0 | 0: Disable BUCK Master 4 low power mode.<br>1: Enable BUCK Master 4 low power mode. | |
| 6 | EN_M4 | 0 | 0: Disable BUCK Master 4 output.<br>1: Enable BUCK Master 4 output (‘OR’ logic with GPIx input). | |
| 5 | EN_M3_LPM | 0 | 0: Disable BUCK Master 3 low power mode.<br>1: Enable BUCK Master 3 low power mode. | |
| 4 | EN_M3 | 0 | 0: Disable BUCK Master 3 output.<br>1: Enable BUCK Master 3 output (‘OR’ logic with GPIx input). | |
| 3 | EN_M2_LPM | 0 | 0: Disable BUCK Master 2 low power mode.<br>1: Enable BUCK Master 2 low power mode. | |
| 2 | EN_M2 | 0 | 0: Disable BUCK Master 2 output.<br>1: Enable BUCK Master 2 output (‘OR’ logic with GPIx input). | |
| 1 | EN_M1_LPM | 0 | 0: Disable BUCK Master 1 low power mode.<br>1: Enable BUCK Master 1 low power mode. | |
| 0 | EN_M1 | 0 | 0: Disable BUCK Master 1 output.<br>1: Enable BUCK Master 1 output (‘OR’ logic with GPIx input). | |

## STUP_DLY1 Global Startup Delay Setting Register 1

| ADDRESS | MODE | | TYPE: O (OTP) | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x07 | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7 | DLY_STEP | 0 | Delay Time Step Selection<br>0: 1ms<br>1: 2ms | |
| 6:5 | RESERVED | 00 | | |
| 4:0 | M2_STUP_DLY[4:0] | 0 0000 | BUCK Master 2 Startup Delay Time Setting (Delay from Rising Edge of EN Pin or GLB_EN)<br>0 0000b = 0ms<br>0 0001b = 1 x DLY_STEP<br>0 0010b = 2 x DLY_STEP<br>. .<br>. .<br>. .<br>1 1110b = 30 x DLY_STEP<br>1 1111b = 31 x DLY_STEP | |

## STUP_DLY2 Global Startup Delay Setting Register 2

| ADDRESS | MODE | | TYPE: O (OTP) | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x08 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:5 | RESERVED | 000 | | |
| 4:0 | M3_STUP_DLY[4:0] | 0 0000 | BUCK Master 3 Startup Delay Time Setting (Delay from Rising Edge of EN Pin or GLB_EN)<br>0 0000b = 0ms<br>0 0001b = 1 x DLY_STEP<br>0 0010b = 2 x DLY_STEP<br>. .<br>. .<br>. .<br>1 1110b = 30 x DLY_STEP<br>1 1111b = 31 x DLY_STEP | |

## STUP_DLY3 Global Startup Delay Setting Register 3

| ADDRESS | MODE | | TYPE: O (OTP) | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x09 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:5 | RESERVED | 000 | | |
| 4:0 | M4_STUP_DLY[4:0] | 0 0000 | BUCK Master 4 Startup Delay Time Setting (Delay from Rising Edge of EN Pin or GLB_EN)<br>0 0000b = 0ms<br>0 0001b = 1 x DLY_STEP<br>0 0010b = 2 x DLY_STEP<br>. .<br>. .<br>. .<br>1 1110b = 30 x DLY_STEP<br>1 1111b = 31 x DLY_STEP | |

## SHDN_DLY1 Global Shutdown Delay Setting Register 1

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x0A | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:5 | RESERVED | 000 | | |
| 4:0 | M1_SHDN_DLY[4:0] | 0 0000 | BUCK Master 1 Shutdown Delay Time Setting (Delay from Falling Edge of EN Pin or GLB_EN)<br>0 0000b = 0ms<br>0 0001b = 1 x DLY_STEP<br>0 0010b = 2 x DLY_STEP<br>. .<br>. .<br>. .<br>1 1110b = 30 x DLY_STEP<br>1 1111b = 31 x DLY_STEP | |

## SHDN_DLY2 Global Shutdown Delay Setting Register 2

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x0B | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:5 | RESERVED | 000 | | |
| 4:0 | M2_SHDN_DLY[4:0] | 0 0000 | BUCK Master 2 Shutdown Delay Time Setting (Delay from Falling Edge of EN Pin or GLB_EN)<br>0 0000b = 0ms<br>0 0001b = 1 x DLY_STEP<br>0 0010b = 2 x DLY_STEP<br>. .<br>. .<br>. .<br>1 1110b = 30 x DLY_STEP<br>1 1111b = 31 x DLY_STEP | |

## SHDN_DLY3 Global Shutdown Delay Setting Register 3

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x0C | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:5 | RESERVED | 000 | | |
| 4:0 | M3_SHDN_DLY[4:0] | 0 0000 | BUCK Master 3 Shutdown Delay Time Setting (Delay from Falling Edge of EN Pin or GLB_EN)<br>0 0000b = 0ms<br>0 0001b = 1 x DLY_STEP<br>0 0010b = 2 x DLY_STEP<br>. .<br>. .<br>. .<br>1 1110b = 30 x DLY_STEP<br>1 1111b = 31 x DLY_STEP | |

## SHDN_DLY4 Global Shutdown Delay Setting Register 4

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x0D | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:5 | RESERVED | 000 | | |
| 4:0 | M4_SHDN_DLY[4:0] | 0 0000 | BUCK Master 4 Shutdown Delay Time Setting (Delay from Falling Edge of EN Pin or GLB_EN)<br>0 0000b = 0ms<br>0 0001b = 1 x DLY_STEP<br>0 0010b = 2 x DLY_STEP<br>. .<br>. .<br>. .<br>1 1110b = 30 x DLY_STEP<br>1 1111b = 31 x DLY_STEP | |

## WDTRSTB_DEB WDTRSTB_IN Input Debounce Time Setting Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x02 |
|---|---|---|---|---|
| 0x0E | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7:3 | RESERVED | 0000 0 | | |
| 2:0 | WDT_DEB[2:0] | 010 | WDTRSTB_IN Debounce Time Setting<br>000b = 0ms<br>001b = 0.8ms<br>010b = 1.6ms<br>011b = 3.2ms<br>100b = 6.4ms<br>101b = 12.8ms<br>111b = 51.2ms | |

## GPI_FUNC GPI Function Selection Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x43 |
|---|---|---|---|---|
| 0x0F | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7:4 | GPI1_FUNC[3:0] | 0100 | GPI1 Function Selection<br>0000b: GLB_EN 1000b: M3_VSEL<br>0001b: M1_EN 1001b: M4_VSEL<br>0010b: M2_EN 1010b: GLB_LPM<br>0011b: M3_EN 1011b: M1_LPM<br>0100b: M4_EN 1100b: M2_LPM<br>0101b: GLB_VSEL 1101b: M3_LPM<br>0110b: M1_VSEL 1110b: M4_LPM<br>0111b: M2_VSEL 1111b: No Function | |
| 3:0 | GPI0_FUNC[3:0] | 0011 | GPI0 Function Selection<br>0000b: GLB_EN 1000b: M3_VSEL<br>0001b: M1_EN 1001b: M4_VSEL<br>0010b: M2_EN 1010b: GLB_LPM<br>0011b: M3_EN 1011b: M1_LPM<br>0100b: M4_EN 1100b: M2_LPM<br>0101b: GLB_VSEL 1101b: M3_LPM<br>0110b: M1_VSEL 1110b: M4_LPM<br>0111b: M2_VSEL 1111b: No Function | |

## GPI_DEB1 GPI Debounce Time Setting Register 1

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x11 |
|---|---|---|---|---|
| 0x10 | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7:4 | LPM_DEB[3:0] | 0001 | LPM Debounce Time Setting<br>0000b = 0µs 1000b = 512µs<br>0001b = 64µs 1001b = 576µs<br>0010b = 128µs 1010b = 640µs<br>0011b = 192µs 1011b = 704µs<br>0100b = 256µs 1100b = 768µs<br>0101b = 320µs 1101b = 832µs<br>0110b = 384µs 1110b = 896µs<br>0111b = 448µs 1111b = 960µs | |
| 3:0 | EN_DEB[3:0] | 0001 | EN Debounce Time Setting<br>0000b = 0µs 1000b = 512µs<br>0001b = 64µs 1001b = 576µs<br>0010b = 128µs 1010b = 640µs<br>0011b = 192µs 1011b = 704µs<br>0100b = 256µs 1100b = 768µs<br>0101b = 320µs 1101b = 832µs<br>0110b = 384µs 1110b = 896µs<br>0111b = 448µs 1111b = 960µs | |

## GPI_DEB2 GPI Debounce Time Setting Register 2

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x11 |
|---|---|---|---|---|
| 0x11 | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7:4 | GPI1_DEB[3:0] | 0001 | GPI1 Debounce Time Setting<br>0000b = 0µs 1000b = 512µs<br>0001b = 64µs 1001b = 576µs<br>0010b = 128µs 1010b = 640µs<br>0011b = 192µs 1011b = 704µs<br>0100b = 256µs 1100b = 768µs<br>0101b = 320µs 1101b = 832µs<br>0110b = 384µs 1110b = 896µs<br>0111b = 448µs 1111b = 960µs | |
| 3:0 | GPI0_DEB[3:0] | 0001 | GPI0 Debounce Time Setting<br>0000b = 0µs 1000b = 512µs<br>0001b = 64µs 1001b = 576µs<br>0010b = 128µs 1010b = 640µs<br>0011b = 192µs 1011b = 704µs<br>0100b = 256µs 1100b = 768µs<br>0101b = 320µs 1101b = 832µs<br>0110b = 384µs 1110b = 896µs<br>0111b = 448µs 1111b = 960µs | |

## GPI_PD_CTRL GPI Pulldown Resistor Control Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x0F |
|---|---|---|---|---|
| 0x12 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:4 | RESERVED | 0000 | | |
| 3 | LPM_PD | 1 | LPM Input Pulldown Resistor Enable Setting<br>0: Disable<br>1: Enable | |
| 2 | EN_PD | 1 | EN Input Pulldown Resistor Enable Setting<br>0: Disable<br>1: Enable | |
| 1 | GPI1_PD | 1 | GPI1 Input Pulldown Resistor Enable Setting<br>0: Disable<br>1: Enable | |
| 0 | GPI0_PD | 1 | GPI0 Input Pulldown Resistor Enable Setting<br>0: Disable<br>1: Enable | |

## PROT_CFG Protection Configuration Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x82 |
|---|---|---|---|---|
| 0x13 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7 | TSHDN_EN | 1 | Thermal Protection Enable Control<br>0: Disable (TSHDN_INT is not disabled)<br>1: Enable | |
| 6:3 | RESERVED | 000 0 | | |
| 2:0 | UVLO_F[2:0] | 010 | $V_{SYS}$ UVLO Falling Threshold<br>000b = 1.95V<br>001b = 2.05V<br>010b = 2.15V<br>011b = 2.25V<br>100b = 2.35V<br>101b = 2.45V<br>110b = 2.55V<br>111b = Disabled | |

*0x14: RESERVED*

## I2C_CFG I²C Configuration Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x15 | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7:4 | RESERVED | NA | | |
| 3:2 | RESERVED | 00 | Write ‘00’ | |
| 1 | PAIR | 0 | Register Data Pair Mode<br>0: Disable (Sequential Mode)<br>1: Enable | |
| 0 | HS_EXT | 0 | HS Mode Extension<br>0: Disable HS mode extension (I²C Rev. 4 Compliant).<br>1: Enable HS mode extension.<br>(HS mode is extended during/after ‘STOP’ condition.) | |

*0x16 – 0x1F: RESERVED*

## BUCK_INT Regulators Interrupt Register

| ADDRESS | MODE | | TYPE: S1 | RESET VALUE: 0x00 |
|---|---|---|---|---|
| 0x20 | R/C | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7:4 | RESERVED | 0000 | | |
| 3 | M4_$\overline{\text{POK}}$_INT | 0 | 1: BUCK Master 4 $\overline{\text{POK}}$ interrupt has triggered. | |
| 2 | M3_$\overline{\text{POK}}$ _INT | 0 | 1: BUCK Master 3 $\overline{\text{POK}}$ interrupt has triggered. | |
| 1 | M2_$\overline{\text{POK}}$ _INT | 0 | 1: BUCK Master 2 $\overline{\text{POK}}$ interrupt has triggered. | |
| 0 | M1_$\overline{\text{POK}}$ _INT | 0 | 1: BUCK Master 1 $\overline{\text{POK}}$ interrupt has triggered. | |

## BUCK_INT_M BUCK Interrupt Mask Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x0F |
|---|---|---|---|---|
| 0x21 | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7:4 | RESERVED | 0000 | | |
| 3 | M4_$\overline{\text{POK}}$ _M | 1 | 0: Enable M4_$\overline{\text{POK}}$ _INT.<br>1: Mask M4_$\overline{\text{POK}}$ _INT. | |
| 2 | M3_$\overline{\text{POK}}$_M | 1 | 0: Enable M3_ $\overline{\text{POK}}$_INT.<br>1: Mask M3_$\overline{\text{POK}}$_INT. | |
| 1 | M2_$\overline{\text{POK}}$_M | 1 | 0: Enable M2_ $\overline{\text{POK}}$_INT.<br>1: Mask M2_$\overline{\text{POK}}$_INT. | |
| 0 | M1_$\overline{\text{POK}}$_M | 1 | 0: Enable M1_$\overline{\text{POK}}$_INT.<br>1: Mask M1_$\overline{\text{POK}}$_INT. | |

## BUCK_STAT BUCK Status Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: N/A |
|---|---|---|---|---|
| 0x22 | R | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:4 | RESERVED | 0000 | | |
| 3 | M4_$\overline{\text{POK}}$ | 0 | BUCK Master 4 $\overline{\text{POK}}$ Status | |
| 2 | M3_$\overline{\text{POK}}$ | 0 | BUCK Master 3 $\overline{\text{POK}}$ Status | |
| 1 | M2_$\overline{\text{POK}}$ | 0 | BUCK Master 2 $\overline{\text{POK}}$ Status | |
| 0 | M1_$\overline{\text{POK}}$ | 0 | BUCK Master 1 $\overline{\text{POK}}$ Status | |

## M1_VOUT BUCK Master1 Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O (OTP) | RESET VALUE: 0x50 |
|---|---|---|---|---|
| 0x23 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M1_VOUT[7:0] | 01010000 | BUCK Master 1 Output Voltage | |

## M2_VOUT BUCK Master 2 Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O (OTP) | RESET VALUE: 0x50 |
|---|---|---|---|---|
| 0x24 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M2_VOUT[7:0] | 01010000 | BUCK Master 2 Output Voltage | |

## M3_VOUT BUCK Master 3 Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O (OTP) | RESET VALUE: 0x46 |
|---|---|---|---|---|
| 0x25 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M3_VOUT[7:0] | 01000110 | BUCK Master 3 Output Voltage | |

## M4_VOUT BUCK Master 4 Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O (OTP) | RESET VALUE: 0x46 |
|---|---|---|---|---|
| 0x26 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M4_VOUT[7:0] | 01000110 | BUCK Master 4 Output Voltage | |

## M1_VOUT_D BUCK Master 1 Default Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x78 |
|---|---|---|---|---|
| 0x27 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M1_VOUT_D[7:0] | 0111 1000 | Buck Master 1 Default Output Voltage. Sets the output voltage when DVS = 1 through a GPI. | |

## M2_VOUT_D BUCK Master 2 Default Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x78 |
|---|---|---|---|---|
| 0x28 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M2_VOUT_D[7:0] | 0111 1000 | Buck Master 2 Default Output Voltage. Sets the output voltage when DVS = 1 through a GPI. | |

## M3_VOUT_D BUCK Master 3 Default Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x78 |
|---|---|---|---|---|
| 0x29 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M3_VOUT_D[7:0] | 0111 1000 | Buck Master 3 Default Output Voltage. Sets the output voltage when DVS = 1 through a GPI. | |

## M4_VOUT_D BUCK Master 4 Default Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x78 |
|---|---|---|---|---|
| 0x2A | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M4_VOUT_D[7:0] | 0111 1000 | Buck Master 4 Default Output Voltage. Sets the output voltage when DVS = 1 through a GPI. | |

## M1_VOUT_S BUCK Master1 Sleep Mode Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x1E |
|---|---|---|---|---|
| 0x2B | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M1_VOUT_S[7:0] | 0001 1110 | Buck Master 1 Sleep Mode Output Voltage. Sets the output voltage when DVS = 0 through a GPI. | |

## M2_VOUT_S BUCK Master 2 Sleep Mode Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x1E |
|---|---|---|---|---|
| 0x2C | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M2_VOUT_S[7:0] | 0001 1110 | Buck Master 2 Sleep Mode Output Voltage. Sets the output voltage when DVS = 0 through a GPI. | |

## M3_VOUT_S BUCK Master 3 Sleep Mode Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x1E |
|---|---|---|---|---|
| 0x2D | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M3_VOUT_S[7:0] | 0001 1110 | Buck Master 3 Sleep Mode Output Voltage. Sets the output voltage when DVS = 0 through a GPI. | |

## M4_VOUT_S BUCK Master 4 Sleep Mode Output Voltage Setting Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x1E |
|---|---|---|---|---|
| 0x2E | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7:0 | M4_VOUT_S[7:0] | 0001 1110 | Buck Master 4 Sleep Mode Output Voltage. Sets the output voltage when DVS = 0 through a GPI. | |

## Buck Output Voltage Table

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0x00 = 0.25000V | 0x20 = 0.41000V | 0x40 = 0.57000V | 0x60 = 0.73000V | 0x80 = 0.89000V | 0xA0 = 1.05000V | 0xC0 = 1.21000V | 0xE0 = 1.37000V |
| 0x01 = 0.25500V | 0x21 = 0.41500V | 0x41 = 0.57500V | 0x61 = 0.73500V | 0x81 = 0.89500V | 0xA1 = 1.05500V | 0xC1 = 1.21500V | 0xE1 = 1.37500V |
| 0x02 = 0.26000V | 0x22 = 0.42000V | 0x42 = 0.58000V | 0x62 = 0.74000V | 0x82 = 0.90000V | 0xA2 = 1.06000V | 0xC2 = 1.22000V | 0xE2 = 1.38000V |
| 0x03 = 0.26500V | 0x23 = 0.42500V | 0x43 = 0.58500V | 0x63 = 0.74500V | 0x83 = 0.90500V | 0xA3 = 1.06500V | 0xC3 = 1.22500V | 0xE3 = 1.38500V |
| 0x04 = 0.27000V | 0x24 = 0.43000V | 0x44 = 0.59000V | 0x64 = 0.75000V | 0x84 = 0.91000V | 0xA4 = 1.07000V | 0xC4 = 1.23000V | 0xE4 = 1.39000V |
| 0x05 = 0.27500V | 0x25 = 0.43500V | 0x45 = 0.59500V | 0x65 = 0.75500V | 0x85 = 0.91500V | 0xA5 = 1.07500V | 0xC5 = 1.23500V | 0xE5 = 1.39500V |
| 0x06 = 0.28000V | 0x26 = 0.44000V | 0x46 = 0.60000V | 0x66 = 0.76000V | 0x86 = 0.92000V | 0xA6 = 1.08000V | 0xC6 = 1.24000V | 0xE6 = 1.40000V |
| 0x07 = 0.28500V | 0x27 = 0.44500V | 0x47 = 0.60500V | 0x67 = 0.76500V | 0x87 = 0.92500V | 0xA7 = 1.08500V | 0xC7 = 1.24500V | 0xE7 = 1.40500V |
| 0x08 = 0.29000V | 0x28 = 0.45000V | 0x48 = 0.61000V | 0x68 = 0.77000V | 0x88 = 0.93000V | 0xA8 = 1.09000V | 0xC8 = 1.25000V | 0xE8 = 1.41000V |
| 0x09 = 0.29500V | 0x29 = 0.45500V | 0x49 = 0.61500V | 0x69 = 0.77500V | 0x89 = 0.93500V | 0xA9 = 1.09500V | 0xC9 = 1.25500V | 0xE9 = 1.41500V |
| 0x0A = 0.30000V | 0x2A = 0.46000V | 0x4A = 0.62000V | 0x6A = 0.78000V | 0x8A = 0.94000V | 0xAA = 1.10000V | 0xCA = 1.26000V | 0xEA = 1.42000V |
| 0x0B = 0.30500V | 0x2B = 0.46500V | 0x4B = 0.62500V | 0x6B = 0.78500V | 0x8B = 0.94500V | 0xAB = 1.10500V | 0xCB = 1.26500V | 0xEB = 1.42500V |
| 0x0C = 0.31000V | 0x2C = 0.47000V | 0x4C = 0.63000V | 0x6C = 0.79000V | 0x8C = 0.95000V | 0xAC = 1.11000V | 0xCC = 1.27000V | 0xEC = 1.43000V |
| 0x0D = 0.31500V | 0x2D = 0.47500V | 0x4D = 0.63500V | 0x6D = 0.79500V | 0x8D = 0.95500V | 0xAD = 1.11500V | 0xCD = 1.27500V | 0xED = 1.43500V |

## Buck Output Voltage Table (continued)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 0x0E = 0.32000V | 0x2E = 0.48000V | 0x4E = 0.64000V | 0x6E = 0.80000V | 0x8E = 0.96000V | 0xAE = 1.12000V | 0xCE = 1.28000V | 0xEE = 1.44000V |
| 0x0F = 0.32500V | 0x2F = 0.48500V | 0x4F = 0.64500V | 0x6F = 0.80500V | 0x8F = 0.96500V | 0xAF = 1.12500V | 0xCF = 1.28500V | 0xEF = 1.44500V |
| 0x10 = 0.33000V | 0x30 = 0.49000V | 0x50 = 0.65000V | 0x70 = 0.81000V | 0x90 = 0.97000V | 0xB0 = 1.13000V | 0xD0 = 1.29000V | 0xF0 = 1.45000V |
| 0x11 = 0.33500V | 0x31 = 0.49500V | 0x51 = 0.65500V | 0x71 = 0.81500V | 0x91 = 0.97500V | 0xB1 = 1.13500V | 0xD1 = 1.29500V | 0xF1 = 1.45500V |
| 0x12 = 0.34000V | 0x32 = 0.50000V | 0x52 = 0.66000V | 0x72 = 0.82000V | 0x92 = 0.98000V | 0xB2 = 1.14000V | 0xD2 = 1.30000V | 0xF2 = 1.46000V |
| 0x13 = 0.34500V | 0x33 = 0.50500V | 0x53 = 0.66500V | 0x73 = 0.82500V | 0x93 = 0.98500V | 0xB3 = 1.14500V | 0xD3 = 1.30500V | 0xF3 = 1.46500V |
| 0x14 = 0.35000V | 0x34 = 0.51000V | 0x54 = 0.67000V | 0x74 = 0.83000V | 0x94 = 0.99000V | 0xB4 = 1.15000V | 0xD4 = 1.31000V | 0xF4 = 1.47000V |
| 0x15 = 0.35500V | 0x35 = 0.51500V | 0x55 = 0.67500V | 0x75 = 0.83500V | 0x95 = 0.99500V | 0xB5 = 1.15500V | 0xD5 = 1.31500V | 0xF5 = 1.47500V |
| 0x16 = 0.36000V | 0x36 = 0.52000V | 0x56 = 0.68000V | 0x76 = 0.84000V | 0x96 = 1.00000V | 0xB6 = 1.16000V | 0xD6 = 1.32000V | 0xF6 = 1.48000V |
| 0x17 = 0.36500V | 0x37 = 0.52500V | 0x57 = 0.68500V | 0x77 = 0.84500V | 0x97 = 1.00500V | 0xB7 = 1.16500V | 0xD7 = 1.32500V | 0xF7 = 1.48500V |
| 0x18 = 0.37000V | 0x38 = 0.53000V | 0x58 = 0.69000V | 0x78 = 0.85000V | 0x98 = 1.01000V | 0xB8 = 1.17000V | 0xD8 = 1.33000V | 0xF8 = 1.49000V |
| 0x19 = 0.37500V | 0x39 = 0.53500V | 0x59 = 0.69500V | 0x79 = 0.85500V | 0x99 = 1.01500V | 0xB9 = 1.17500V | 0xD9 = 1.33500V | 0xF9 = 1.49500V |
| 0x1A = 0.38000V | 0x3A = 0.54000V | 0x5A = 0.70000V | 0x7A = 0.86000V | 0x9A = 1.02000V | 0xBA = 1.18000V | 0xDA = 1.34000V | 0xFA = 1.50000V |
| 0x1B = 0.38500V | 0x3B = 0.54500V | 0x5B = 0.70500V | 0x7B = 0.86500V | 0x9B = 1.02500V | 0xBB = 1.18500V | 0xDB = 1.34500V | 0xFB = 1.50500V |
| 0x1C = 0.39000V | 0x3C = 0.55000V | 0x5C = 0.71000V | 0x7C = 0.87000V | 0x9C = 1.03000V | 0xBC = 1.19000V | 0xDC = 1.35000V | 0xFC = 1.51000V |
| 0x1D = 0.39500V | 0x3D = 0.55500V | 0x5D = 0.71500V | 0x7D = 0.87500V | 0x9D = 1.03500V | 0xBD = 1.19500V | 0xDD = 1.35500V | 0xFD = 1.51500V |
| 0x1E = 0.40000V | 0x3E = 0.56000V | 0x5E = 0.72000V | 0x7E = 0.88000V | 0x9E = 1.04000V | 0xBE = 1.20000V | 0xDE = 1.36000V | 0xFE = 1.52000V |
| 0x1F = 0.40500V | 0x3F = 0.56500V | 0x5F = 0.72500V | 0x7F = 0.88500V | 0x9F = 1.04500V | 0xBF = 1.20500V | 0xDF = 1.36500V | 0xFF = 1.52500V |

## M1_CFG BUCK Master 1 Configuration Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0xD1 |
|---|---|---|---|---|
| 0x2F | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7 | M1_AD | 1 | BUCK Master 1 Output Active Discharge<br>0: Disable<br>1: Enable | |
| 6:4 | M1_ILIM[2:0] | 101 | BUCK Master 1 PMOS Peak/NMOS Valley Current Limit Setting<br>000b: 3.0A/2.0A<br>001b: 3.6A/2.4A<br>010b: 4.2A/2.8A<br>011b: 4.8A/3.2A<br>100b: 5.4A/3.6A<br>101b: 6.0A/4.0A<br>110b: 6.6A/4.4A<br>111b: 7.2A/4.8A | |
| 2:3 | RESERVED | 00 | Write ‘00’ | |
| 1 | M1_FPWM | 0 | BUCK Master 1 Forced PWM<br>0: Turn off Forced PWM<br>(Automatic skip mode operation under light load)<br>1: Turn on Forced PWM mode | |
| 0 | M1_FSREN | 1 | BUCK Master 1 Falling Slew Rate Control<br>0: Disable<br>BUCK Master 1 operates in skip mode during the output voltage ramp-down (only if M1_FPWM = 0). In skip mode, negative current through the low-side FET is not allowed so that the output voltage falling slew rate is a function of the output capacitance and the external load under light load condition. If the load is heavy, the output voltage falling slew rate is limited to the ramp-down slew rate set by B_RD_SR[1:0]. Note that the internal feedback string always imposes a 2μA load on the output.<br>1: Enable<br>BUCK Master 1 operates in Forced PWM mode during the output voltage ramp-down. In Forced PWM mode, BUCK Master 1 can sink current from the output capacitor to ensure that the output voltage decreases at the ramp-down slew rate set by B_RD_SR[1:0]. To ensure a smooth output voltage ramp-down, Forced PMW mode remains engaged for 50μs after the output voltage decreases to its target voltage. | |

## M2_CFG BUCK Master 2 Configuration Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0xD1 |
|---|---|---|---|---|
| 0x30 | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7 | M2_AD | 1 | BUCK Master 2 Output Active Discharge<br>0: Disable<br>1: Enable | |
| 6:4 | M2_ILIM[2:0] | 101 | BUCK Master 2 PMOS Peak/NMOS Valley Current Limit Setting<br>000b: 3.0A/2.0A<br>001b: 3.6A/2.4A<br>010b: 4.2A/2.8A<br>011b: 4.8A/3.2A<br>100b: 5.4A/3.6A<br>101b: 6.0A/4.0A<br>110b: 6.6A/4.4A<br>111b: 7.2A/4.8A | |
| 2:3 | RESERVED | 00 | Write ‘00’ | |
| 1 | M2_FPWM | 0 | BUCK Master 2 Forced PWM<br>0: Turn off Forced PWM<br>(Automatic skip mode operation under light load)<br>1: Turn on Forced PWM mode | |
| 0 | M2_FSREN | 1 | BUCK Master 2 Falling Slew Rate Control<br>0: Disable<br>BUCK Master 2 operates in skip mode during the output voltage ramp-down (only if M2_FPWM = 0). In skip mode, negative current through the low-side FET is not allowed so that the output voltage falling slew rate is a function of the output capacitance and the external load under light load condition. If the load is heavy, the output voltage falling slew rate is limited to the ramp-down slew rate set by B_RD_SR[1:0]. Note that the internal feedback string always imposes a 2μA load on the output.<br>1: Enable<br>BUCK Master 2 operates in Forced PWM mode during the output voltage ramp-down. In Forced PWM mode, BUCK Master 2 can sink current from the output capacitor to ensure that the output voltage decreases at the ramp-down slew rate set by B_RD_SR[1:0]. To ensure a smooth output voltage ramp-down, Forced PMW mode remains engaged for 50μs after the output voltage decreases to its target voltage. | |

## M3_CFG BUCK Master 3 Configuration Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0xD1 |
|---|---|---|---|---|
| 0x31 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7 | M3_AD | 1 | BUCK Master 3 Output Active Discharge<br>0: Disable<br>1: Enable | |
| 6:4 | M3_ILIM[2:0] | 101 | BUCK Master 3 PMOS Peak/NMOS Valley Current Limit Setting<br>000b: 3.0A/2.0A<br>001b: 3.6A/2.4A<br>010b: 4.2A/2.8A<br>011b: 4.8A/3.2A<br>100b: 5.4A/3.6A<br>101b: 6.0A/4.0A<br>110b: 6.6A/4.4A<br>111b: 7.2A/4.8A | |
| 2:3 | RESERVED | 00 | Write '00' | |
| 1 | M3_FPWM | 0 | BUCK Master 3 Forced PWM<br>0: Turn off Forced PWM<br>(Automatic skip mode operation under light load)<br>1: Turn on Forced PWM mode | |
| 0 | M3_FSREN | 1 | BUCK Master 3 Falling Slew Rate Control<br>0: Disable<br>BUCK Master 3 operates in skip mode during the output voltage ramp-down (only if M3_FPWM = 0). In skip mode, negative current through the low-side FET is not allowed so that the output voltage falling slew rate is a function of the output capacitance and the external load under light load condition. If the load is heavy, the output voltage falling slew rate will be limited to the ramp-down slew rate set by B_RD_SR[1:0]. Note that the internal feedback string always imposes a 2μA load on the output.<br>1: Enable<br>BUCK Master 3 operates in Forced PWM mode during the output voltage ramp-down. In Forced PWM mode, BUCK Master 3 can sink current from the output capacitor to ensure that the output voltage decreases at the ramp-down slew rate set by B_RD_SR[1:0]. To ensure a smooth output voltage ramp-down, Forced PMW mode remains engaged for 50μs after the output voltage decreases to its target voltage. | |

## M4_CFG BUCK Master 4 Configuration Register

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0xD1 |
|---|---|---|---|---|
| 0x32 | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7 | M4_AD | 1 | BUCK Master 4 Output Active Discharge<br>0: Disable<br>1: Enable | |
| 6:4 | M4_ILIM[2:0] | 101 | BUCK Master 4 PMOS Peak/NMOS Valley Current Limit Setting<br>000b: 3.0A/2.0A<br>001b: 3.6A/2.4A<br>010b: 4.2A/2.8A<br>011b: 4.8A/3.2A<br>100b: 5.4A/3.6A<br>101b: 6.0A/4.0A<br>110b: 6.6A/4.4A<br>111b: 7.2A/4.8A | |
| 2:3 | RESERVED | 00 | Write ‘00’ | |
| 1 | M4_FPWM | 0 | BUCK Master4 Forced PWM<br>0: Turn off Forced PWM<br>(Automatic skip mode operation under light load)<br>1: Turn on Forced PWM mode | |
| 0 | M4_FSREN | 1 | BUCK Master 4 Falling Slew Rate Control<br>0: Disable<br>BUCK Master 4 operates in skip mode during the output voltage ramp-down (only if M4_FPWM = 0). In skip mode, negative current through the low-side FET is not allowed so that the output voltage falling slew rate is a function of the output capacitance and the external load under light load condition. If the load is heavy, the output voltage falling slew rate is limited to the ramp-down slew rate set by B_RD_SR[1:0]. Note that the internal feedback string always imposes a 2μA load on the output.<br>1: Enable<br>BUCK Master 4 operates in Forced PWM mode during the output voltage ramp-down. In Forced PWM mode, BUCK Master 4 can sink current from the output capacitor to ensure that the output voltage decreases at the ramp-down slew rate set by B_RD_SR[1:0]. To ensure a smooth output voltage ramp-down, Forced PMW mode remains engaged for 50μs after the output voltage decreases to its target voltage. | |

## GLB_CFG1 BUCK Global Configuration Register 1

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x24 |
|---|---|---|---|---|
| 0x33 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7 | RESERVED | 0 | | |
| 6:4 | B_SD_SR[2:0] | 010 | Shutdown Slew Rate<br>000b: 1.25mV/μs<br>001b: 2.5mV/μs<br>010b: 5mV/μs<br>011b: 10mV/μs<br>100b: 20mV/μs<br>101b: 40mV/μs<br>110b: 60mV/μs<br>111b: 60mV/μs | |
| 3 | RESERVED | 0 | | |
| 0:2 | B_SS_SR[2:0] | 100 | Soft Start Slew Rate<br>000b: 1.25mV/μs<br>001b: 2.5mV/μs<br>010b: 5mV/μs<br>011b: 10mV/μs<br>100b: 20mV/μs<br>101b: 40mV/μs<br>110b: 60mV/μs<br>111b: 60mV/μs | |

## GLB_CFG2 BUCK Global Configuration Register 2

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x24 |
|---|---|---|---|---|
| 0x34 | R/W | | | |
| **BIT** | **NAME** | **POR** | **DESCRIPTION** | |
| 7 | RESERVED | 0 | | |
| 6:4 | B_RD_SR[2:0] | 010 | Ramp-Down Slew Rate<br>000b: 1.25mV/µs<br>001b: 2.5mV/µs<br>010b: 5mV/µs<br>011b: 10mV/µs<br>100b: 20mV/µs<br>101b: 40mV/µs<br>110b: 60mV/µs<br>111b: 60mV/µs | |
| 3 | RESERVED | 0 | | |
| 0:2 | B_RU_SR[2:0] | 100 | Ramp-Up Slew Rate<br>000b: 1.25mV/µs<br>001b: 2.5mV/µs<br>010b: 5mV/µs<br>011b: 10mV/µs<br>100b: 20mV/µs<br>101b: 40mV/µs<br>110b: 60mV/µs<br>111b: 60mV/µs | |

## GLB_CFG3 BUCK Global Configuration Register 3

| ADDRESS | MODE | | TYPE: O | RESET VALUE: 0x5F |
|---|---|---|---|---|
| 0x35 | R/W | | | |
| BIT | NAME | POR | DESCRIPTION | |
| 7 | RESERVED | 0 | | |
| 6 | RESERVED | 1 | | |
| 5 | RESERVED | 0 | | |
| 4 | RESERVED | 1 | | |
| 3 | RESERVED | 1 | | |
| 2 | RESERVED | 1 | | |
| 1 | B_PETR_EN | 1 | Positive Enhanced Transient Response Control<br>0: Disable<br>1: Enable | |
| 0 | B_NETR_EN | 1 | Negative Enhanced Transient Response Control<br>0: Disable<br>1: Enable | |

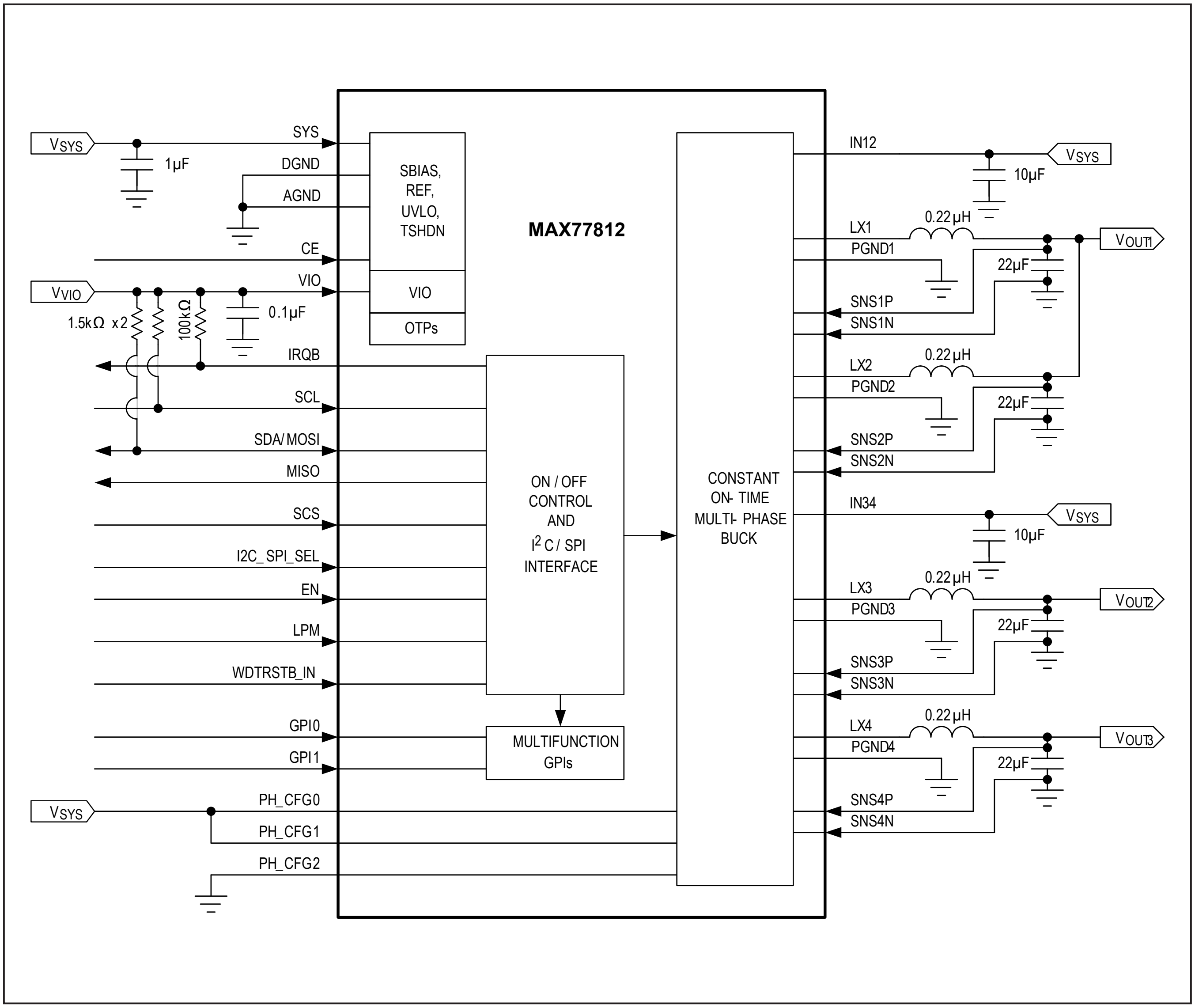
*0x36 – 0xFF: RESERVED*

## PCB Layout Guidelines

Careful circuit board layout is critical to low-power switching losses and clean stable operation.

For more details on PCB layout recommendations for the MAX77812, refer to **Application Note 6819: MAX77812 PCB Layout Guide**.

## Simplified Block Diagram



## Ordering Information

| PART | DEFAULT OUTPUT VOLTAGE (V) | | | | STARTUP DELAY TIME (ms) | | | I2C SLAVE ADDRESS |
|---|---|---|---|---|---|---|---|---|
| | M1_VOUT | M2_VOUT | M3_VOUT | M4_VOUT | M2_STUP_DLY | M3_STUP_DLY | M4_STUP_DLY | |
| MAX77812EWB+T | 0.650 | 0.650 | 0.600 | 0.600 | 0 | 0 | 0 | 0x60–0x69 |
| MAX77812AEWB+T | 0.700 | 0.700 | 0.800 | 1.100 | 0 | 0 | 2 | 0x60–0x69 |
| MAX77812BEWB+T | 1.120 | 1.120 | 0.920 | 0.950 | 0 | 0 | 0 | 0x60–0x69 |
| MAX77812CEWB+T | 0.720 | 1.495 | 0.820 | 0.820 | 5 | 1 | 3 | 0x60–0x69 |
| MAX77812DEWB+T | 0.720 | 1.200 | 0.900 | 0.750 | 3 | 6 | 9 | 0x60–0x69 |
| MAX77812FEWB+T | 0.620 | 1.100 | 0.900 | 1.495 | 0 | 0 | 0 | 0x70–0x79 |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*
*T = Tape and reel.*

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 64 WLP | W643C3+1 | **21-100087** | Refer to **Application Note 1891: Wafer-Level Packaging (WLP) and Its Applications** |

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 6/16 | Initial release | — |
| 1 | 3/17 | Updated *Applications* section, updated *Benefits and Features* section, updated MIN/TYP/MAX values in the *Electrical Characteristics* section and changed inductor to 220nH, DCR = 16mΩ, added Cyntec information to *Table 2,* added $I^2C$ slave addresses for OTP = 1 to *Table 5*, updated Figures 6–9 and communication protocols description, updated GPI_FUNC, M1_CFG, M2_CFG, M3_CFG, M4_CFG, GLB_CFG1, GLB_CFG2 registers in the *Register Map* table, updated *Typical Application Circuit* | 1–14, 29, 32–36, 42, 43, 49, 56, 60–66 |
| 2 | 6/17 | Updated *Benefits and Features* section and *Register Map* table, fixed various typos | 1, 2, 4–6, 8, 11, 12, 14, 15, 23, 25, 26, 31, 33-38, 42, 43, 46-48, 62–64 |
| 3 | 8/17 | Updated title, *Benefits and Features* section, and *Electrical Characteristics* table, corrected label error to Output Voltage Error (%) in *Typical Operating Characteristics*, corrected errors to register name and removed error statement in HS mode in *Detailed Description* section, removed inductor from *Table 2*, corrected error in POR bits in the *GPI_PD_CTRL GPI Pulldown Resistor Control Register* table | 1, 10, 14, 16, 26, 29, 30, 38, 51 |
| 4 | 1/18 | Updated *Applications* and *Benefits and Features* sections, added *Simplified Block Diagram*, added LX1/2/3/4 pulsed ratings, updated *Electrical Characteristics* tables, updated *Detailed Description* section, added ALPS 220nH, removed process information | 1–4, 11, 15, 26–29, 30, 31, 38, 67 |
| 5 | 5/18 | Updated *General Description*, *Benefits and Features*, and *Applications* sections, renamed *Typical Application Circuit* and moved to page 1, updated *Absolute Maximum Ratings* for LXx RMS current, updated *Electrical Characteristics* tables, updated *Typical Operating Characteristics* global conditions and TOCs, updated *Detailed Description* sections, Table 1, Figure 2, Table 5, corrected errors in Registers information, renamed *Simplified Block Diagram* and updated to 2+1+1 configuration, updated *Ordering Information* table | 1–3, 14, 16, 17, 26, 28–30, 32, 34, 35, 47–50, 59–62, 66, 67 |
| 6 | 7/18 | Corrected typo in *Electrical Characteristics* table and other sections, updated *Ordering Information* table | 1, 13, 22, 24–43, 53, 63, 65 |
| 7 | 6/19 | Updated Table 5 and *Ordering Information* table | 32, 65 |
| 8 | 8/19 | Updated *Typical Operating Characteristics* global conditions and TOCs, corrected label error to Output Voltage Error (%) in *Typical Operating Characteristics*, updated *Output Voltage Setting* section, added *Enhanced Transient Response* section, and added *PCB Layout Guidelines* section | 14-15, 28-29, 63 |
| 9 | 9/19 | Updated *Typical Operating Characteristics* section | 14–22 |

## Revision History (continued)

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 10 | 4/20 | Updated *Startup and Shutdown Sequence* section, *Phase/Output Configurations* section, *Multifunction GPIs General Description* section, *Register Map* table, M1_VOUT_D, M2_VOUT_D, M3_VOUT_D, M4_VOUT_D, M1_VOUT_S, M2_VOUT_S, M3_VOUT_S, and M4_VOUT_S register descriptions, and *GLB_CFG3 BUCK Global Configuration Register 3* table; added *Inductor Current Limit* section and *Unused Outputs* section | 27–28, 31–32, 45, 56–57, 65 |
| 11 | 12/20 | Updated *Absolute Maximum Ratings* section, added *Recommended Operating Conditions* table, and updated global conditions in *Electrical Characteristics* tables | 1–13 |
| 12 | 10/22 | Updated *Undervoltage Lockout* and *Output Voltage Setting* sections, added *Power-OK (POK)* section | 26, 29, 31 |