

# SLG59H1313C

A 23 mΩ, 4.5 A nFET Integrated Power Switch with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

## General Description

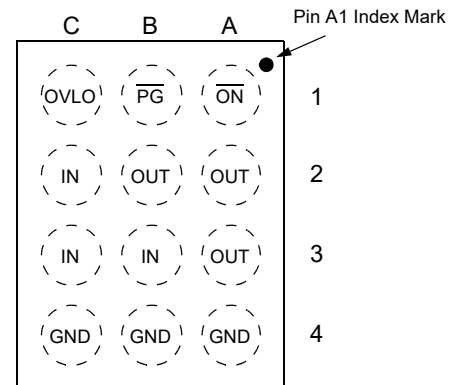
The SLG59H1313C features a low 23 mΩ RDS<sub>ON</sub> internal nFET that protects low-voltage 2.5 Vdc to 5.5 Vdc operating systems against voltage faults up to 29 Vdc. An internal clamp circuit protects the downstream components from surge voltage up to 100 V. The SLG59H1313C features a fast 50 ns (typ) over-voltage response time that turns off the internal nFET if the input voltage exceeds the OVP threshold. The OVP threshold is adjustable with optional external resistors to any voltage between 4 V and 20 V. Over-temperature protection powers down the device at 145 °C (typ). SLG59H1313C also features an Over-current protection that turns off the switch if the current exceeds 7 A (typ), this gives additional protection from over-heating the device.

SLG59H1313C incorporates an open-drain output  $\overline{\text{PG}}$  pin. When  $V_{\text{IN\_min}} < V_{\text{IN}} < V_{\text{OVLO}}$  and the switch is on,  $\overline{\text{PG}}$  will be driven low indicating a good power input, otherwise it is high impedance.

## Features

- Pin-to-pin to PFP2280 with Improved Performance
- Surge protection (IEC61000-4-5: >100 V)
- Input maximum voltage rating: 29 Vdc
- Integrated low RDS<sub>ON</sub> nFET switch: 23 mΩ (typ)
- 4.5 A continuous current capability
- Over-Voltage Protection (OVP): adjustable 4 V to 20 V
- Over-Temperature Protection (OTP): 145 °C (typ)
- 7 A Over-Current Protection (OCP)
- Under-Voltage Lockout (UVLO)
- Fast OVP turn-off response: typical 50 ns
- 1.3 mm x 1.8 mm in 12-ball WLCSP
- Pb-Free/Halogen-Free /ROHS Compliant

## Pin Configuration

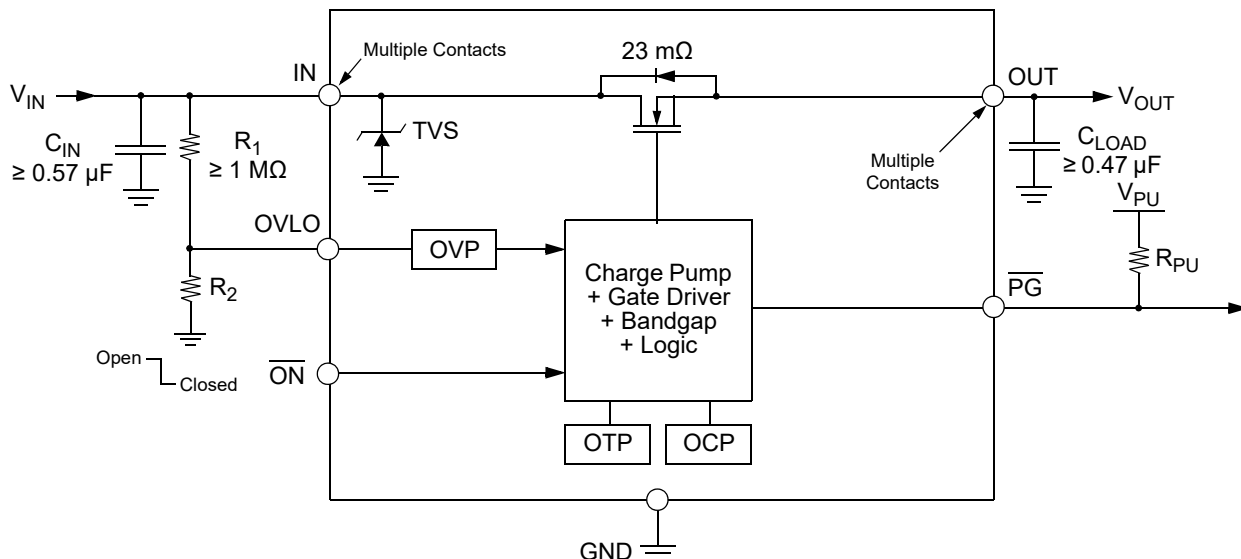


(Laser Marking View)  
1.3 x 1.8 x 0.5 mm, 0.4 mm pitch

## Applications

- Wearable Devices
- Tablet PCs and Smartphones

## Block Diagram



## A 23 mΩ, 4.5 A nFET Integrated Power Switch with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

### Pin Description

Pin Name	Pin #	Type	Pin Description				
IN	B3, C2, C3	Input	IC power supply and power switch input (3 contacts). Bypass the IN pin to GND with a 0.57 μF (or larger) capacitor. Capacitors used at the IN pin should be rated at 30 V or higher.				
OUT	A2, A3, B2	Output	Power switch output to Load (3 contacts). Connect a low-ESR capacitor from the OUT pin to ground and follow the C <sub>LOAD</sub> recommendation in the Electrical Characteristics section. Capacitors used at the OUT pin should be rated at 30 V or higher.				
$\overline{\text{PG}}$	B1	Output	Power Good is an open-drain, active LOW output and becomes asserted when $2.5 \text{ V} < V_{\text{IN}} < V_{\text{OVLO}}$ . For additional details on setting $V_{\text{OVLO}}$ , please consult the “OVLO Calculation” section under Applications Information. <table border="1" style="margin-left: 20px;"> <tr> <td>1</td> <td><math>V_{\text{IN}} &lt; V_{\text{IN\_min}}</math> or <math>V_{\text{IN}} \geq V_{\text{OVLO}}</math></td> </tr> <tr> <td>0</td> <td>Voltage Stable</td> </tr> </table>	1	$V_{\text{IN}} < V_{\text{IN\_min}}$ or $V_{\text{IN}} \geq V_{\text{OVLO}}$	0	Voltage Stable
1	$V_{\text{IN}} < V_{\text{IN\_min}}$ or $V_{\text{IN}} \geq V_{\text{OVLO}}$						
0	Voltage Stable						
$\overline{\text{ON}}$	A1	Input	A high-to-low transition on this pin initiates the operation of the SLG59H1313C’s logic control. $\overline{\text{ON}}$ is an asserted active-LOW, level-sensitive CMOS input with $V_{\text{IL\_ON}} < 0.5 \text{ V}$ and $V_{\text{IH\_ON}} > 1.2 \text{ V}$ . As the $\overline{\text{ON}}$ pin input circuit is directly connected to internal digital circuits, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller – do not allow this pin to be open-circuited.				
OVLO	C1	Input	Overvoltage Lockout Adjustment Pin. To set the SLG59H1313C’s OVLO trip threshold to its internal $V_{\text{IN\_OVLO}}$ , connect OVLO pin to GND. To set the SLG59H1313C’s OVLO trip threshold with an external resistor network, please consult Applications Information section; - minimum recommended value for $R_1$ is 1 MΩ				
GND	A4, B4, C4	GND	Analog GND (3 contacts)				

### Ordering Information

Part Number	Type	Production Flow
SLG59H1313C	WLCSP 12L	Industrial, -40 °C to 85 °C
SLG59H1313CTR	WLCSP 12L (Tape and Reel)	Industrial, -40 °C to 85 °C

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### Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>IN</sub> to GND	Power Switch Input Voltage to Ground	Continuous	-0.3	--	29	V
V <sub>OUT</sub> to GND	Power Switch Output Voltage to GND		-0.3	--	V <sub>IN</sub> + 0.3	V
V <sub>OVLO</sub> to GND	OVLO Voltage to GND		-0.3	--	24	V
$\overline{\text{ON}}$ , $\overline{\text{PG}}$ to GND	$\overline{\text{ON}}$ , $\overline{\text{PG}}$ Pin Voltages to GND		--	--	6	V
I <sub>IN</sub>	Switch I/O Current	Continuous	--	--	4.5	A
t <sub>PD</sub>	Total Power Dissipation at T <sub>A</sub> = 25°C	Continuous	--	--	1.48	W
T <sub>STG</sub>	Storage Temperature Range		-65	--	+150	°C
T <sub>J</sub>	Maximum Junction Temperature		--	--	+150	°C
θ <sub>JA</sub>	Package Thermal Resistance, Junction-to-Ambient	1.3 x 1.8 mm 12L WLCSP; Determined using a 1 in <sup>2</sup> , 1 oz. copper pad under each IN and OUT terminal and FR4 pcb material.	--	--	84.1	°C/W
VIN ESD <sub>SYS</sub>	IEC 61000-4-2 System ESD	Air Gap	15	--	--	kV
		Contact	8	--	--	kV
ESD <sub>HBM</sub>	Human Body Model ESD Protection	All pins	4	--	--	kV
ESD <sub>CDM</sub>	Charged Device Model ESD Protection	All pins	1	--	--	kV
ESD <sub>SURGE</sub>	VIN Surge Protection ESD Protection	IEC 61000-4-5	+100	--	--	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended Operating Conditions

T<sub>A</sub> = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Min.	Typ.	Max.	Unit
<b>Basic Operation</b>					
V <sub>IN</sub>	Power Switch Input Voltage	2.5	--	20	V
T <sub>A</sub>	Operating Temperature	-40	--	85	°C

### Electrical Characteristics

T<sub>A</sub> = -40 °C to 85 °C (unless otherwise stated). Typical values are V<sub>IN</sub> = 5.0 V, I<sub>IN</sub> ≤ 3 A, C<sub>IN</sub> = 0.57 μF, T<sub>A</sub> = 25 °C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
<b>Basic Operation</b>						
V <sub>IN_CLAMP</sub>	Input Clamping Voltage	I <sub>IN</sub> = 10 mA	--	35	--	V
I <sub>Q</sub>	Input Quiescent Current	V <sub>IN</sub> = 5 V; $\overline{\text{ON}}$ = 0 V	--	245	310	μA
I <sub>Q_OFF</sub>	Input Quiescent Current when OFF	V <sub>IN</sub> = 5 V; $\overline{\text{ON}}$ = 1.2 V	--	0.15	1	μA
I <sub>IN_Q</sub>	OVLO Supply Current	V <sub>OVLO</sub> = 3 V; V <sub>IN</sub> = 5 V; V <sub>OUT</sub> = 0 V	--	165	200	μA

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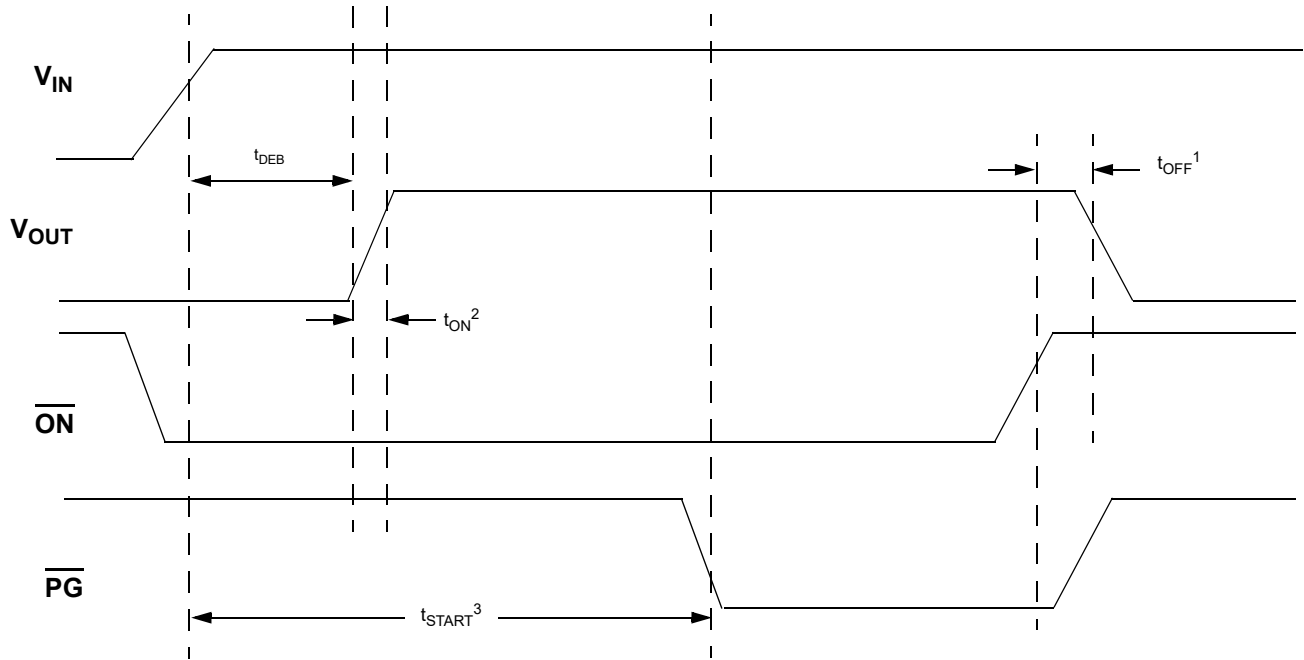
### Electrical Characteristics (continued)

T<sub>A</sub> = -40 °C to 85 °C (unless otherwise stated). Typical values are V<sub>IN</sub> = 5.0 V, I<sub>IN</sub> ≤ 3 A, C<sub>IN</sub> = 0.57 μF, T<sub>A</sub> = 25 °C

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V <sub>IN_OVLO</sub>	Internal Over-Voltage Trip Level	V <sub>IN</sub> Rising, OVLO = GND	6.2	6.5	6.8	V
		V <sub>IN</sub> Falling, OVLO = GND	6.0	--	--	V
V <sub>OVLO_TH</sub>	OVLO Set Threshold	V <sub>IN</sub> = 2.5 V to V <sub>OVLO</sub>	1.10	1.20	1.30	V
V <sub>OVLO_RNG</sub>	Adjustable OVLO Threshold Range	V <sub>IN</sub> = 2.5 V to V <sub>OVLO</sub>	4	--	20	V
V <sub>OVLO_SELECT</sub>	External OVLO Select Threshold		--	0.30	0.28	V
RDS <sub>ON</sub>	ON Resistance	V <sub>IN</sub> = 5 V; I <sub>OUT</sub> = 0.1 A; T <sub>A</sub> = 25 °C	--	23	28	mΩ
		V <sub>IN</sub> = 5 V; I <sub>OUT</sub> = 0.1 A; T <sub>A</sub> = 85 °C	--	29	34	mΩ
C <sub>LOAD</sub>	Output Load Capacitance	V <sub>IN</sub> = 5 V	0.47	--	500	μF
I <sub>OVLO</sub>	OVLO Input Leakage Current	V <sub>OVLO</sub> = V <sub>OVLO_TH</sub>	-100	--	100	nA
THERM <sub>ON</sub>	Thermal Shutdown Turn-on Temperature		--	145	--	°C
THERM <sub>HYS</sub>	Thermal Shutdown Hysteresis		--	20	--	°C
I <sub>OC</sub>	Regular Over Current Protection	V <sub>IN</sub> = 2.5 V to V <sub>OVLO</sub>	--	7	--	A
I <sub>SCP</sub>	Startup Current Protection	V <sub>IN</sub> = 2.5 V to V <sub>OVLO</sub>	--	1	--	A
<b>Digital Signals</b>						
V <sub>OL_PG</sub>	$\overline{\text{PG}}$ Output LOW Voltage	V <sub>I/O</sub> = 3.3 V; I <sub>SINK</sub> = 1 mA	--	--	0.4	V
V <sub>IH_ON</sub>	$\overline{\text{ON}}$ HIGH Voltage	V <sub>IN</sub> = 2.5 V to V <sub>OVLO</sub>	1.2	--	--	V
V <sub>IL_ON</sub>	$\overline{\text{ON}}$ LOW Voltage	V <sub>IN</sub> = 2.5 V to V <sub>OVLO</sub>	--	--	0.5	V
I <sub>LKG_PG</sub>	$\overline{\text{PG}}$ Leakage Current	V <sub>I/O</sub> = 3.3 V; $\overline{\text{PG}}$ Deasserted, $\overline{\text{ON}} = 0$ V	-0.5	--	0.5	μA
I <sub>LKG_ON</sub>	$\overline{\text{ON}}$ Leakage current	V <sub>IN</sub> = 5 V; V <sub>OUT</sub> = Float	-1.0	--	1.0	μA
<b>Timing Characteristics</b>						
t <sub>DEB</sub>	Debounce Time	Time from 2.5 V < V <sub>IN</sub> < V <sub>IN_OVLO</sub> to V <sub>OUT</sub> = 0.1 x V <sub>IN</sub>	--	15	--	ms
t <sub>START</sub>	Soft-Start Time	Time from V <sub>IN</sub> = V <sub>IN_min</sub> to 0.2 x $\overline{\text{PG}}$ ; V <sub>I/O</sub> = 1.8 V with 10 kΩ pull-up resistor	--	30	--	ms
t <sub>ON</sub>	Switch Turn-on Time	V <sub>IN</sub> = 5 V; R <sub>LOAD</sub> = 100 Ω; V <sub>OUT</sub> from 0.1 V <sub>IN</sub> to 0.9 V <sub>IN</sub> ; C <sub>LOAD</sub> = 100 μF	--	4	--	ms
t <sub>OFF</sub>	Switch Turn-off Time	R <sub>LOAD</sub> = 100 Ω; C <sub>LOAD</sub> = 0 μF; V <sub>IN</sub> > V <sub>OVLO</sub> to V <sub>OUT</sub> = V <sub>IN</sub> - 50 mV	--	50	--	ns
Notes:						
1. Based on bench measurement only.						

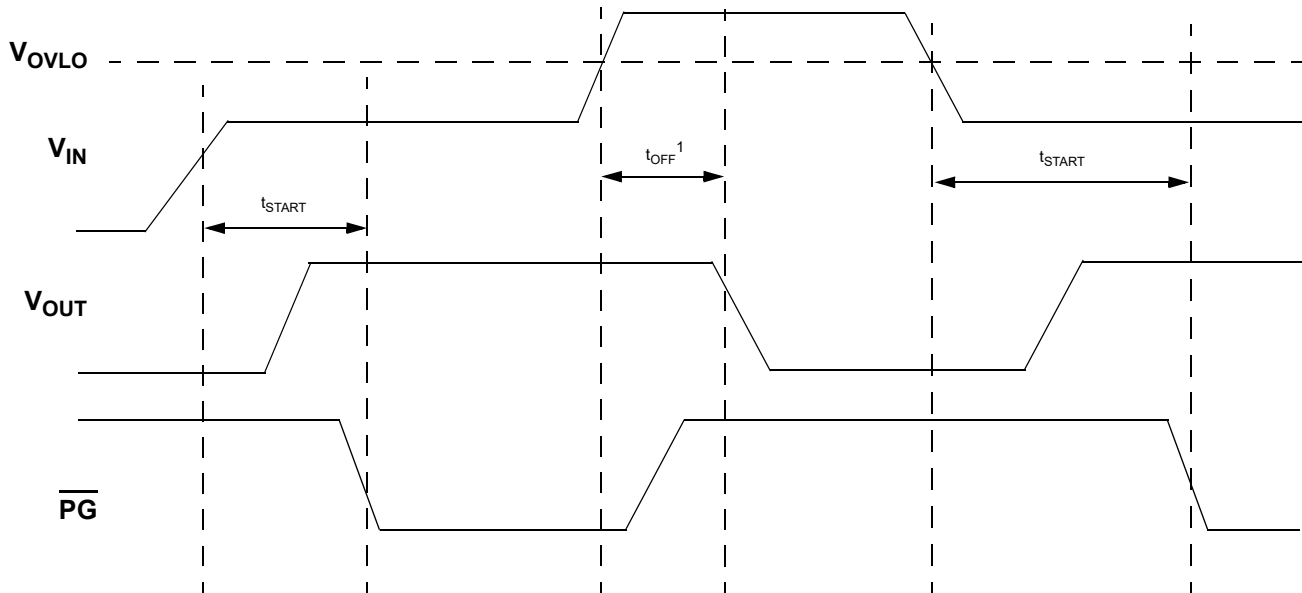
A 23 mΩ, 4.5 A nFET Integrated Power Switch with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

Timing Diagram: Power up and Normal Operation



1. Measured @ 80%  $\overline{ON}$ ,  $V_{OUT} = 80\% V_{IN}$
2. Measured @ 10/90%
3. Measured @  $V_{IN} > 2.5\text{ V}$  to  $0.2 \times \overline{PG}$ ;  $\overline{PG}$ :  $V_{IO} = 1.8\text{ V}$  w/ 10K Pull Up

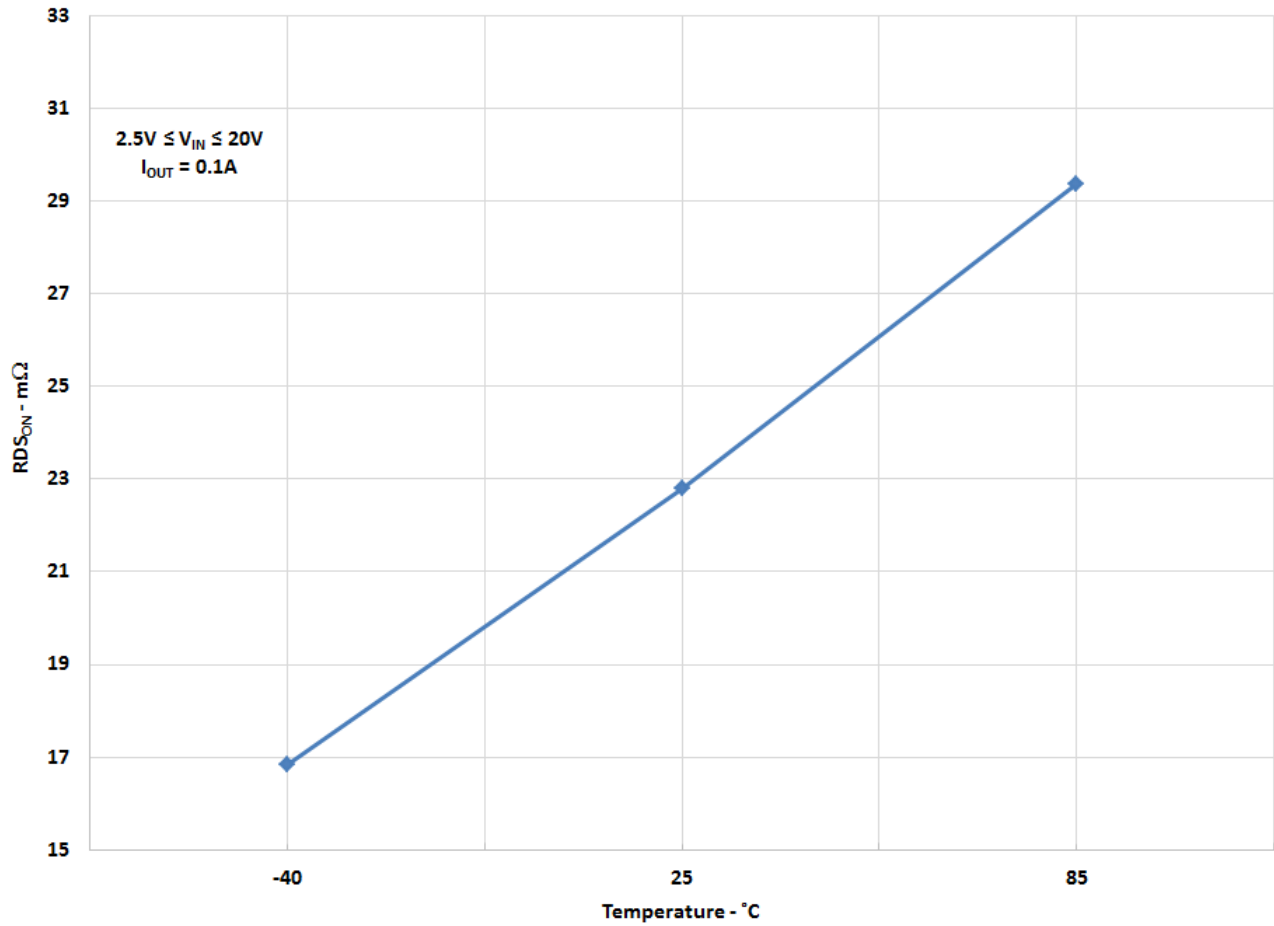
Timing Diagram: OVLO Trigger



1. Measured @ OVLO Rising  $V_{OUT} = V_{IN} - 50\text{ mV}$

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**RDSON vs. Temperature and VIN**



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Typical Turn-on Waveforms

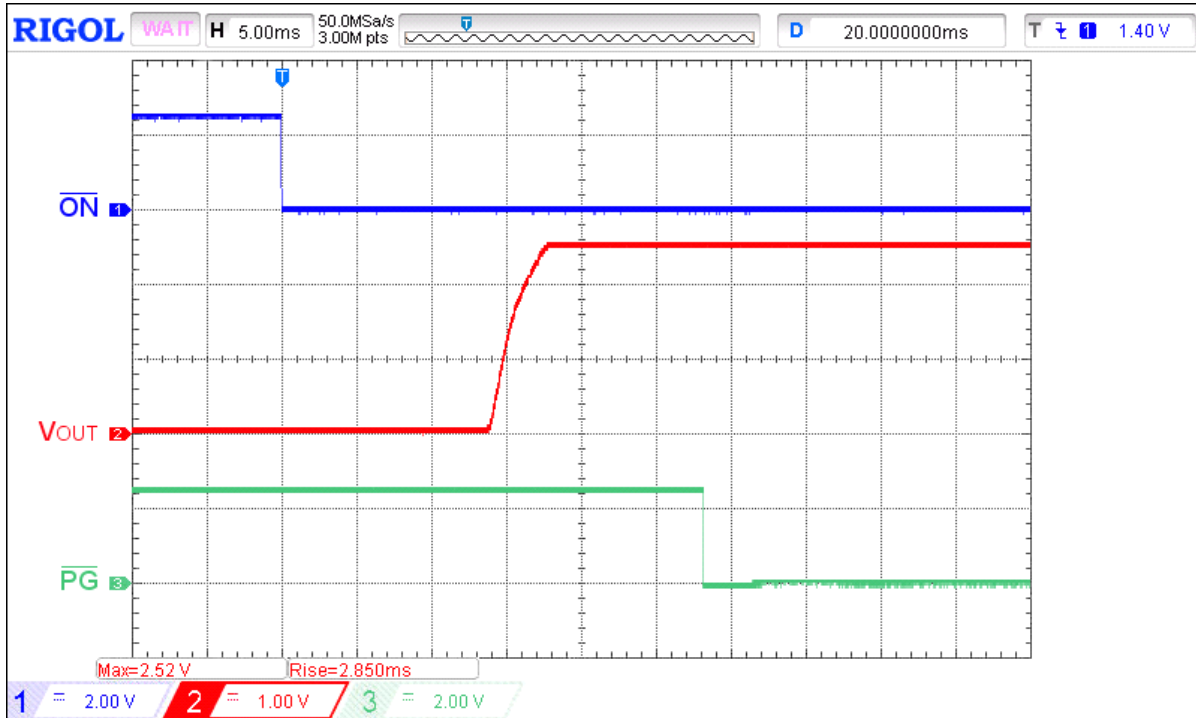


Figure 1. Typical Turn ON operation waveform for  $V_{IN} = 2.5\text{ V}$ ,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $R_{LOAD} = 100\ \Omega$

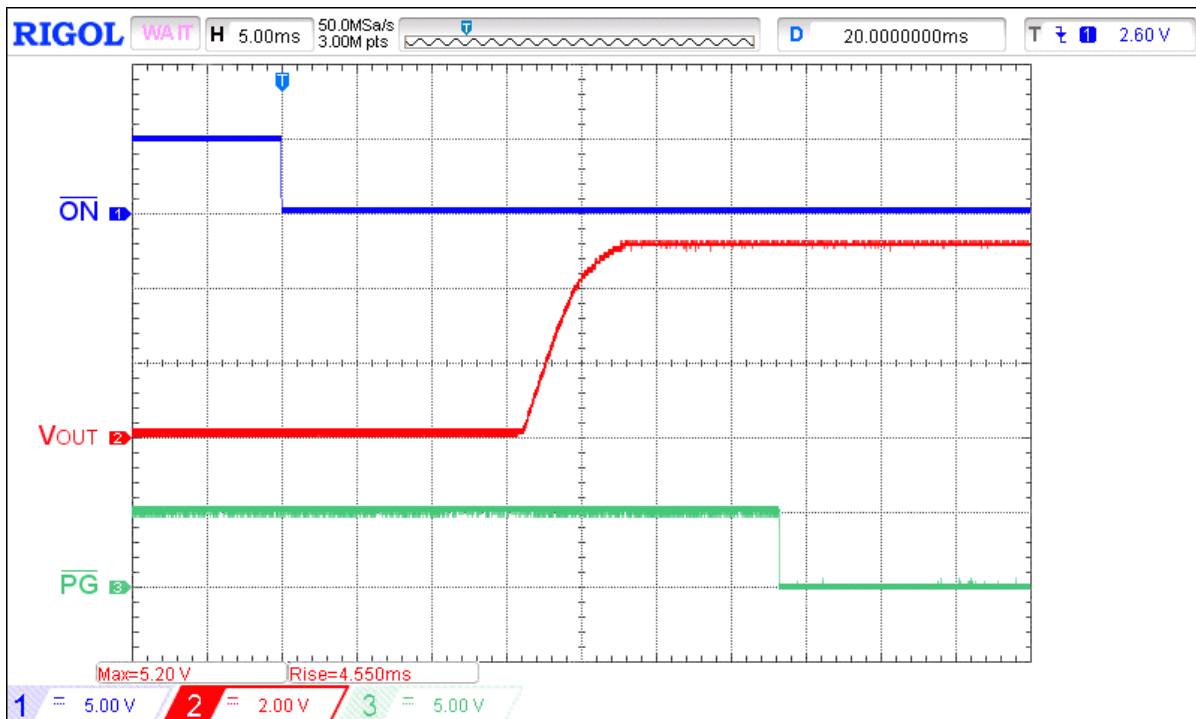


Figure 2. Typical Turn ON operation waveform for  $V_{IN} = 5\text{ V}$ ,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $R_{LOAD} = 100\ \Omega$

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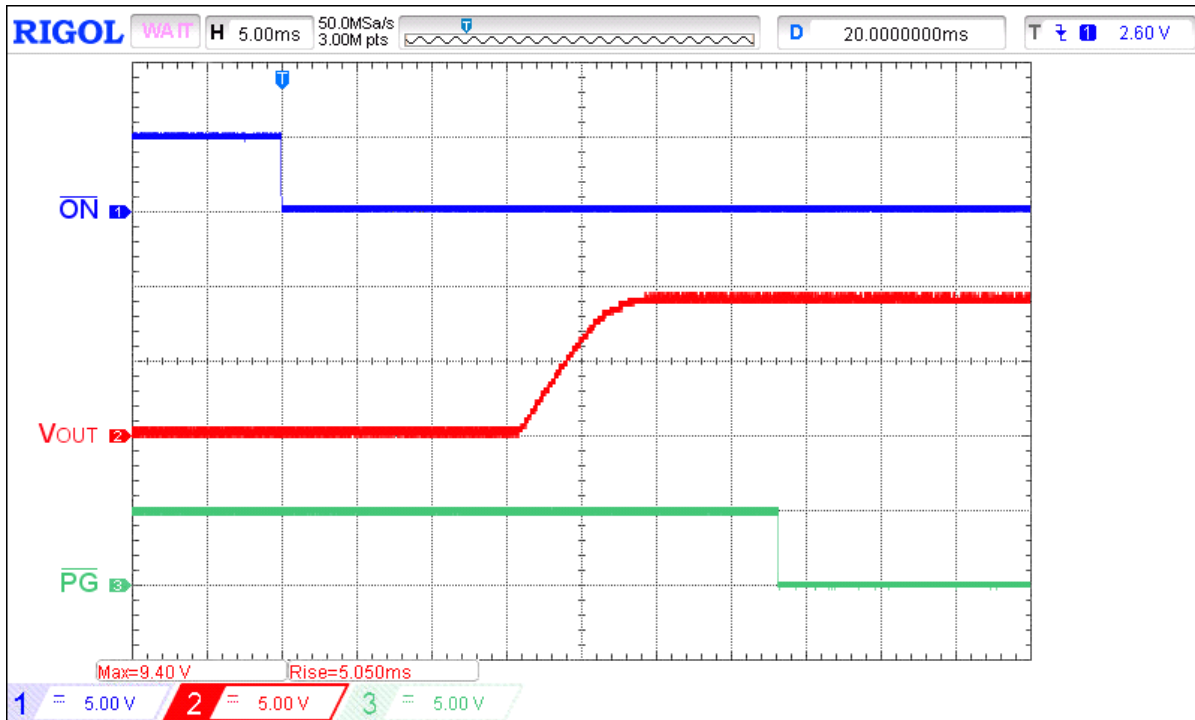


Figure 3. Typical Turn ON operation waveform for  $V_{IN} = 9\text{ V}$ ,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $R_{LOAD} = 100\ \Omega$

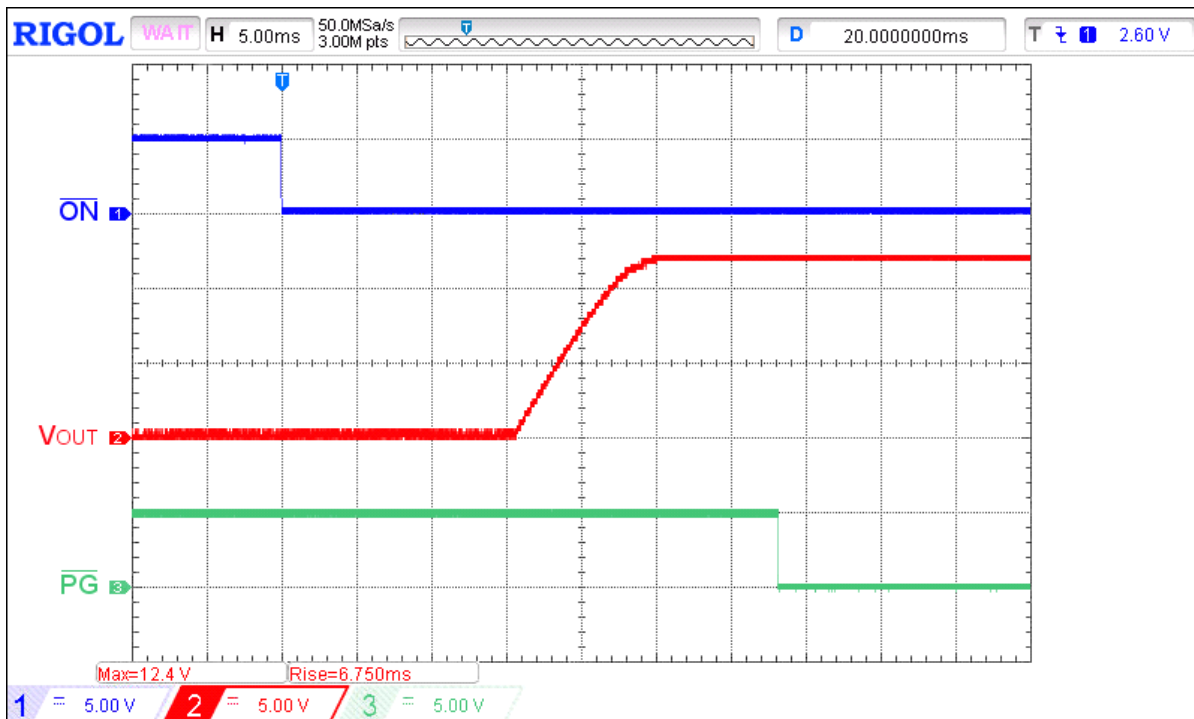


Figure 4. Typical Turn ON operation waveform for  $V_{IN} = 12\text{ V}$ ,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $R_{LOAD} = 100\ \Omega$



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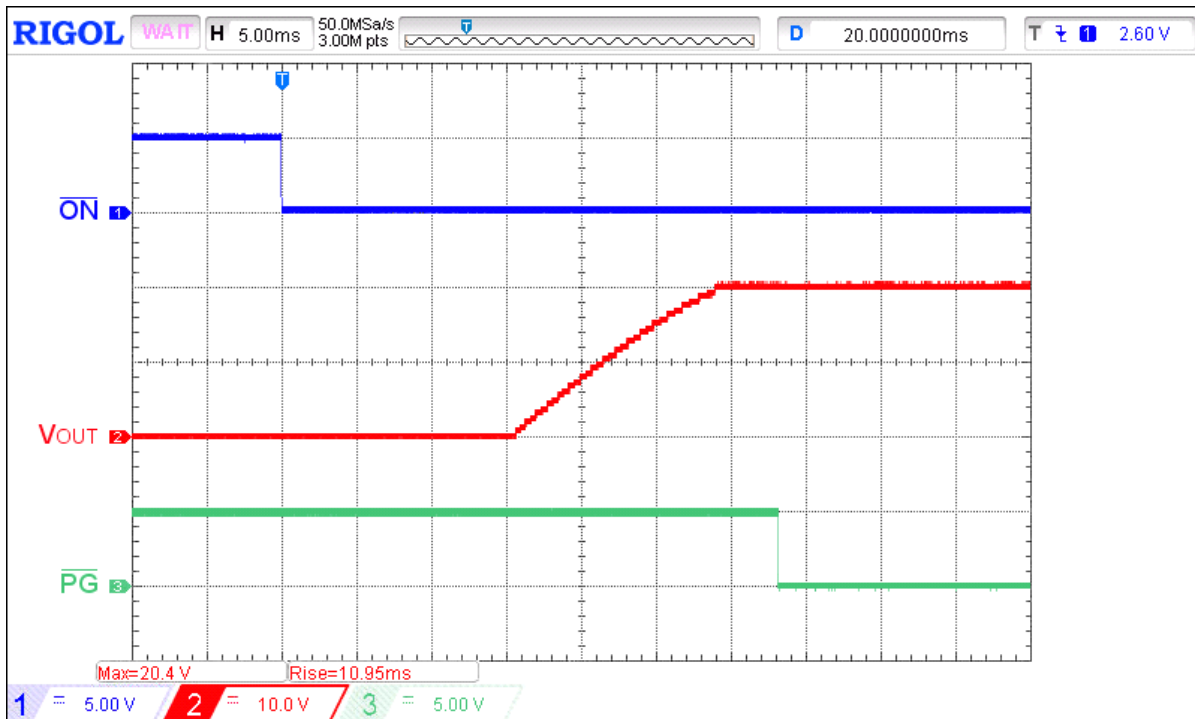


Figure 5. Typical Turn ON operation waveform for  $V_{IN} = 20\text{ V}$ ,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $R_{LOAD} = 100\ \Omega$

Typical Turn-off Waveforms

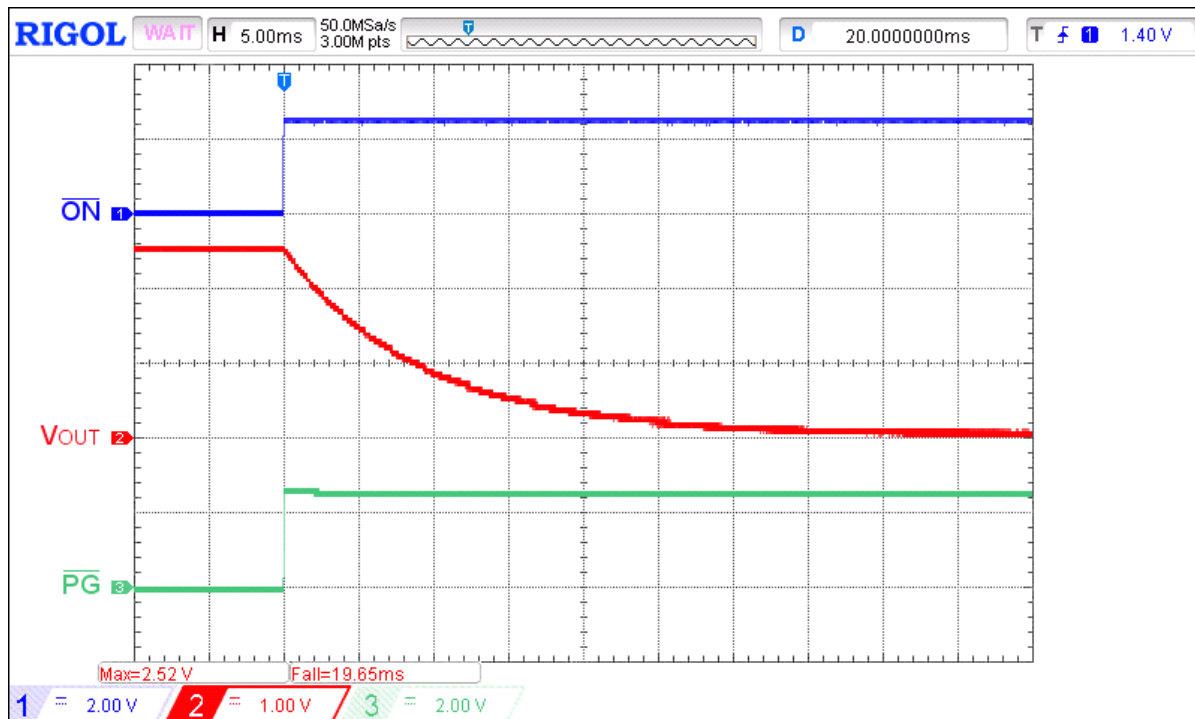


Figure 6. Typical Turn OFF operation waveform for  $V_{IN} = 2.5\text{ V}$ ,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $R_{LOAD} = 100\ \Omega$

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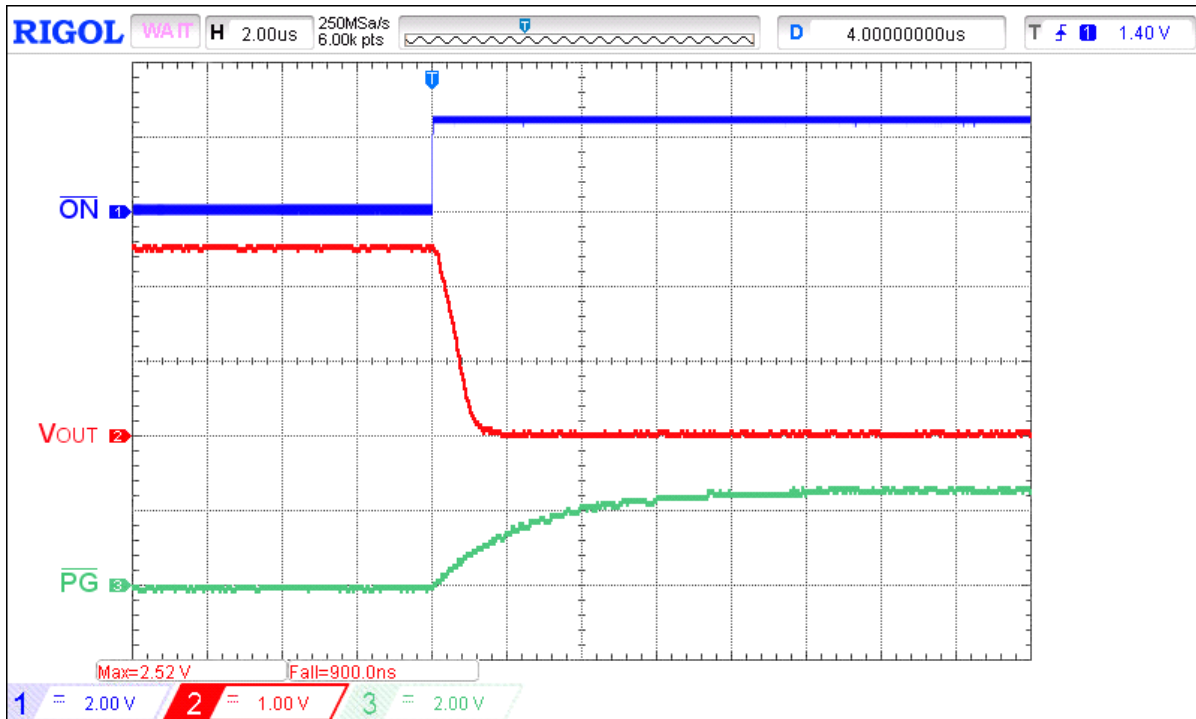


Figure 7. Typical Turn OFF operation waveform for  $V_{IN} = 2.5\text{ V}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 100\ \Omega$

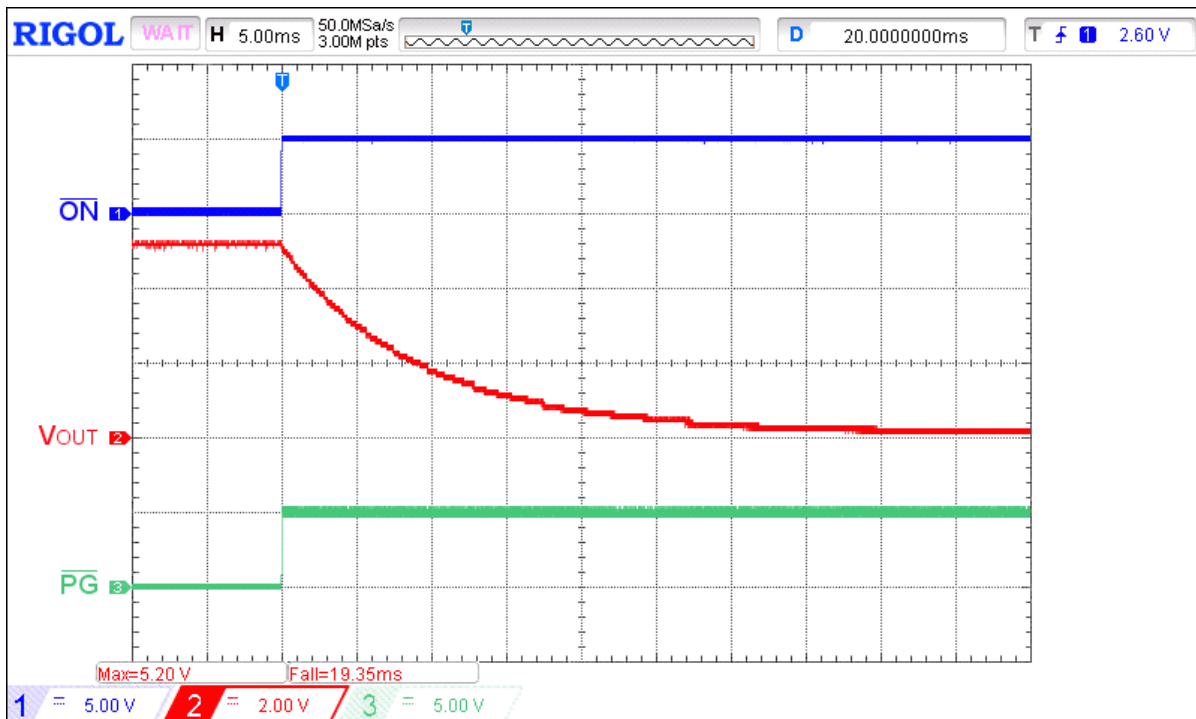


Figure 8. Typical Turn OFF operation waveform for  $V_{IN} = 5\text{ V}$ ,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $R_{LOAD} = 100\ \Omega$

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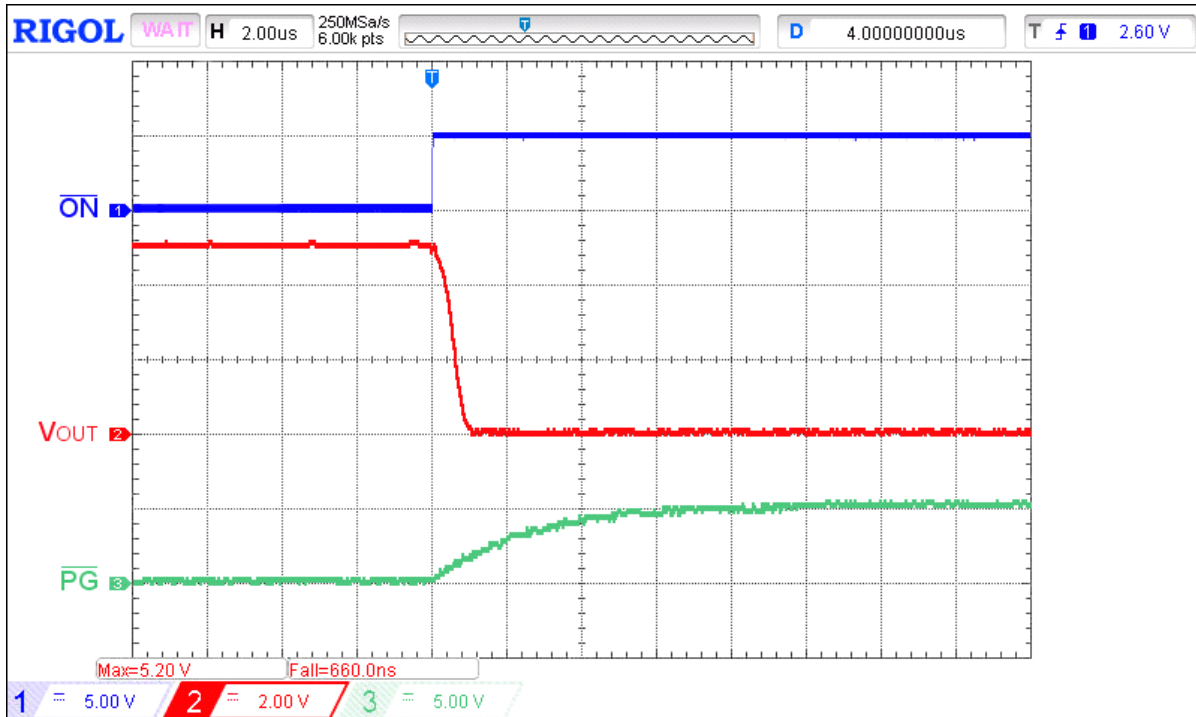


Figure 9. Typical Turn OFF operation waveform for  $V_{IN} = 5\text{ V}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 100\ \Omega$

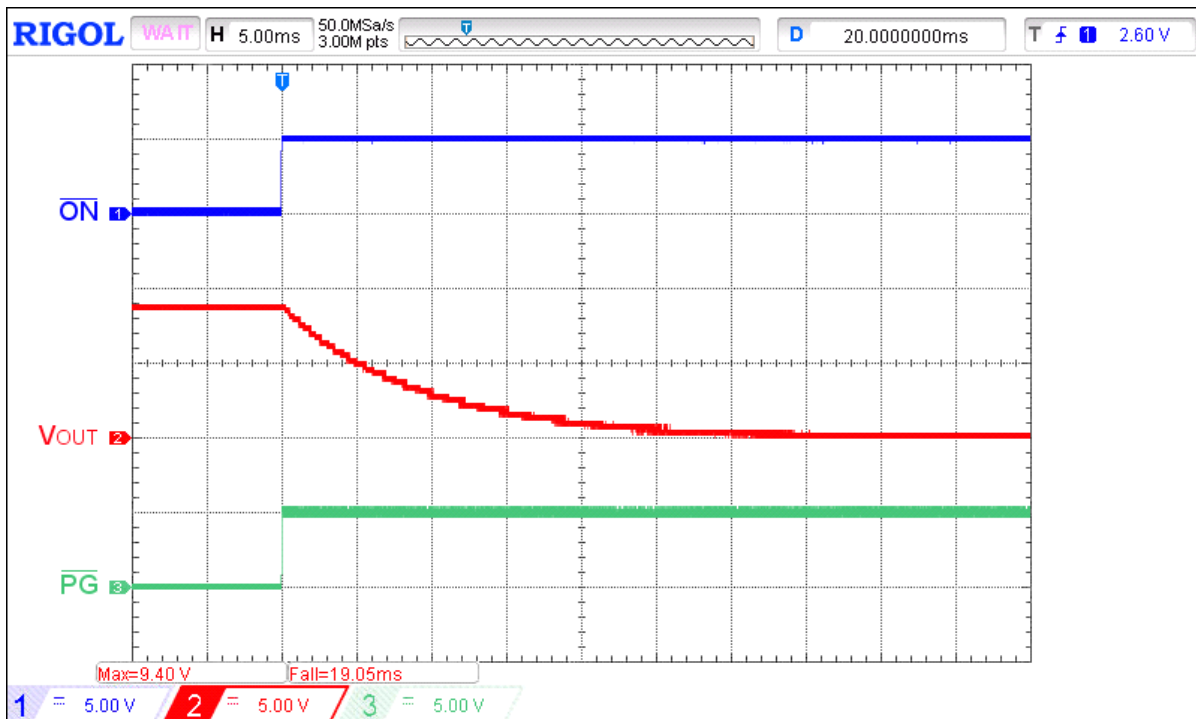


Figure 10. Typical Turn OFF operation waveform for  $V_{IN} = 9\text{ V}$ ,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $R_{LOAD} = 100\ \Omega$

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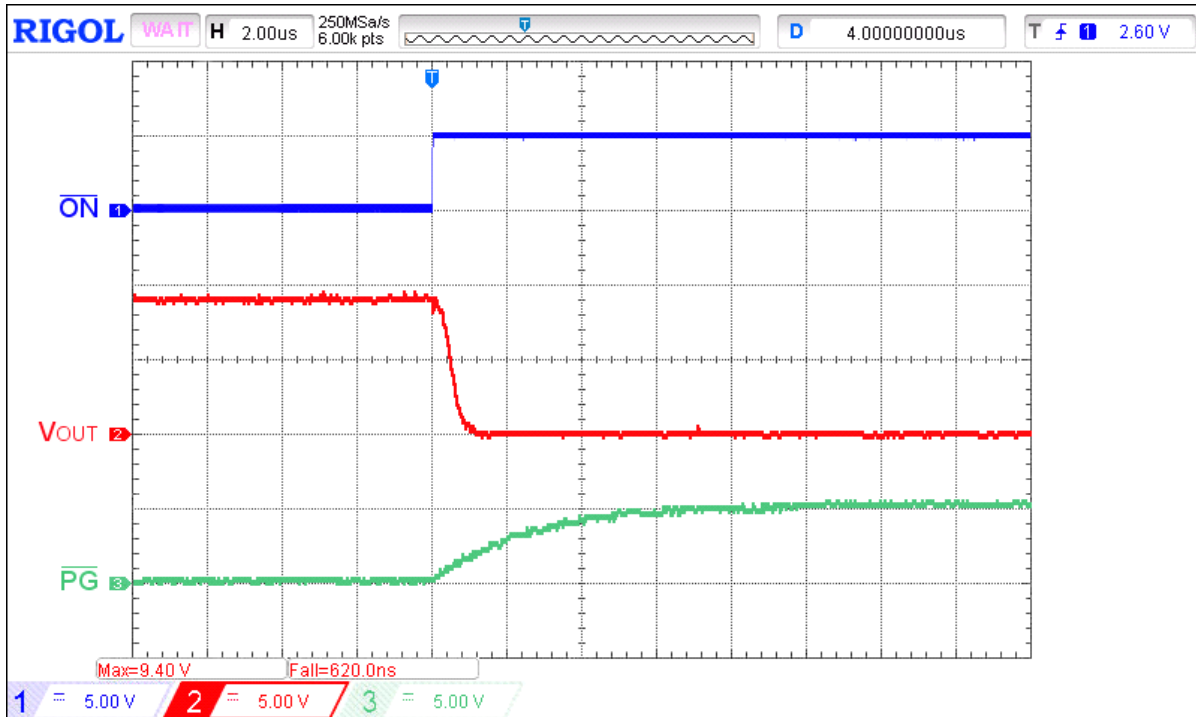


Figure 11. Typical Turn OFF operation waveform for  $V_{IN} = 9\text{ V}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 100\ \Omega$

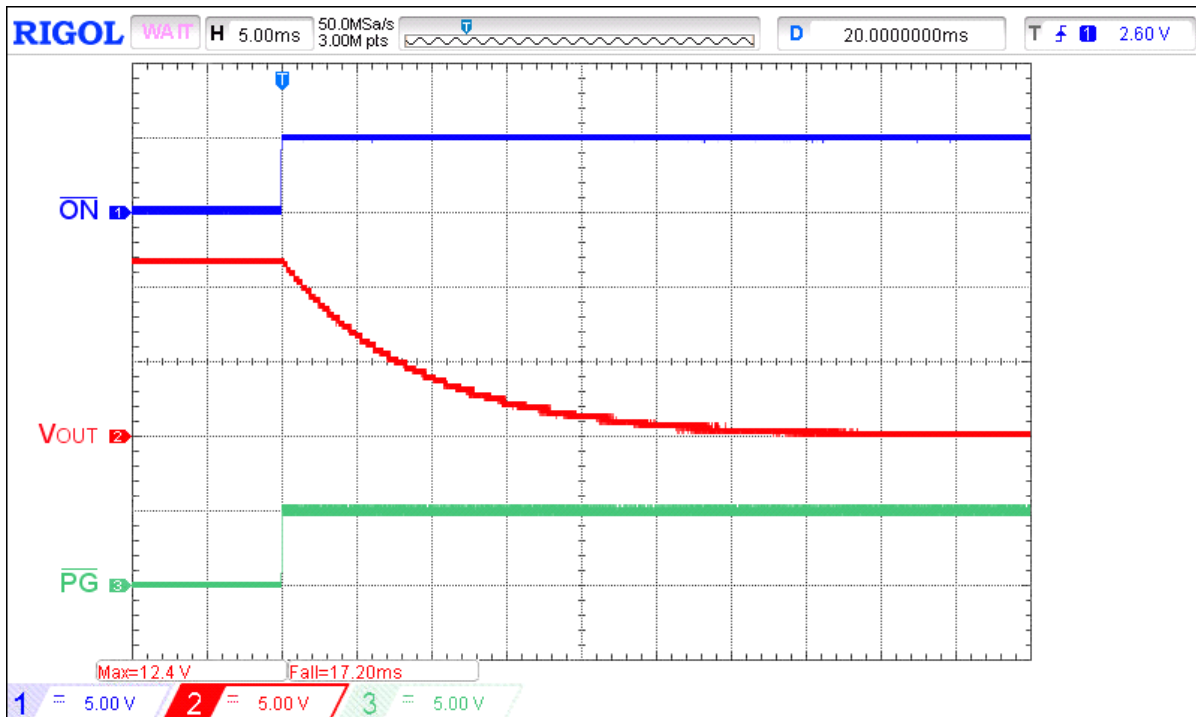


Figure 12. Typical Turn OFF operation waveform for  $V_{IN} = 12\text{ V}$ ,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $R_{LOAD} = 100\ \Omega$

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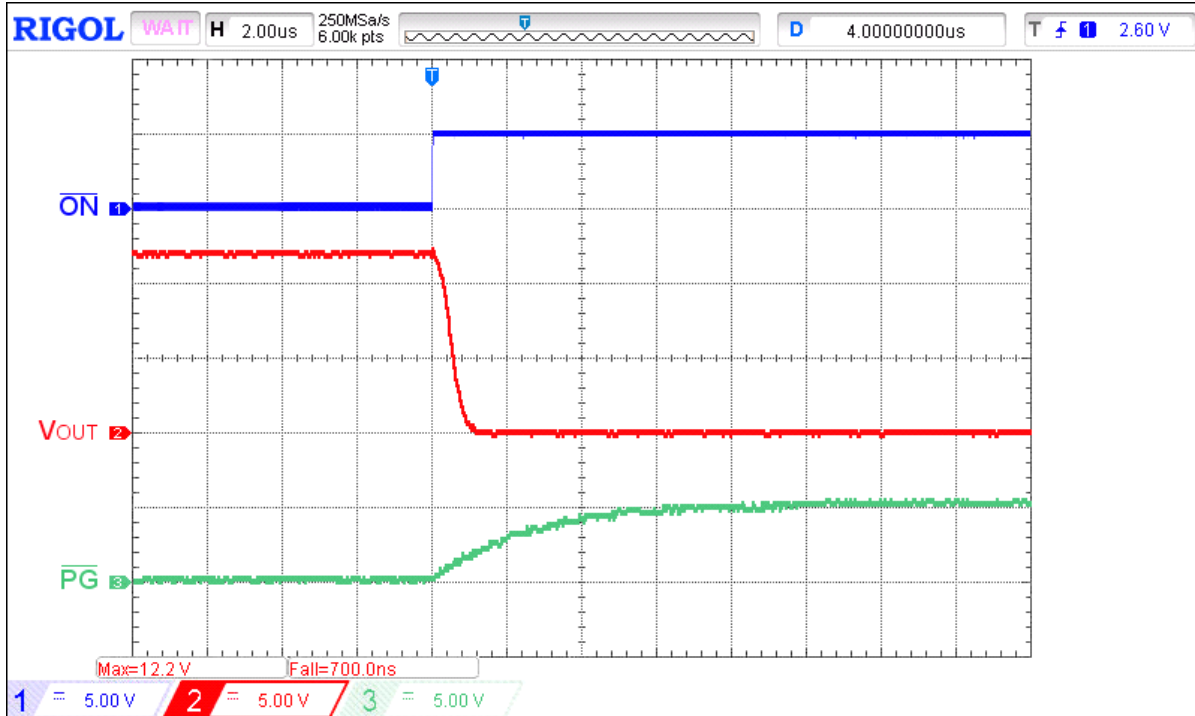


Figure 13. Typical Turn OFF operation waveform for  $V_{IN} = 12\text{ V}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 100\ \Omega$

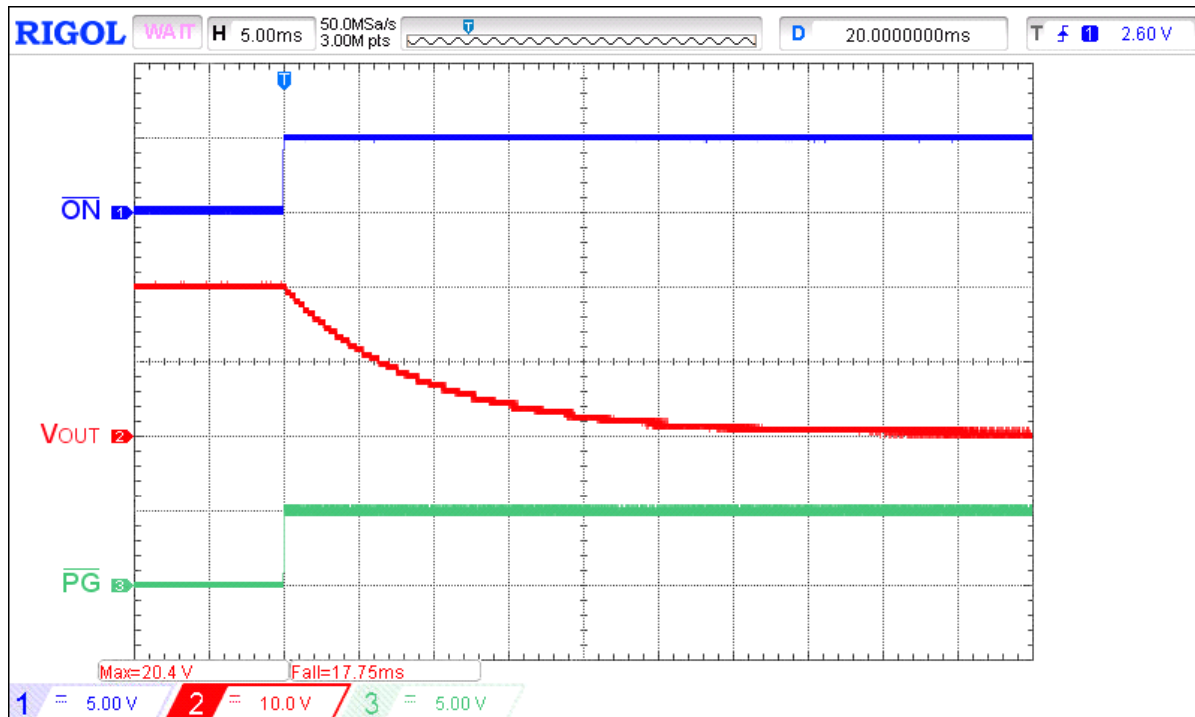


Figure 14. Typical Turn OFF operation waveform for  $V_{IN} = 20\text{ V}$ ,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $R_{LOAD} = 100\ \Omega$

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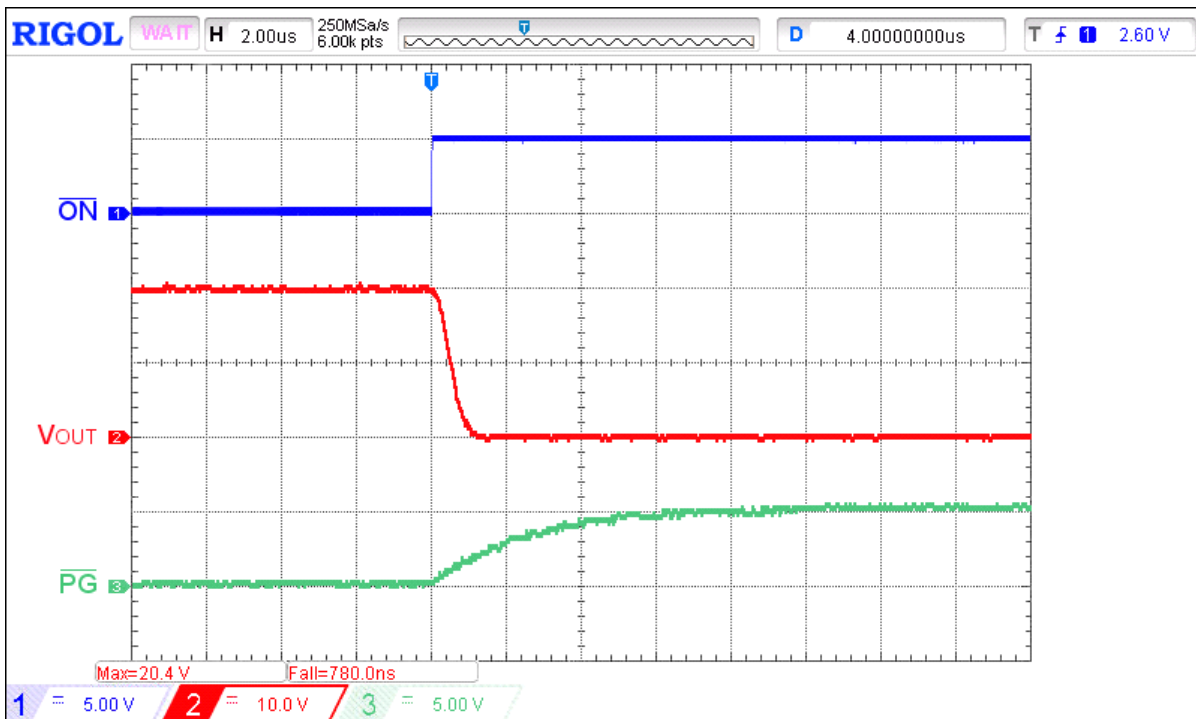


Figure 15. Typical Turn OFF operation waveform for  $V_{IN} = 20\text{ V}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 100\ \Omega$

Overcurrent Protection Waveform

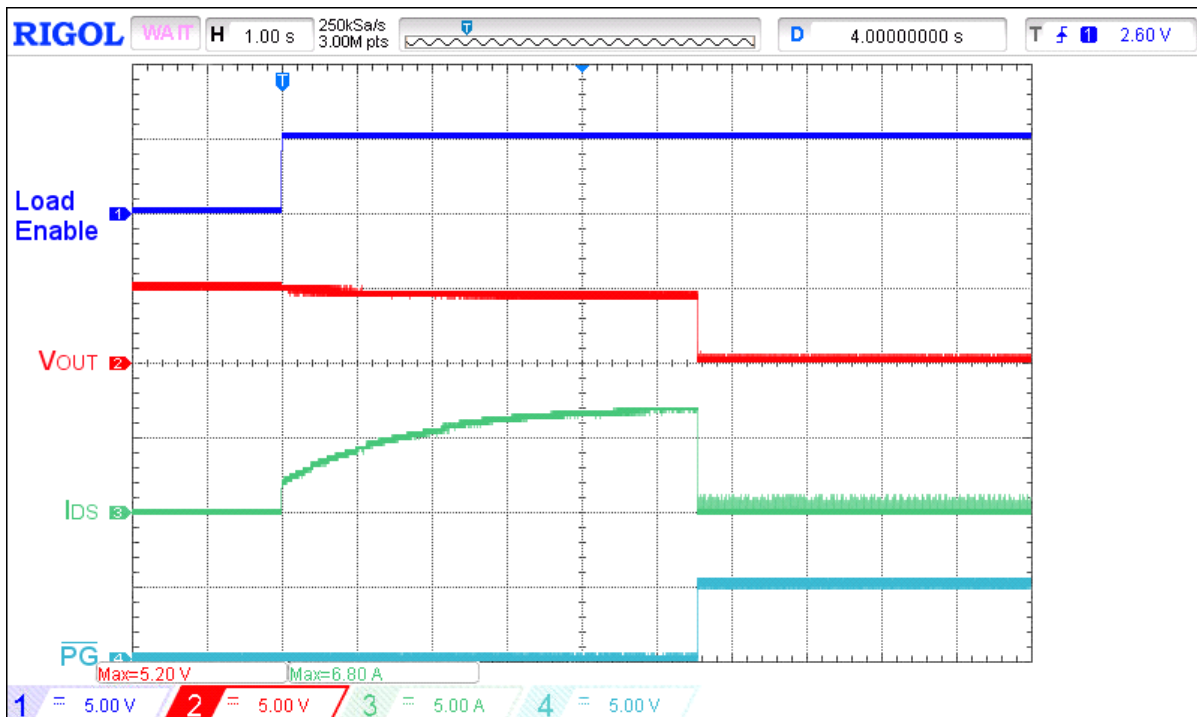


Figure 16. Overcurrent Protection operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 0.7\ \Omega$

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Overvoltage Operation Waveform

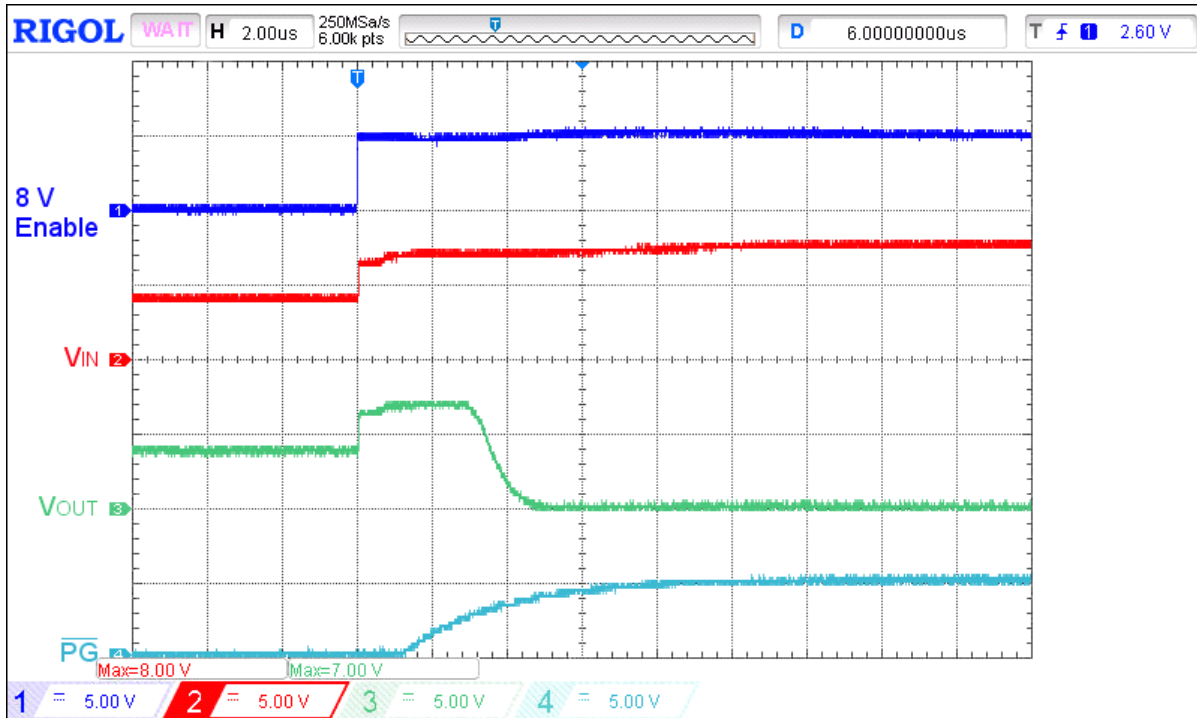


Figure 17. Overvoltage during normal operation for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 100\ \Omega$

Startup Current Protection Waveforms

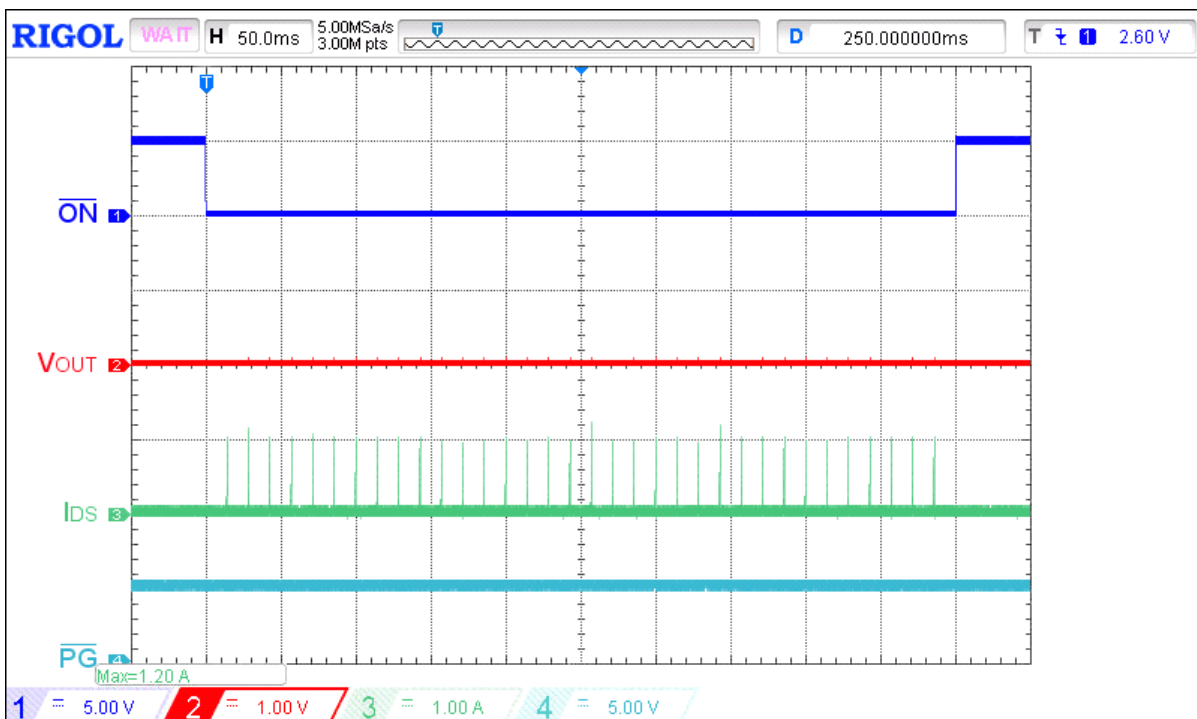


Figure 18. Startup Current Protection operation waveform for  $V_{IN} = 2.5\text{ V}$

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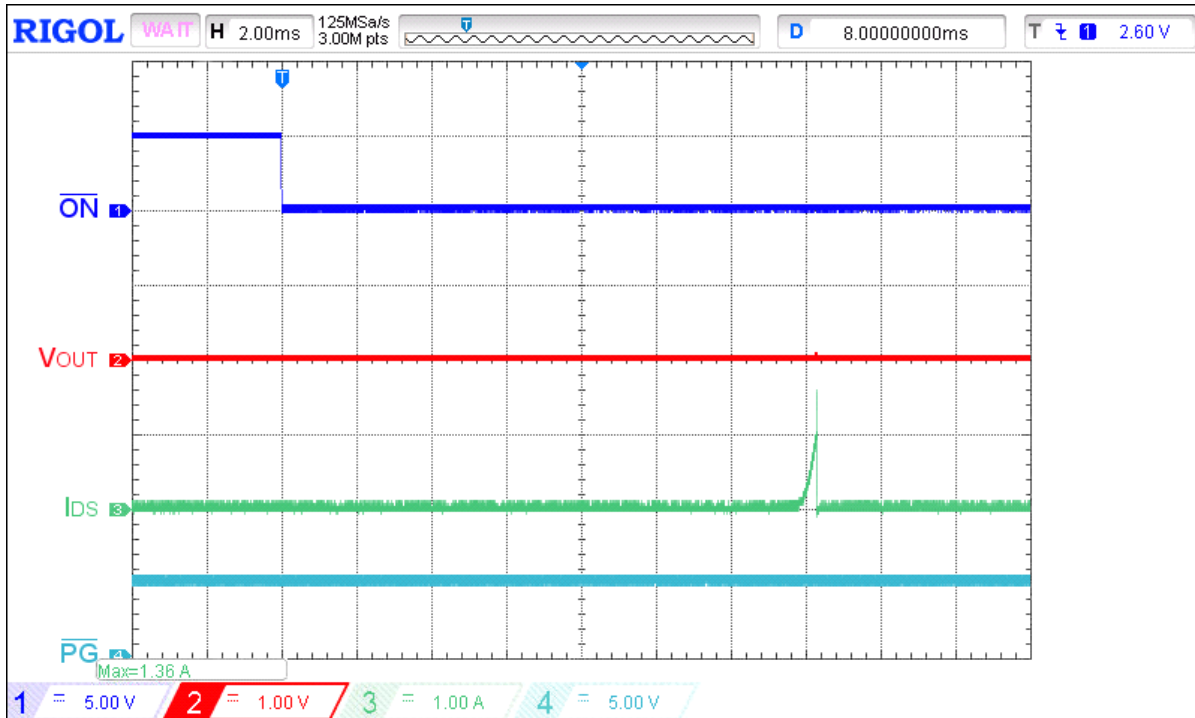


Figure 19. Startup Current Protection operation waveform for  $V_{IN} = 2.5\text{ V}$  (extended view)

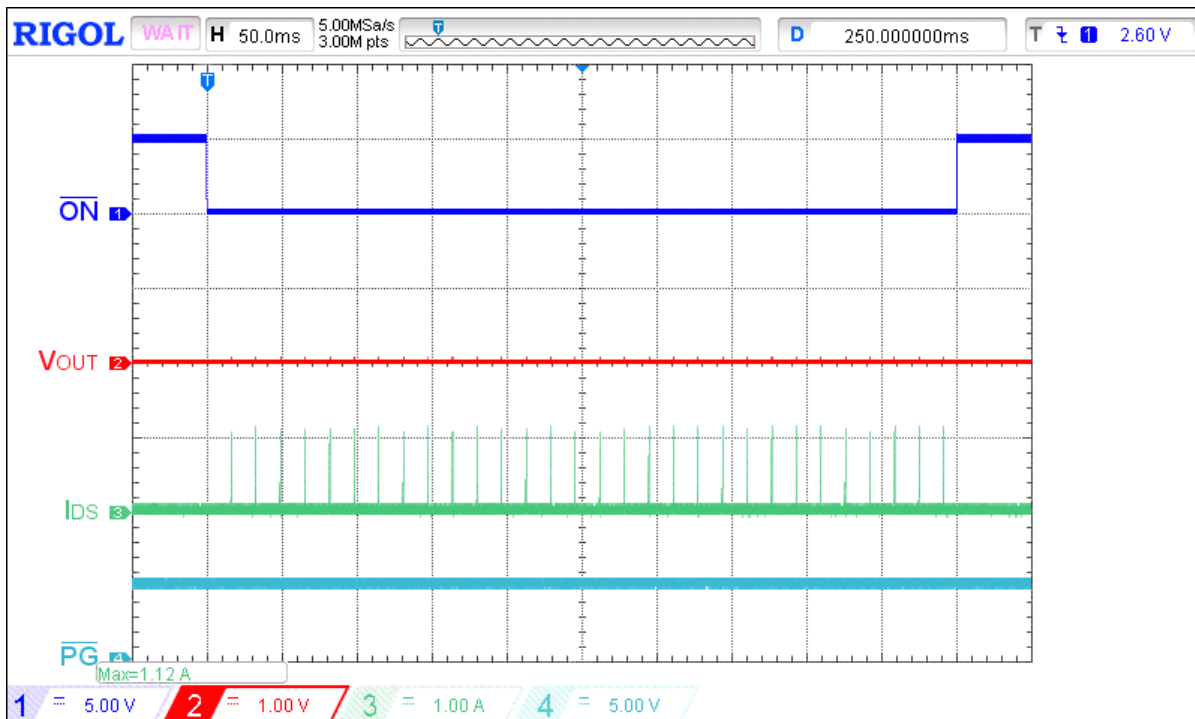


Figure 20. Startup Current Protection operation waveform for  $V_{IN} = 5\text{ V}$



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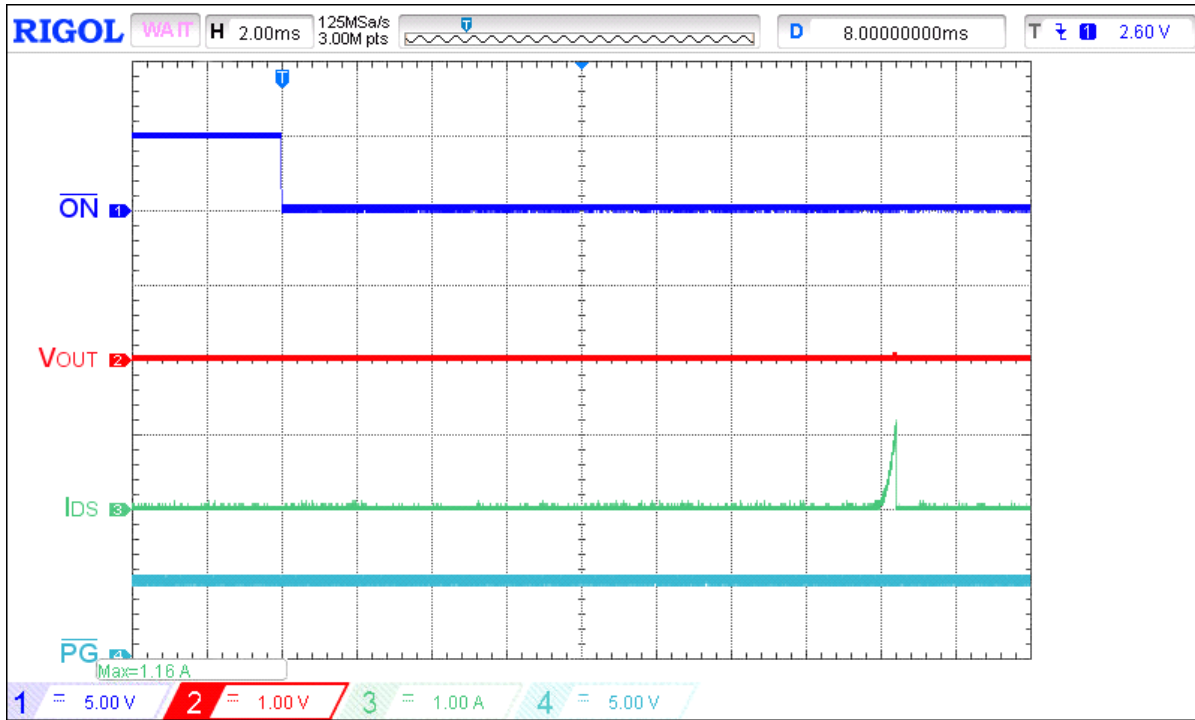


Figure 21. Startup Current Protection operation waveform for  $V_{IN} = 5\text{ V}$  (extended view)

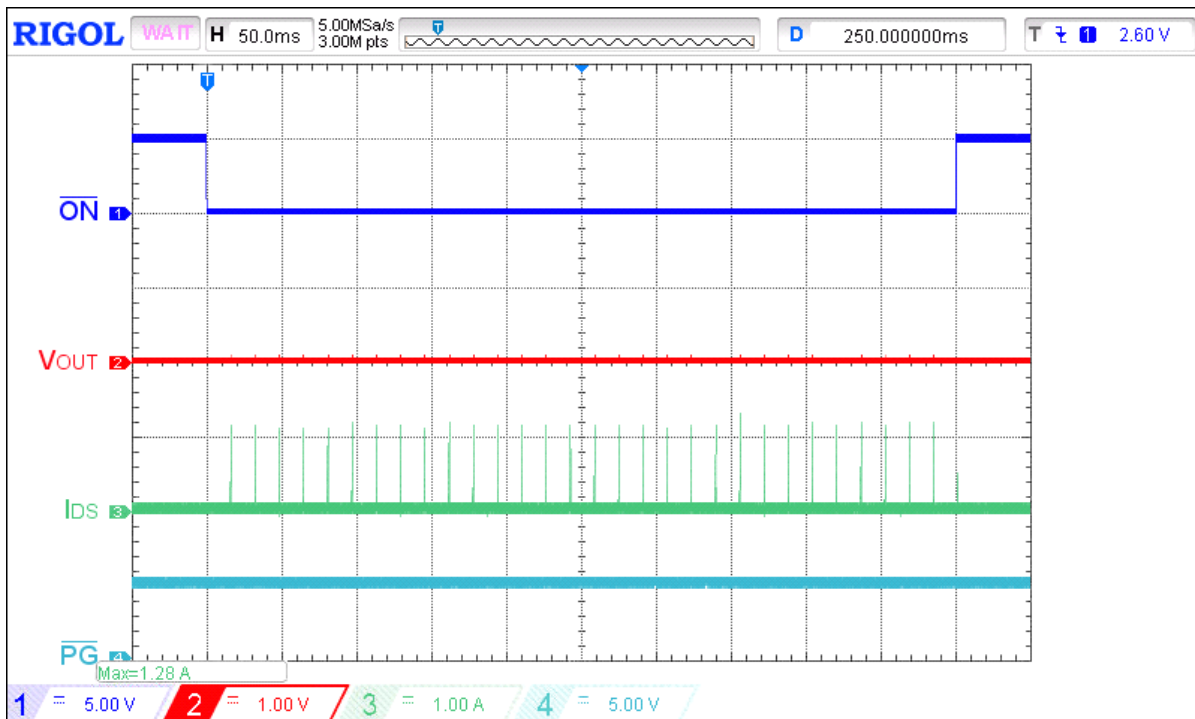


Figure 22. Startup Current Protection operation waveform for  $V_{IN} = 9\text{ V}$

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with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

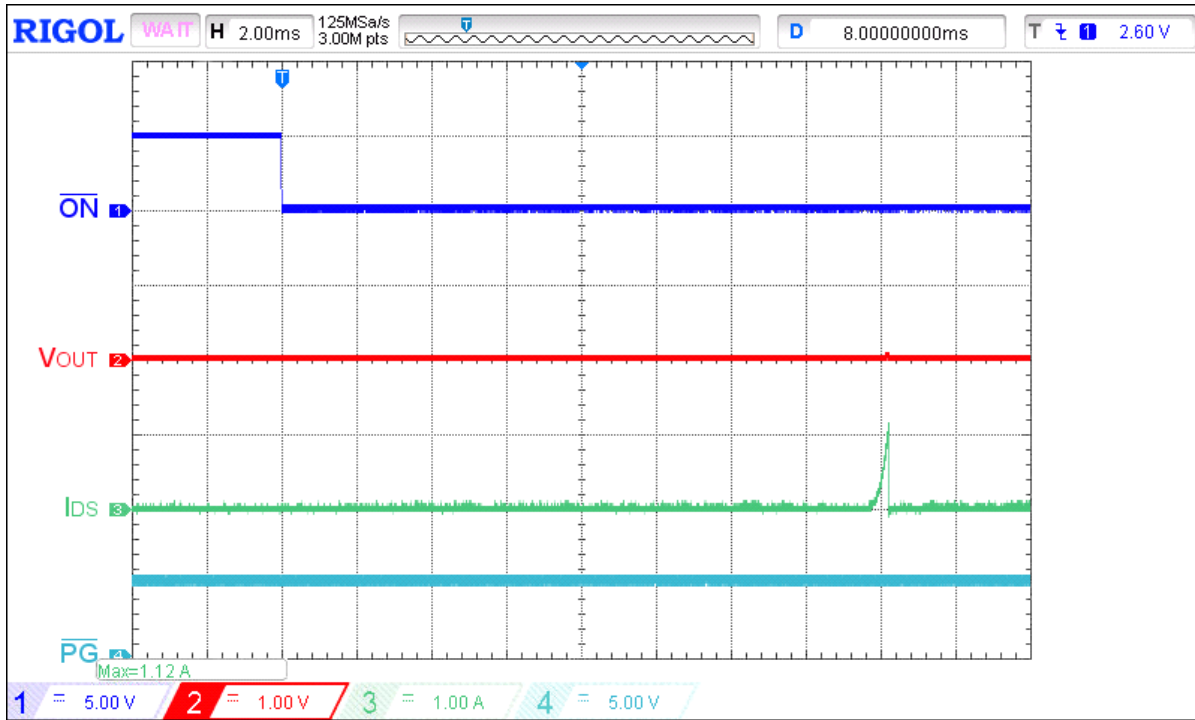


Figure 23. Startup Current Protection operation waveform for  $V_{IN} = 9\text{ V}$  (extended view)

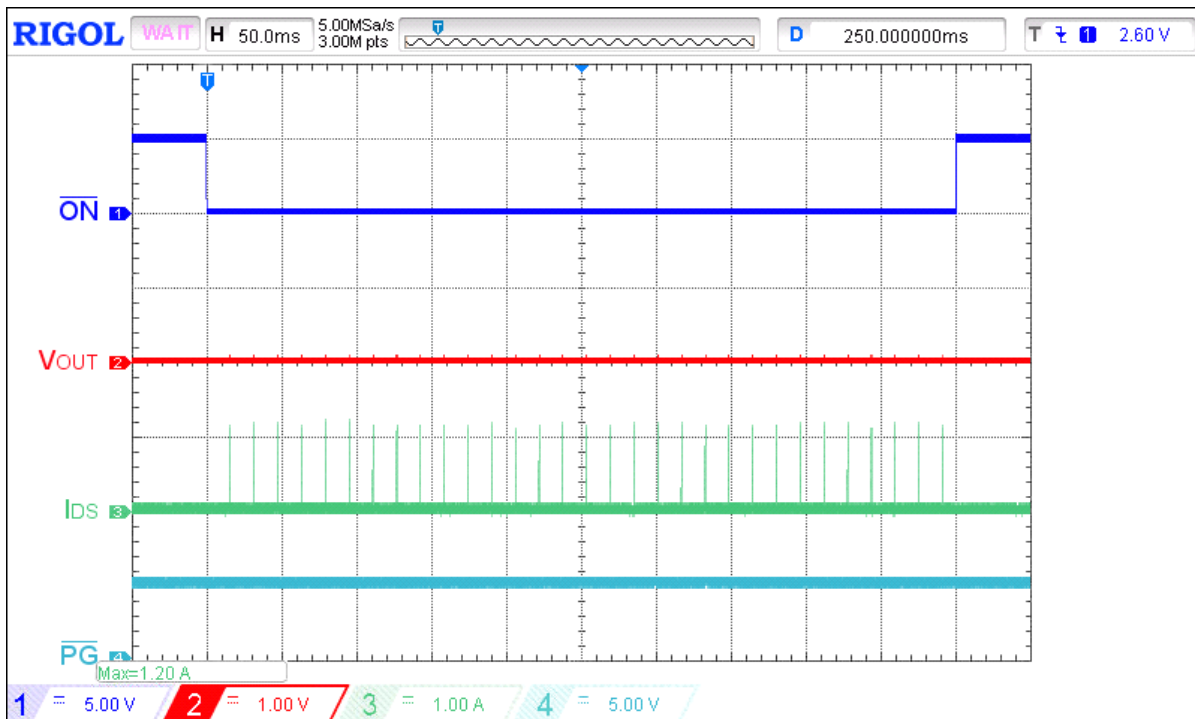


Figure 24. Startup Current Protection operation waveform for  $V_{IN} = 12\text{ V}$

A 23 mΩ, 4.5 A nFET Integrated Power Switch  
with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

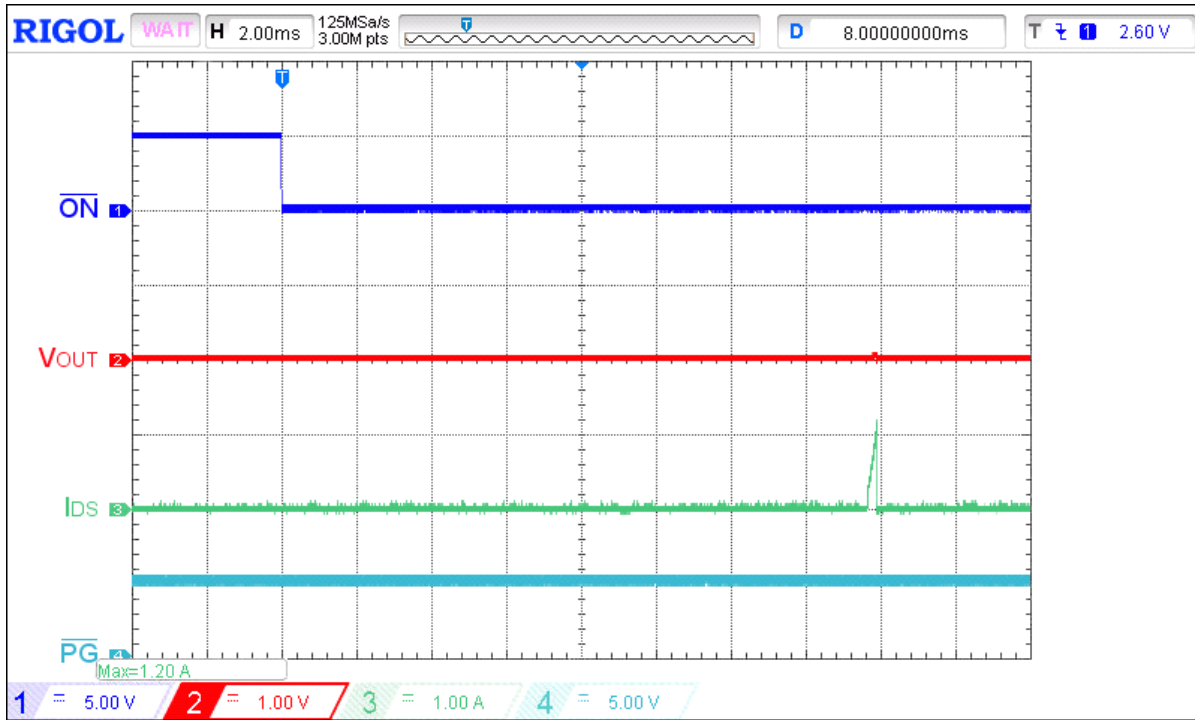


Figure 25. Startup Current Protection operation waveform for  $V_{IN} = 12\text{ V}$  (extended view)

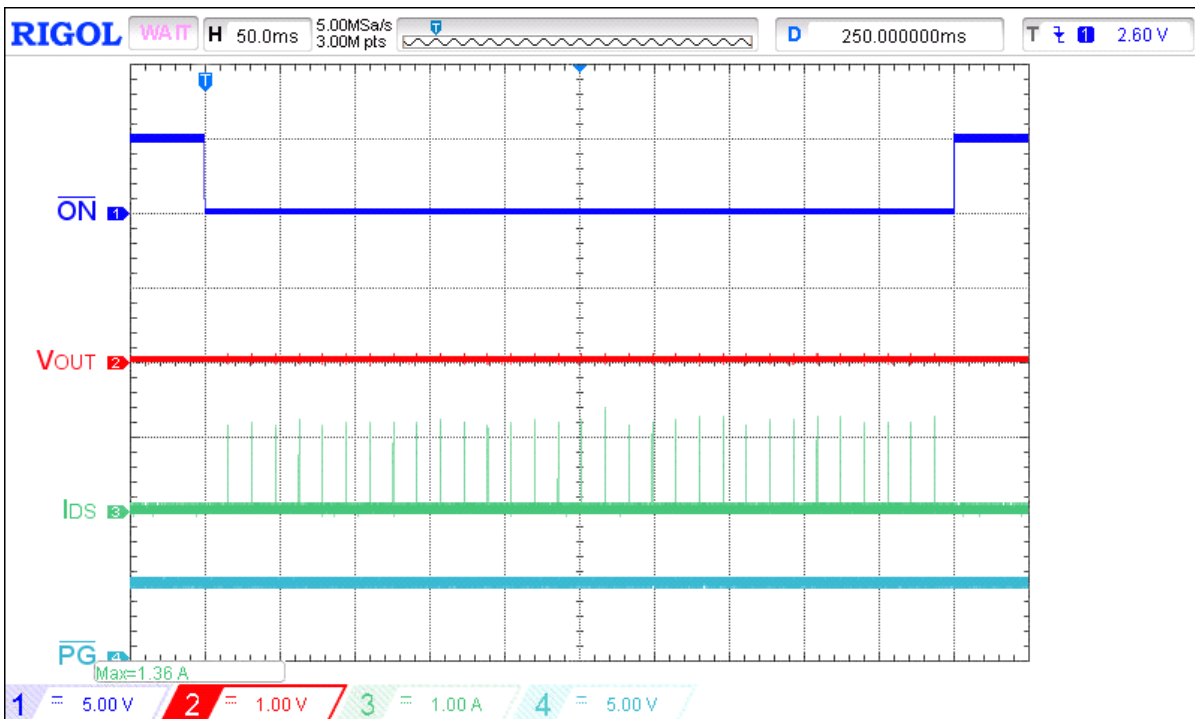


Figure 26. Startup Current Protection operation waveform for  $V_{IN} = 20\text{ V}$

A 23 mΩ, 4.5 A nFET Integrated Power Switch  
with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

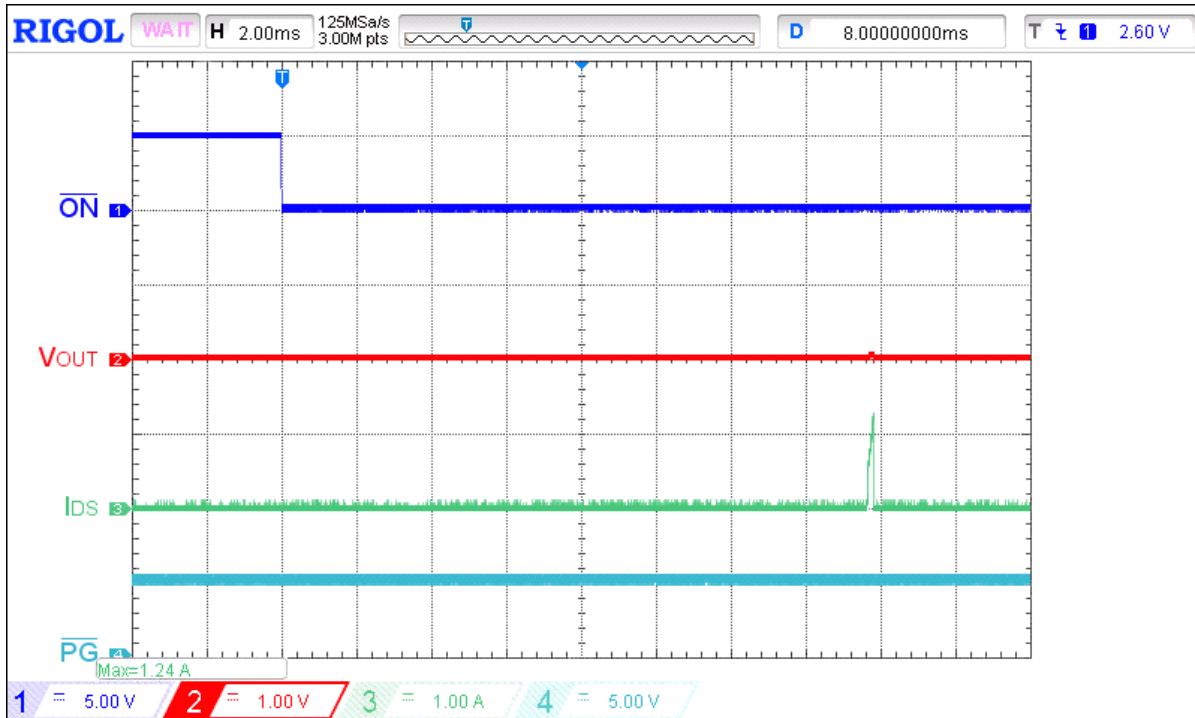


Figure 27. Startup Current Protection operation waveform for  $V_{IN} = 20\text{ V}$  (extended view)

Typical Power Up/Down Operation Waveform

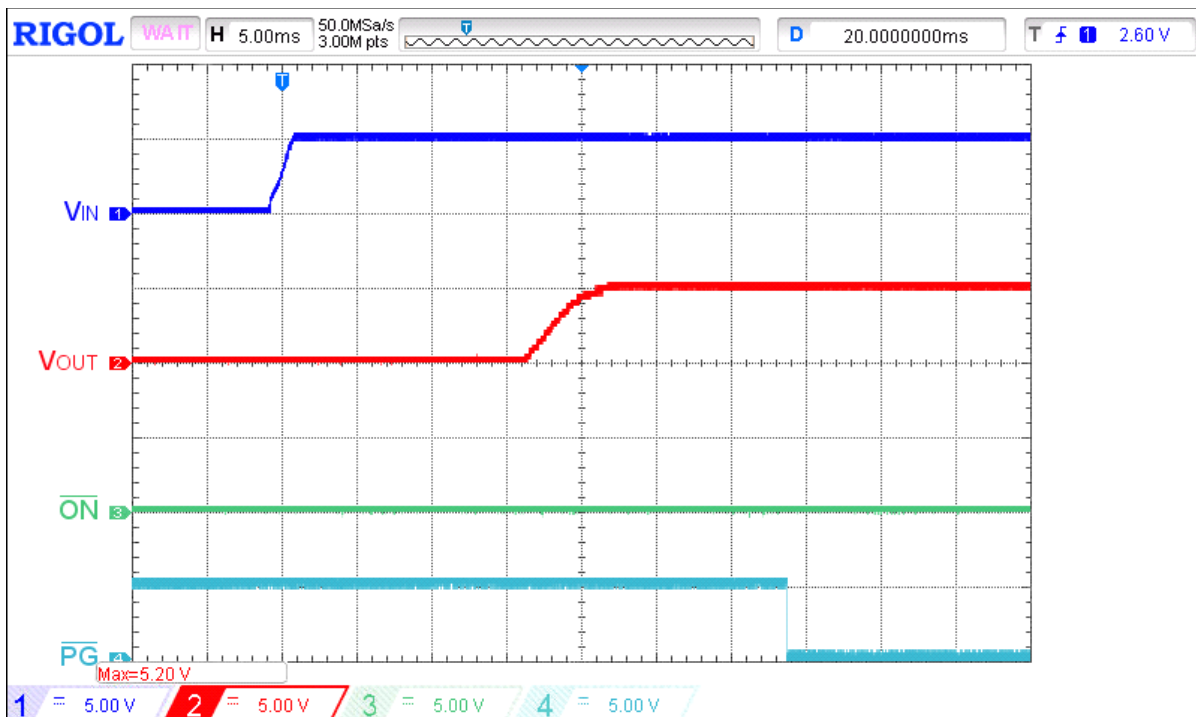


Figure 28. Typical Power Up operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 100\ \Omega$

A 23 m $\Omega$ , 4.5 A nFET Integrated Power Switch  
with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

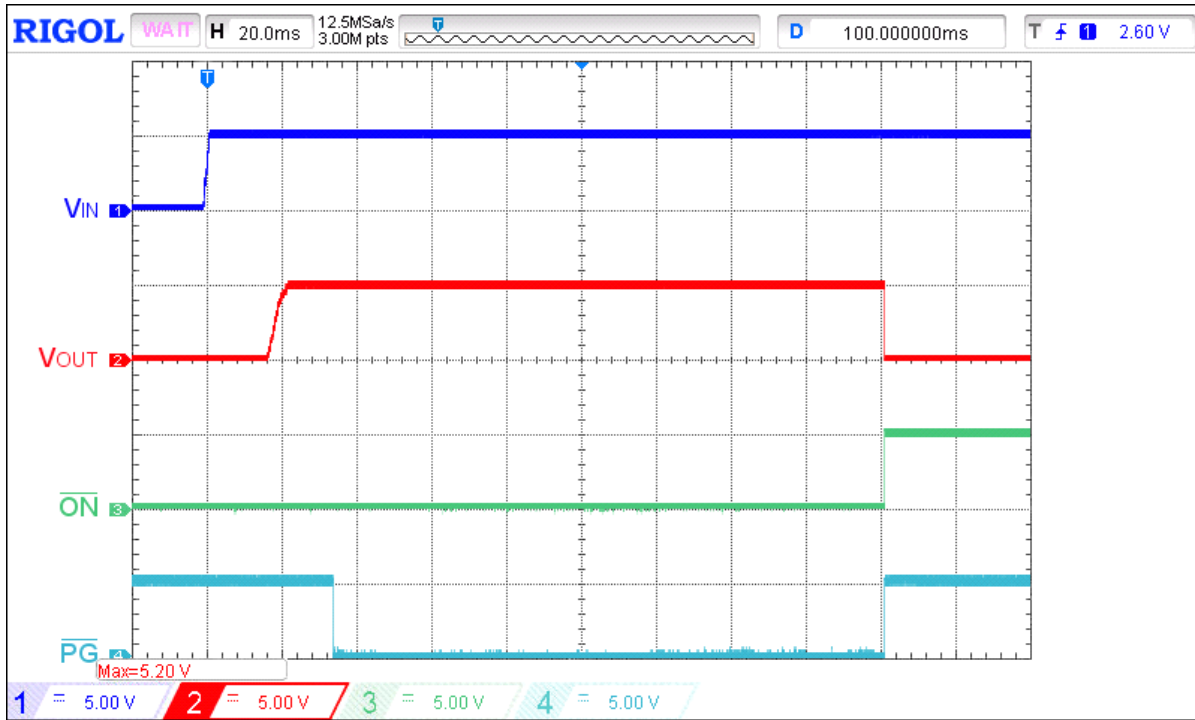
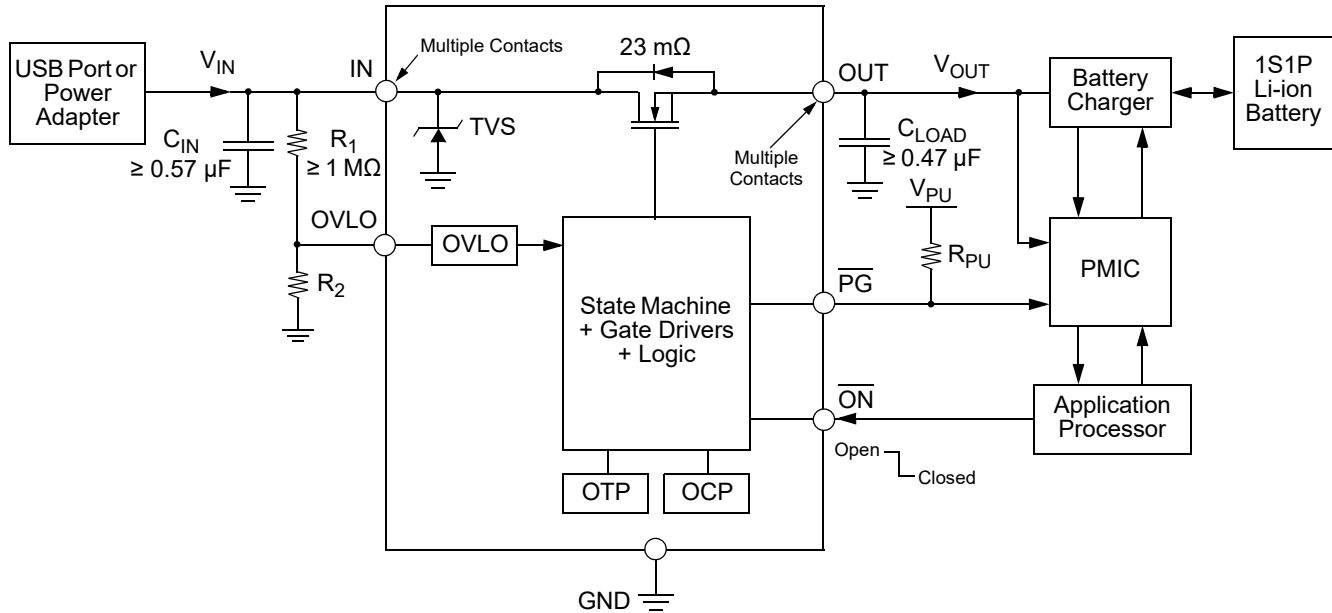


Figure 29. Typical Power Up/Down operation waveform for  $V_{IN} = 5\text{ V}$ ,  $R_{LOAD} = 100\ \Omega$

A 23 mΩ, 4.5 A nFET Integrated Power Switch with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

Applications Information

Typical Application Circuit



VIN Over-Voltage Lockout (OVLO) Calculation

V<sub>OVLO</sub> can be set externally and override the SLG59H1313C's default OVP by connecting an external resistor-divider to the OVLO pin.

The following equation produces the desired trip voltage and resistor values:

$$V_{OVLO} = V_{OVLO\_TH} \times \left( 1 + \frac{R_1}{R_2} \right)$$

Recommended minimum R<sub>1</sub> = 1 MΩ.

Since the minimum recommended value for R<sub>1</sub> is 1 MΩ, the equation can be rewritten to isolate R<sub>2</sub> for a desired V<sub>OVLO</sub>:

$$R_2 = \frac{R_1}{\frac{V_{OVLO}}{V_{OVLO\_TH}} - 1}$$

On-The-Go (OTG) Functionality

During OTG operation, the SLG59H1313C's initially disabled and its power FET bulk diode becomes forward biased. The bulk diode forward drop when conducting is approximately 0.7 V and remains forward biased until the applied V<sub>IN</sub> rises higher than 2.5 V. While the IC is disabled and its FET body diode is forward biased, the max DC current through the diode is 1.8 A. This current is limited by the thermal performance of the IC (0.7 V x 1.8 A = 1.26 W). Since sustained DC power dissipation in the OFF state should be minimized, the FET's body diode can withstand transient current operation so long as the max limit is never exceeded. To enable the operation of the SLG59H1313C, its ON pin must be pulled LOW. The time-domain profile of any transient current through the bulk diode should not exceed the RC time constant formed by the C<sub>IN</sub> and C<sub>LOAD</sub> capacitors. At the system level, over-voltage and over-current protection should be provided external to the SLG59H1313C.

## A 23 mΩ, 4.5 A nFET Integrated Power Switch with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

### Layout Guidelines:

1. Since the IN and OUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in [Figure 30](#), illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C<sub>IN</sub> and output C<sub>LOAD</sub> low-ESR capacitors as close as possible to the SLG59H1313C's IN and OUT pins;
3. The GND pin should be connected to system analog or power ground plane.

### SLG59H1313C Evaluation Board:

A HFET1 Evaluation Board for SLG59H1313C is designed according to the statements above and is illustrated on [Figure 30](#). Please note that evaluation board has D\_Sense and S\_Sense pads. They cannot carry high currents and dedicated only for RDS<sub>ON</sub> evaluation.

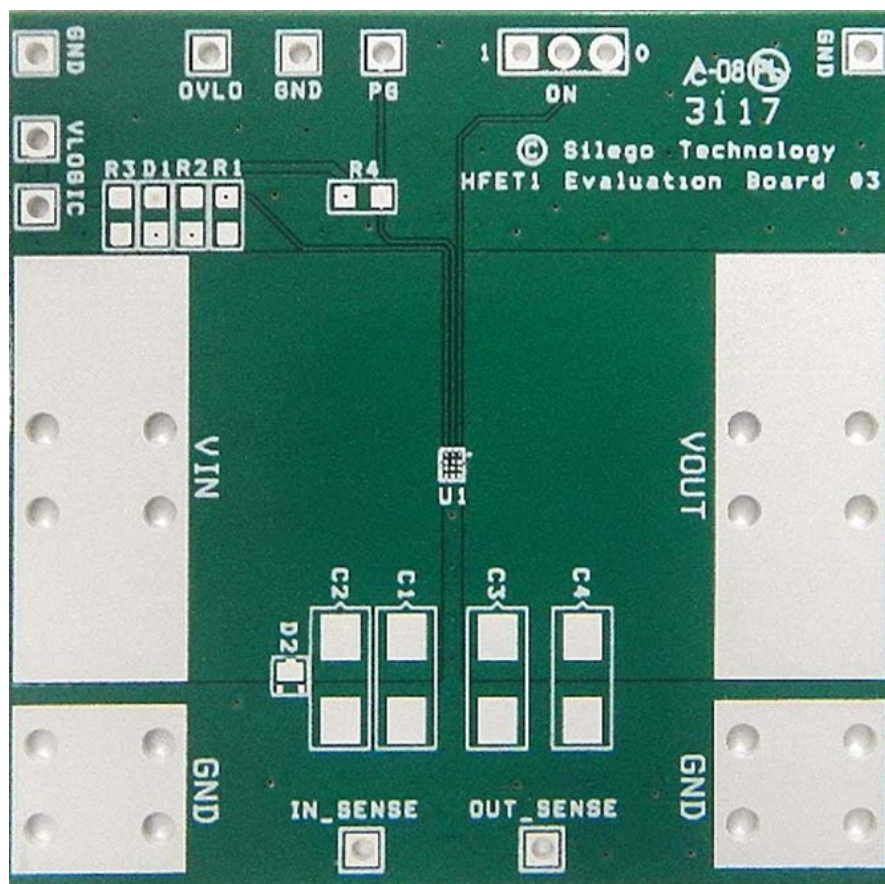


Figure 30. SLG59H1313C Evaluation Board

A 23 mΩ, 4.5 A nFET Integrated Power Switch with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

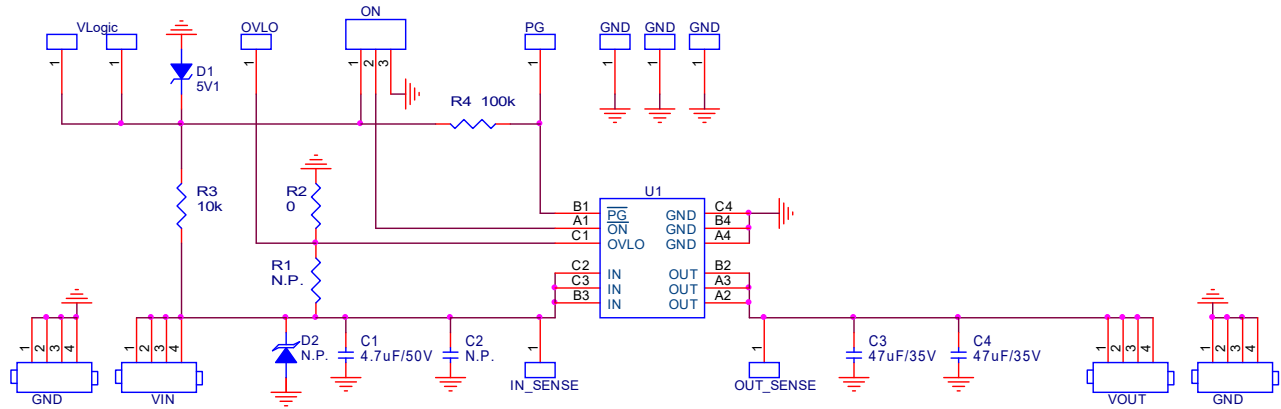


Figure 31. SLG59H1313C Evaluation Board Connection Circuit

Basic Test Setup and Connections

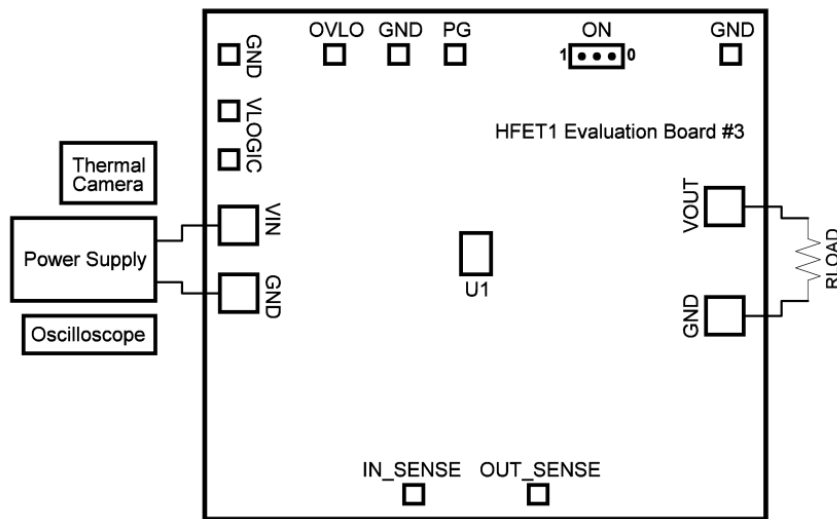


Figure 32. SLG59H1313C Evaluation Board Connection Circuit

EVB Configuration

1. Connect oscilloscope probes to VIN, VOUT, ON, etc.;
2. Using resistor divider for OVLO pin set desired  $V_{IN\_OVLO}$  threshold or tie OVLO pin to GND in case of using internal  $V_{IN\_OVLO}$  threshold;
3. Turn on Power Supply and set desired  $V_{IN}$  from 2.5 V ... 20 V;
4. Toggle the ON signal High or Low to observe SLG59H1313C operation.



A 23 mΩ, 4.5 A nFET Integrated Power Switch  
with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

Package Top Marking System Definition



1313 - Part ID Field  
WW - Date Code Field<sup>1</sup>  
NNN - Lot Traceability Code Field<sup>1</sup>  
A - Assembly Site Code Field<sup>2</sup>  
RR - Part Revision Code Field<sup>2</sup>

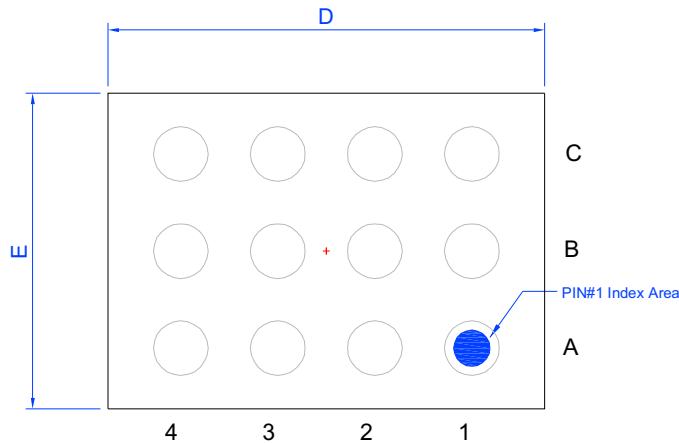
Note 1: Each character in code field can be alphanumeric A-Z and 0-9  
Note 2: Character in code field can be alphabetic A-Z

A 23 mΩ, 4.5 A nFET Integrated Power Switch  
with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

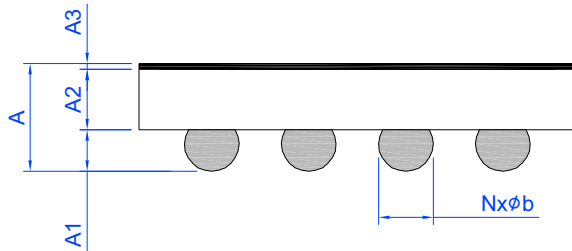
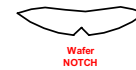
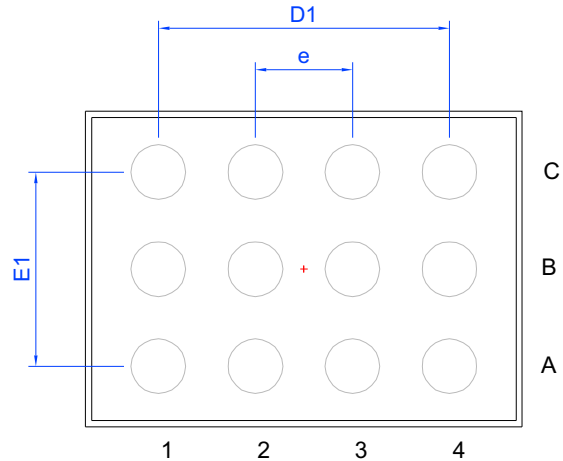
Package Drawing and Dimensions

12 Lead WLCSP Package

**Laser Marking View**



**Bump View**



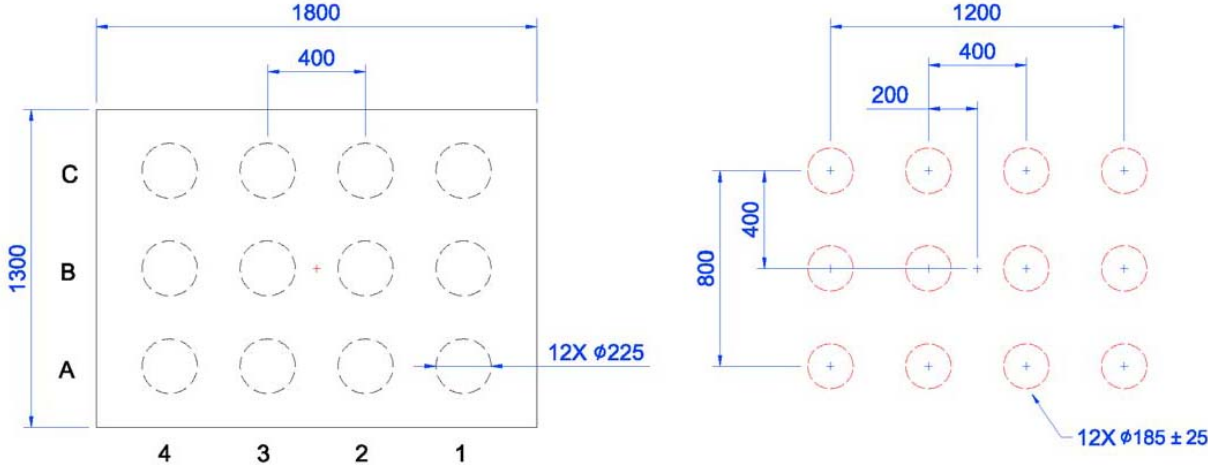
**SIDE View**

UNIT: mm							
Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.390	0.445	0.500	D	1.770	1.800	1.830
A1	0.145	0.170	0.195	E	1.270	1.300	1.330
A2	0.225	0.250	0.275	D1	1.20 BSC		
A3	0.020	0.025	0.030	E1	0.80 BSC		
b	0.200	0.225	0.250	e	0.40 BSC		
				N	12 (bump)		

# SLG59H1313C

A 23 mΩ, 4.5 A nFET Integrated Power Switch with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

## SLG59H1313C 12-pin WLCSP PCB Landing Pattern



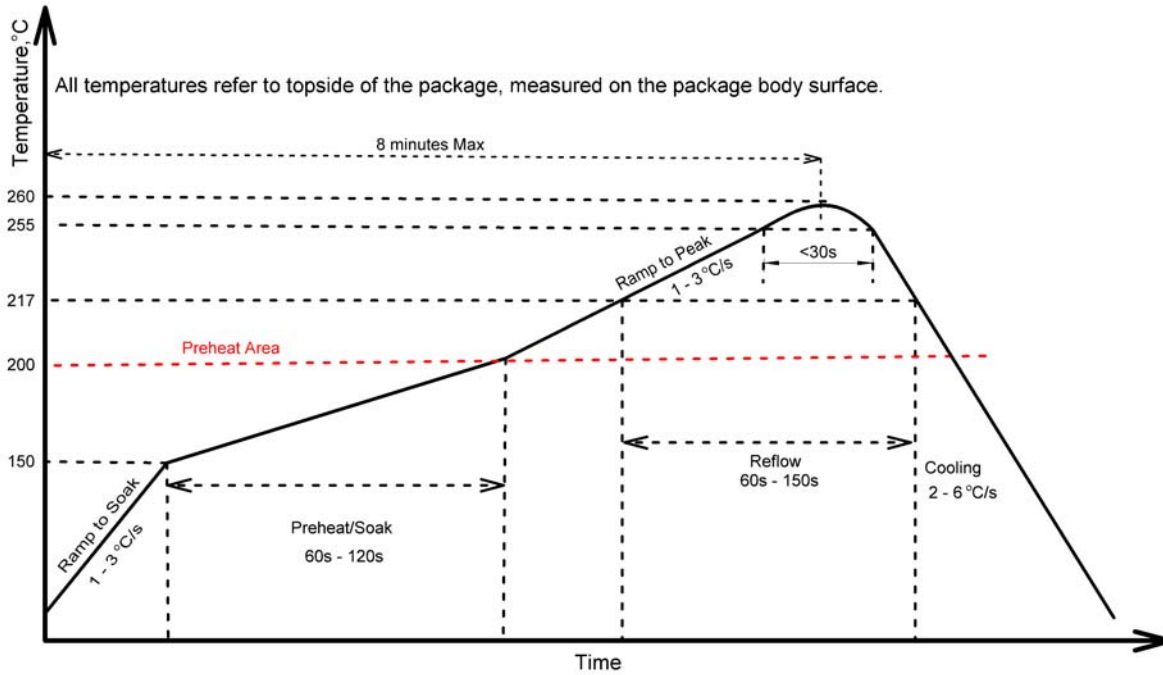
Solder mask detail (not to scale)

**Unit:  $\mu\text{m}$**

A 23 mΩ, 4.5 A nFET Integrated Power Switch with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

Recommended Reflow Soldering Profile

For successful reflow of the SLG59H1313C a recommended thermal profile is illustrated below:



Note: This reflow profile is for classification/preconditioning and are not meant to specify board assembly profile. Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed parameters depicted on figure above.

Please see more information on IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.17 mm<sup>3</sup> (nominal).

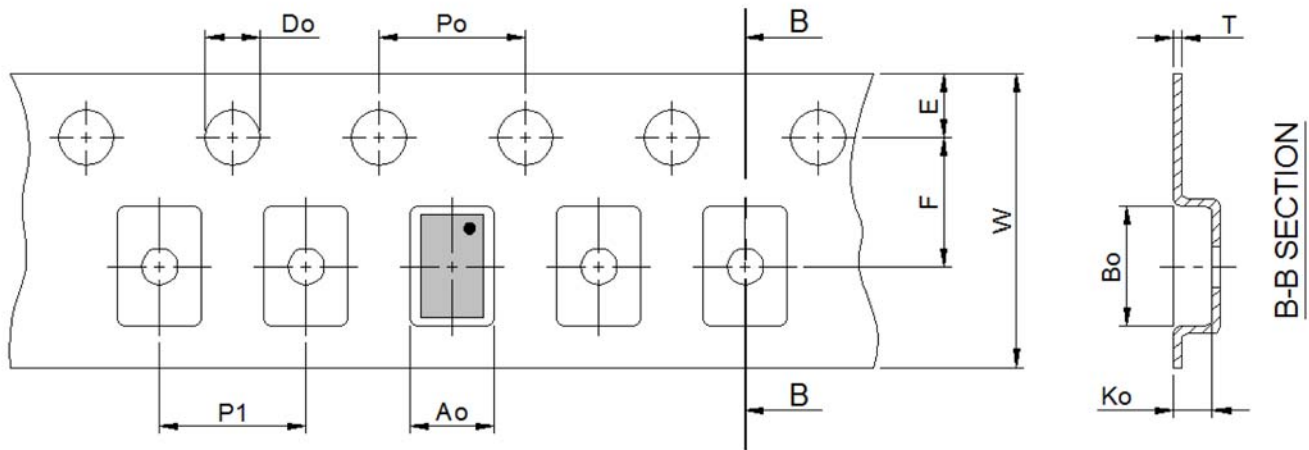
A 23 mΩ, 4.5 A nFET Integrated Power Switch  
with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
WLCSP 12L 1.3 x 1.8 mm 0.4P Green	12	1.3 x 1.8 x 0.5	3,000	3,000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width	Tape Thickness
	A0	B0	K0	P0	P1	D0	E	F	W	T
WLCSP 12L 1.3 x 1.8 mm 0.4P Green	1.51	2.04	0.67	4	4	1.5	1.75	3.5	8	0.25



Note: Orientation in carrier: Pin1 is at upper right corner (Quadrant 2).

Refer to EIA-481 specification

A 23 m $\Omega$ , 4.5 A nFET Integrated Power Switch  
with Surge Protection and Adjustable OVP in a 2.34 mm<sup>2</sup> WLCSP

### Revision History

Date	Version	Change
12/20/2018	1.04	Added Layout Guidelines
7/24/2018	1.03	Updated V <sub>OVLO_TH</sub> spec to 2 decimal places
7/09/2018	1.02	Fixed typos
6/20/2018	1.01	Fixed typo in Landing Pattern Updated style and formatting
3/5/2018	1.00	Production Release