ON Semiconductor®

Product Bulletin

Document #:PB23685Z
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Title of Change:	NCV8412-D Datasheet Update
Effective date:	13 Jan 2021
Contact information:	Contact your local ON Semiconductor Sales Office or Jana.Kubincova@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Change Category - other
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

ON Semiconductor Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

In the Maximum Ratings table, parameters Total Power Dissipation and Thermal Resistance were changed. The Typical curves regarding the thermal resistances were also changed – Figure 21. and Figure 23. (previously Figure 22.).

The reason for the change is that at the initial release only the faster and therefore less accurate simulations were used to be able to release the product within the required timeframe. Since then, the more detailed and more accurate simulations were completed, so these results should be more closely represent the device's true behaviour.

Removing the Junction-to-Case (Top) because the definition of the Junction-to-Case (Top) parameter assumes, that the heat generated in the die is dissipated upwards through the mold compound of the device. However, in practical application that never happens, as the lead frame has much higher conductivity, so most of the heat is dissipated downwards – characterized by the parameter Junction-to-Case (Soldering Point).

Except these changes, three new typical curves were added, related to the thermal characteristics of the SOIC-8 Dual package – Figures 22, 24 and 25.

Please note that although these parameters and curves are shown in the datasheet, they are not guaranteed parameters by any means and are solely based on calculations of the expected thermal behaviour of the materials used during the assembly process.

The change will not impact form, fit, or function of product(s).

Update Total Power Dissipation and Thermal Resistance parameters in Maximum ratings table on page 2. Remove Junction-to-Case (Top) for SOT-223 and SOIC-8 Dual.

Current datasheet

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–to–Source Voltage Internally Clamped	V_{DSS}	42	V
Drain–to–Gate Voltage Internally Clamped	V_{DG}	42	V
Gate–to–Source Voltage	V_{GS}	±14	V
Drain Current – Continuous	I_D	Internally Limited	
Total Power Dissipation (SOT–223) @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	1.44 2.20	W
Total Power Dissipation (SOIC–8 Dual), both channels loaded equally @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	1.14 1.53	W
Total Power Dissipation (SOIC–8 Dual), only one channel loaded @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	0.93 1.18	W
Thermal Resistance (SOT–223) Junction–to–Ambient (Note 1) Junction–to–Ambient (Note 2) Junction–to–Case (Soldering Point) Junction–to–Case (Top)	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$ $R_{\theta JCT}$	86.7 56.9 4.7 58	°C/W
Thermal Resistance (SOIC–8 Dual), both channels loaded equally Junction–to–Ambient (Note 1) Junction–to–Ambient (Note 2) Junction–to–Case (Soldering Point) Junction–to–Case (Top)	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$ $R_{\theta JCT}$	109.2 81.7 28.6 69	°C/W
Thermal Resistance (SOIC–8 Dual), only one channel loaded Junction–to–Ambient (Note 1) Junction–to–Ambient (Note 2) Junction–to–Case (Soldering Point) Junction–to–Case (Top)	$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$ $R_{\theta JCT}$	134.4 105.8 28.6 69	°C/W
Single Pulse Inductive Load Switching Energy (L = 50 mH, I_{Lpeak} = 2 A, V_{GS} = 5 V, R_G = 25 Ω, T_{Jstart} = 25°C)	E_{AS}	100	mJ
Load Dump Voltage (V_{GS} = 0 and 10 V, R_L = 22 Ω) (Note 3)	U_S*	55	V
Operating Junction Temperature	T_J	–40 to 150	°C
Storage Temperature	$T_{storage}$	–55 to 150	°C

Proposed change

Symbol	Value	Unit
V_{DSS}	42	V
V_{DG}	42	V
V_{GS}	± 14	V
I_D	Internally Limited	
P_D	1.28 2.19	W
P_D	0.57 0.78	W
P_D	0.93 1.20	W
$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$	97.0 57.0 7.9	°C/W
$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$	107.8 79.4 29.0	°C/W
$R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JS}$	133.6 103.8 29.1	°C/W
E_{AS}	100	mJ
U_S*	55	V
T_J	–40 to 150	°C
$T_{storage}$	–55 to 150	°C

Added Figure 22. RθJA vs. Copper Area – SOIC-8 Dual and updated Figure 21. . RθJA vs. Copper Area – SOT-223 on page 8.

Current datasheet

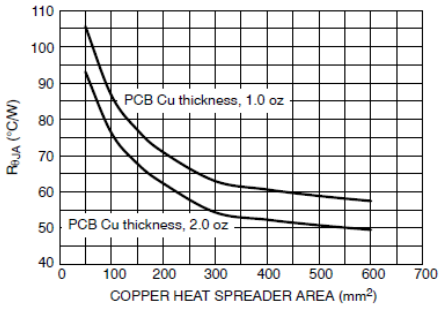

Figure 21. $R_{\theta JA}$ vs. Copper Area – SOT–223

Proposed changes

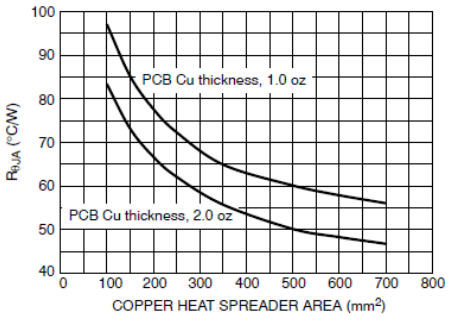

Figure 21. $R_{\theta JA}$ vs. Copper Area – SOT–223

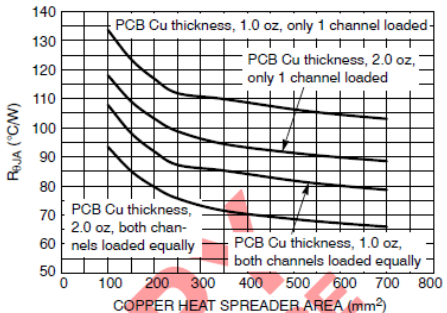

Figure 22. $R_{\theta JA}$ vs. Copper Area – SOIC–8 Dual

Update of Figure 23 - Transient Thermal Resistance − SOT−223 on page 8

Current datasheet

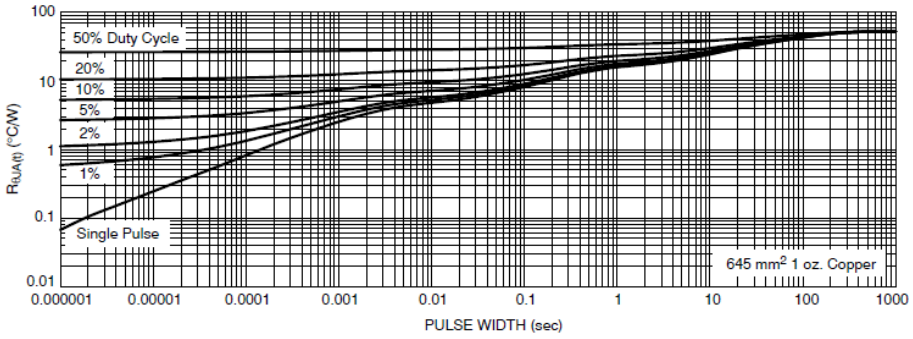

Figure 22. Transient Thermal Resistance − SOT−223

Proposed changes

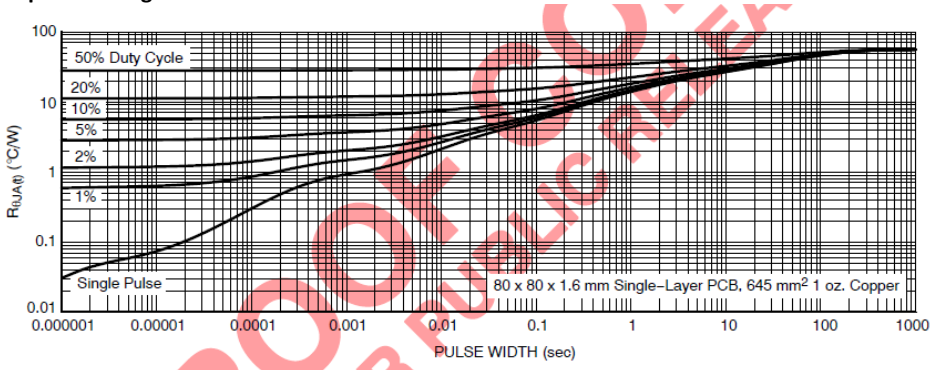

Figure 23. Transient Thermal Resistance − SOT−223

Added Figure 24. Transient Thermal Resistance − SOIC−8 Dual, only 1 channel loaded and Figure 25. Transient Thermal Resistance − SOIC−8 Dual, both channels loaded equally on page 9.

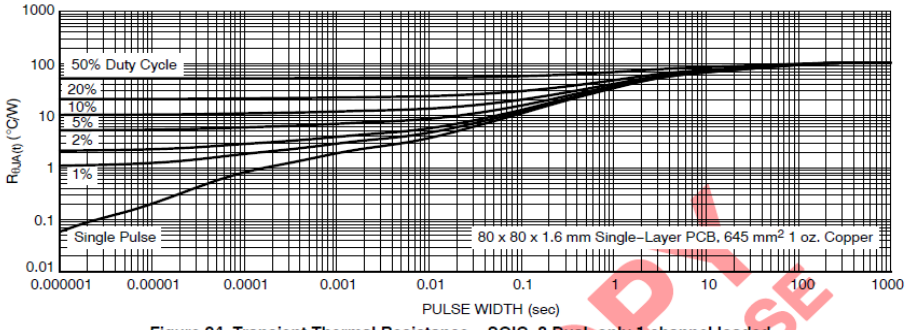

Figure 24. Transient Thermal Resistance − SOIC−8 Dual, only 1 channel loaded

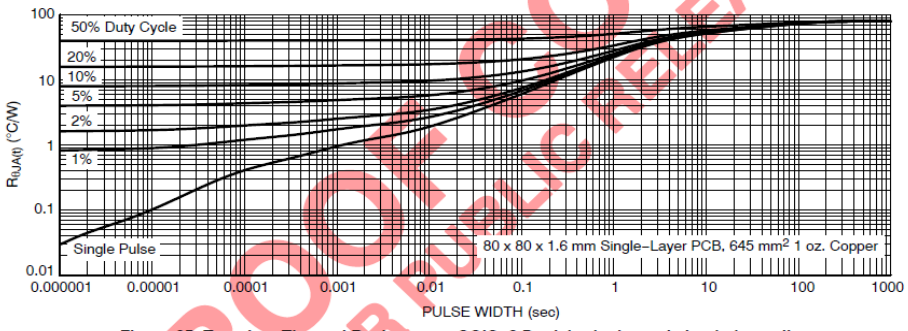

Figure 25. Transient Thermal Resistance − SOIC−8 Dual, both channels loaded equally

Updated Table Device Ordering Information

Current datasheet

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCV8412ASTT1G	8412A	SOT−223 (Pb−Free)	1,000 / Tape & Reel
NCV8412ASTT3G	8412A	SOT−223 (Pb−Free)	1,000 / Tape & Reel
NCV8412ADDR2G (In Development)	8412AD	SOIC−8 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Proposed changes

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCV8412ASTT1G	8412A	SOT−223 (Pb−Free)	1,000 / Tape & Reel
NCV8412ASTT3G	8412A	SOT−223 (Pb−Free)	1,000 / Tape & Reel
NCV8412ADDR2G	8412AD	SOIC−8 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

NCV8412ASTT1G	NCV8412ASTT3G	NCV8412ADDR2G

Appendix A: Changed Products

Product	Customer Part Number	Qualification Vehicle	New Part Number	Replacement Supplier
NCV8412ASTT1G				
NCV8412ASTT3G				