



# MC68EN302

## Product Brief

# Integrated Multiprotocol Processor with Ethernet

Freescale introduces a version of the well-known MC68302 Integrated Multiprotocol Processor (IMP) with Ethernet and DRAM controllers. It is known as the MC68EN302, and expands a family of devices based on the MC68302.

The Ethernet controller has a 16-bit interface, resides on the 68000 bus and provides complete IEEE 802.3 compatibility. The programming model is adopted from the standard 68302 programming model. The DRAM controller is adopted from the MC68306 product. It is enhanced to support both parity and external bus masters.

The MC68EN302 is packed in a low profile 144 TQFP.

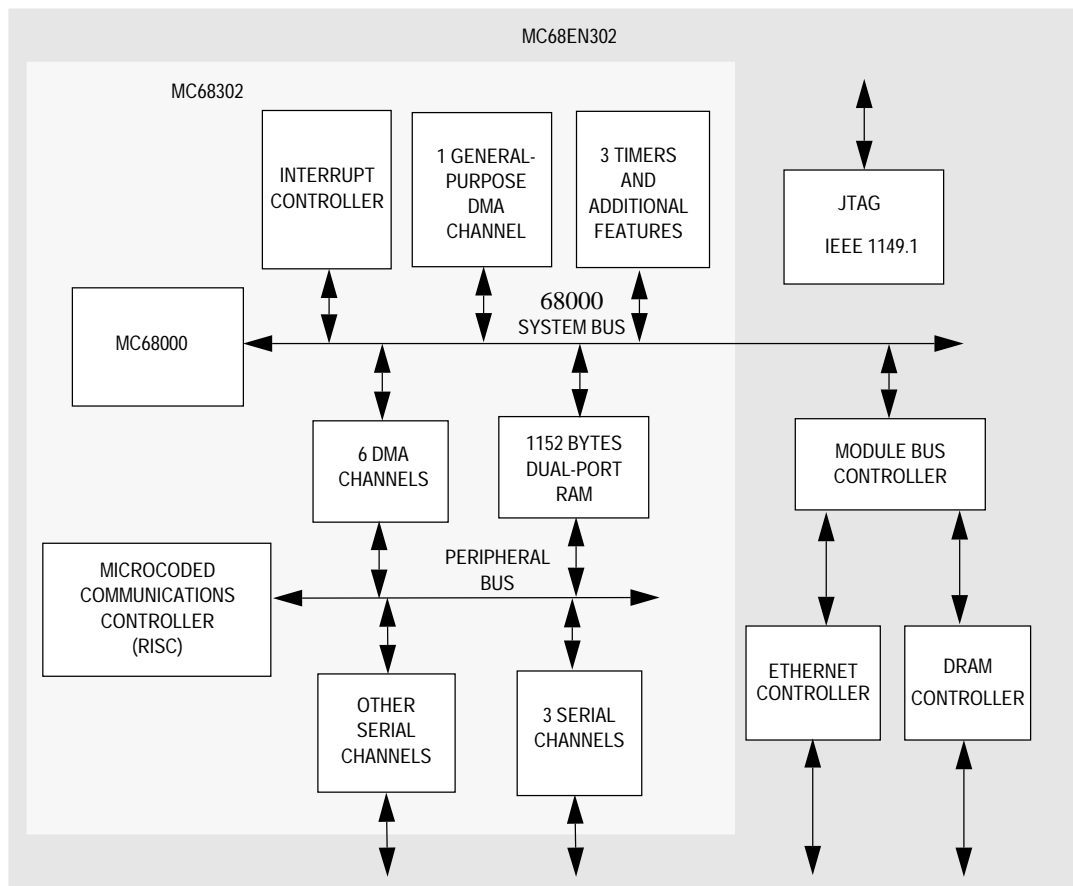


Figure 1. MC68EN302 Block Diagram

This document contains information on a product under development. Freescale reserves the right to change or discontinue this product without notice.

**SEMICONDUCTOR PRODUCT INFORMATION**

## FEATURE LIST

The following features are incorporated into the MC68EN302 device:

- Full Complement of Existing Three SCC's Plus Ethernet Channel
- Ethernet Channel Fully Compliant with IEEE 802.3 Specification.
- Supports Data Rates up to 10 Mbps.
- Supports the "68302" Style Programming Model.
- On-Chip Descriptors Lower Processor Bus Bandwidth Requirements.
- Separate 128 Byte FIFOs for Transmit and Receive.
- Automatic Internal Retransmission (which Frees the Processor Bus).
- Automatic Internal Flushing of Receive FIFO During Collisions (which Frees the Processor Bus).
- Dynamic Bus Sizing Support for 8-Bit Devices
- Glueless Dynamic RAM Controller without External Bus Master
- Address Muxing Support for External Bus Masters Using DRAM Controller
- Fully IEEE 1149.1 JTAG Compliant
- 144 TQFP Package for Up to 25 MHz

## ETHERNET CONTROLLER

The Ethernet controller consists of a Ethernet protocol core, transmit and receive FIFOs, and a 16-bit wide data/control interface to a 68000 bus (refer to Figure 2). The Ethernet protocol core (EPC) provides compatibility with the IEEE 802.3 Ethernet standard. The transmit and receive FIFOs allow automatic handling of collisions and collision fragments by the EPC, and they also provide for bus latency that can be encountered by the DMA channels. Separate DMA channels are used for transmit and receive data paths. A dual-port RAM is used for the on-chip buffer descriptors. A buffer descriptor control (BDC) block updates the buffer descriptors. Control status registers are used for direct control of all of the blocks in the Ethernet controller.

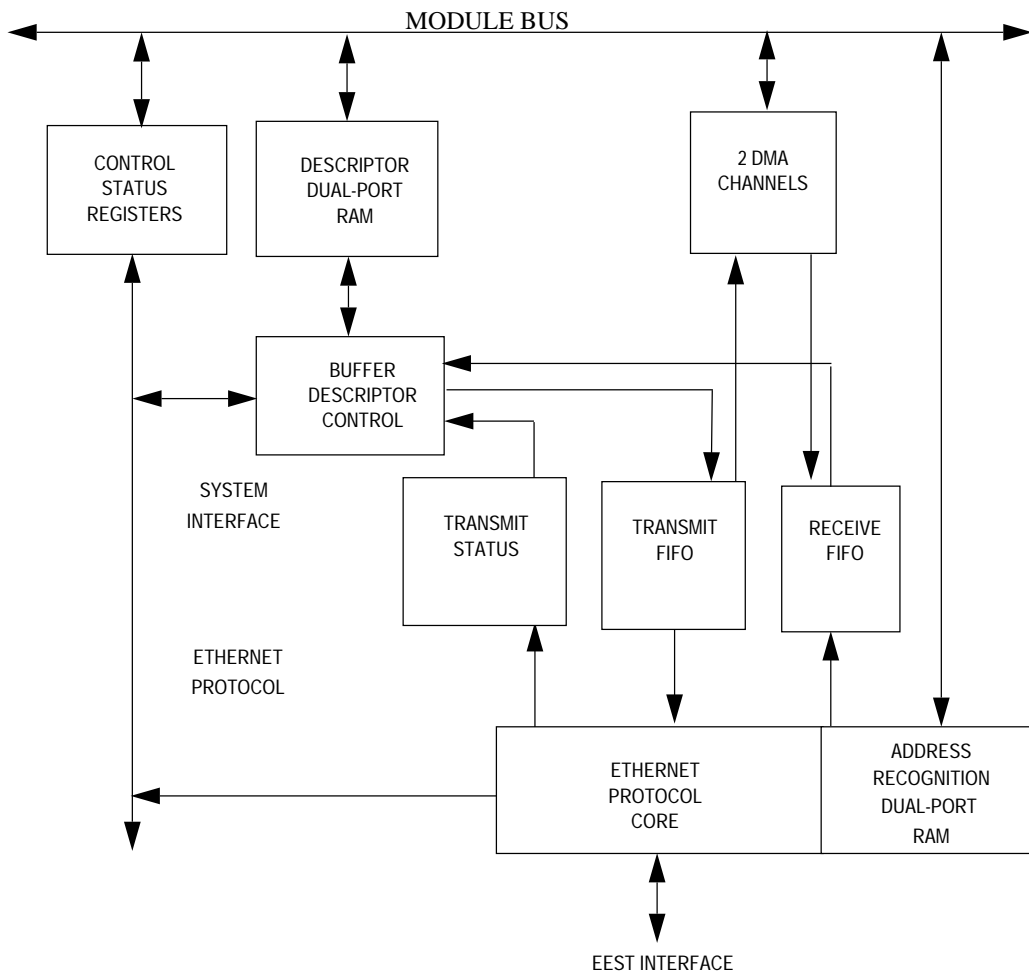
## ETHERNET FEATURES

- Does Not Affect Performance of Existing SCCs
- 802.3 MAC Layer Support
- Compatible with 68160 EEST (Twisted Pair/AUI)
- Two Dedicated Ethernet DMA channels, Transmit and Receive
- Full-Duplex (Switched) Ethernet Support
- Up to 10 Mb/s Operation (20 Mb/s Full-Duplex)
- 128-Byte FIFO on both Transmit and Receive
- No CPU or Bus Overhead Required on Rx or Tx Frame Collisions
- 64 entry CAM with Hash Option
- 128 internal Buffer Descriptors
- Performs Framing Functions

## MC68EN302 PRODUCT INFORMATION

**For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)**

- Full Collision Support
- Receives Back-to-Back Frames
- Detection of Receive Frames That Are Too Long
- Multi-Buffer Data Structure
- Supports 48-Bit Addressing
- Heartbeat Indication
- Transmitter Network Management and Diagnostics
- Receiver Network Management and Diagnostics
- Loopback Mode for Testing
- Non-Aggressive Deferral Option
- Heartbeat Status and Interrupt Option
- Graceful Stop Command



**Figure 2. Ethernet Controller Block Diagram**

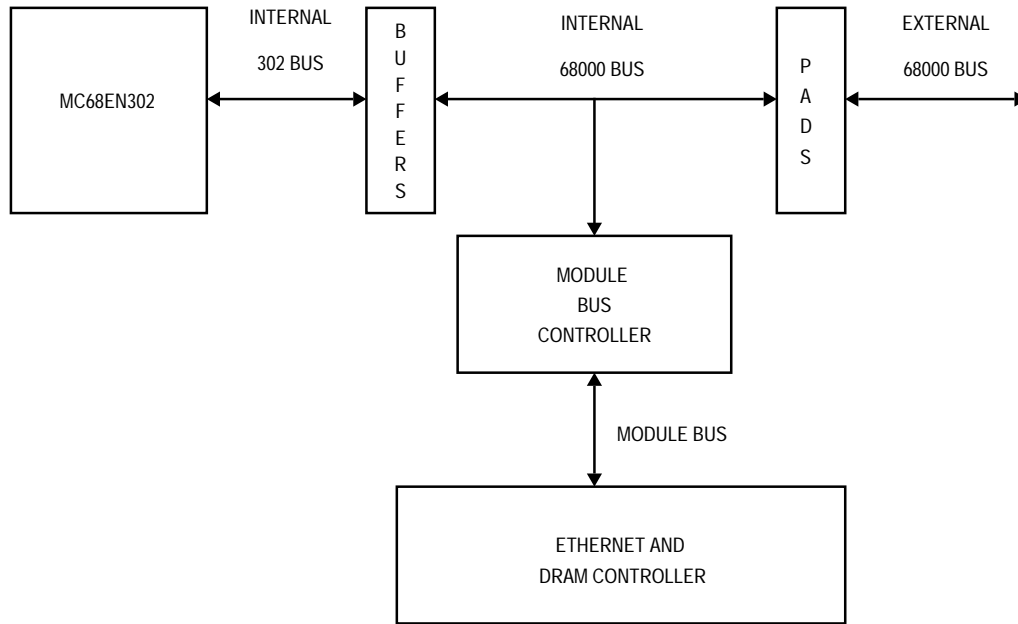
**MC68EN302 PRODUCT INFORMATION**

**For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)**

## MODULE BUS CONTROLLER

The MC68EN302 module bus controller provides basic interface capabilities to the module bus as well as basic system responsibilities. The features of the module bus controller are:

- Interface Between Internal 68000 bus and the Module Bus.
- Provision for Dynamic Bus Sizing, Using the Chip Select Logic of the 68302 Core.
- Handling of Interrupts for the Ethernet Controller and DRAM Controller.
- Coordination of Bus Mastership from External Sources, the Module Bus, and the MC68EN302 Core.



**Figure 3. BusStructure**

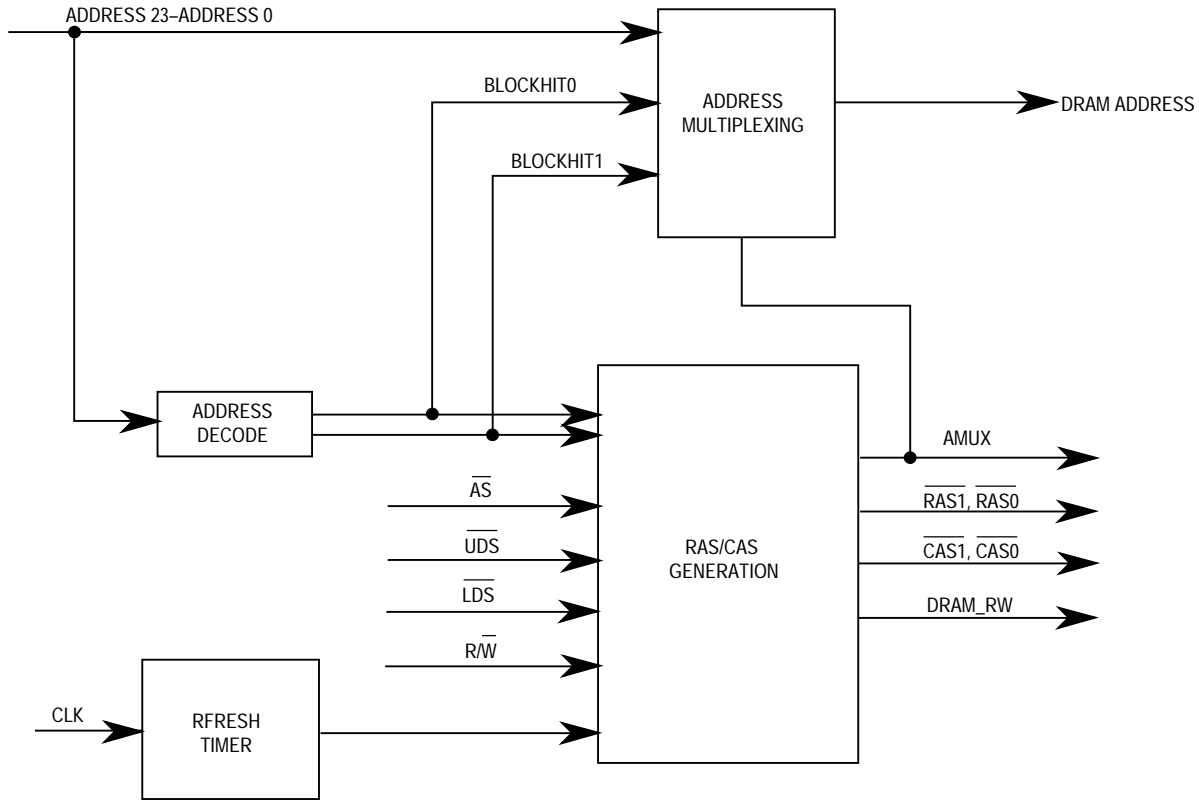
## DRAM CONTROLLER

- Provides two CAS lines
- Provides two RAS lines (two banks supported)
- DRAM address multiplexing on standard address bus
- Programmable up to three wait states
- 100 nS DRAM for zero wait states at 20 MHz
- 80 nS DRAM for zero wait states at 25 MHz
- CAS before RAS refresh and refresh support during system reset

### MC68EN302 PRODUCT INFORMATION

**For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)**

- Programmable refresh period and pre-charge period
- RAS lines are separate from the four chip selects
- Refresh hidden from bus accesses
- Write protect option
- Each bank programmable size from 128Kbytes to 8Mbytes



**Figure 4. DRAM Controller**

## MC68EN302 APPLICATIONS

The MC68EN302 is intended for low-end bridge and router applications. It has the three SCCs from the MC68302, plus an additional Ethernet interface giving it a total of four serial interfaces.

Since the MC68EN302 has both the three SCCs as well as an Ethernet interface, it would be an excellent choice in an ISDN to Ethernet router.

For remote access dial-in, the MC68EN302 could be used in a dial-up modem that would connect to an Ethernet LAN.

- Low End Bridges

### MC68EN302 PRODUCT INFORMATION

**For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)**



- Industrial Control
- Remote LAN Access Points for Remote Dial-In
- PCMCIA Ethernet + WAN Cards
- Communication System Control Boards
- Intelligent Peripheral Chip to an 020/030

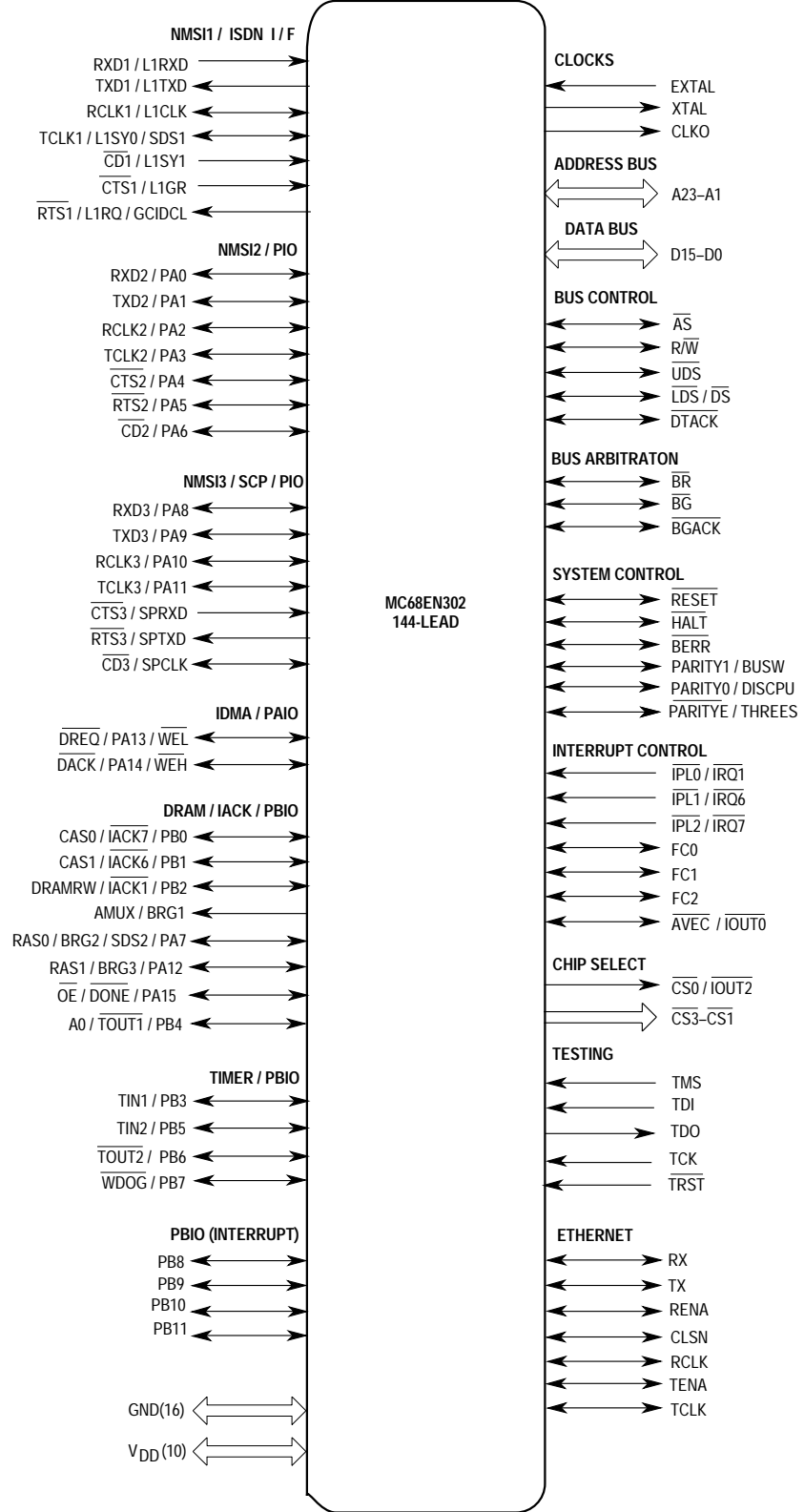
**MC68EN302 PRODUCT INFORMATION**

**For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)**



# MC68EN302 PIN DESCRIPTION

Freescale Semiconductor, Inc.



## MC68EN302 PRODUCT INFORMATION

For More Information On This Product,  
Go to: [www.freescale.com](http://www.freescale.com)

**Table 1. MC68EN302 Ordering Information**

Package Type	Operating Voltage	Frequency (MHz)	Temperature	Order Number
Thin Quad Flat Pack (PV Suffix)	5V	20	0°C to 70°C	MC68EN302PV20
Thin Quad Flat Pack (PV Suffix)	5V	25	0°C to 70°C	MC68EN302PV25

**Table 2. Documentation**

Document Title	Order Number	Contents
MC68302 User's Manual	MC68302UM/AD	Detailed information for design
M68000 Family Programmer's Reference Manual	M68000PM/AD	M68000 Family Instruction Set
The 68K Source	BR729/D	Independent vendor listing supporting software and development tools
The MC68EN302 Addendum		Describes the differences between the MC68302 and the MC68EN302

RoHS-compliant and/or Pb-free versions of Freescale products have the functionality and electrical characteristics of their non-RoHS-compliant and/or non-Pb-free counterparts. For further information, see <http://www.freescale.com> or contact your Freescale sales representative.

For information on Freescale's Environmental Products program, go to <http://www.freescale.com/epp>.

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document. Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

