# 1-Mbps QUAD DIGITAL ISOLATORS

**Check for Samples: ISO7240A, ISO7241A, ISO7242A**

## FEATURES

- **4000-$V_{peak}$ Isolation, 560-$V_{peak}$ $V_{IORM}$**
  - **UL 1577 , IEC 60747-5-2 (VDE 0884, Rev 2), IEC 61010-1, IEC 60950-1 and CSA Approved**
- **4 kV ESD Protection**
- **Operate With 3.3-V or 5-V Supplies**
- **Typical 25-Year Life at Rated Working Voltage (See Application Note (SLLA197 ) and Figure 10)**
- **High Electromagnetic Immunity (See Application Report (SLLA181))**
- **–40°C to 125°C Operating Range**

## APPLICATIONS

- **Industrial Fieldbus**
- **Computer Peripheral Interface**
- **Servo Control Interface**
- **Data Acquisition**

## DESCRIPTION

See the Product Notification section. The ISO7240A, ISO7241A and ISO7242A are quad-channel digital isolators with multiple channel configurations and output enable functions. These devices have logic input and output buffers separated by TI's silicon dioxide ($SiO_2$) isolation barrier. Used in conjunction with isolated power supplies, these devices block high voltage, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

The ISO7240A has all four channels in the same direction while the ISO7241A has three channels the same direction and one channel in opposition. The ISO7242A has two channels in each direction.

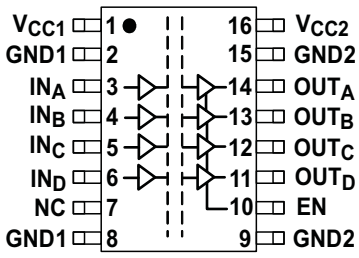
The devices have TTL input thresholds and a noise-filter at the input that prevents transient pulses from being passed to the output of the device.

A periodic update pulse is sent across the barrier to ensure the proper dc level of the output. If this dc-refresh pulse is not received, the input is assumed to be unpowered or not being actively driven, and the failsafe circuit drives the output to a logic high state. (See ISO7240CF (SLLS869) or contact TI for a logic low failsafe option).

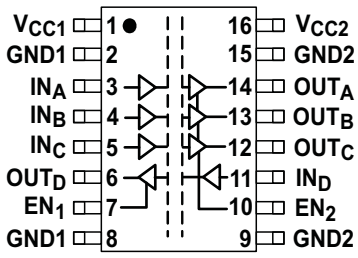
These devices may be powered from either 3.3-V or 5-V supplies on either side in any 3.3-V / 3.3-V, 5-V / 5-V, 5-V / 3.3-V, or 3.3-V / 5-V combination. Note that the signal input pins are 5-V tolerant regardless of the voltage supply level being used.

These devices are characterized for operation over the ambient temperature range of –40°C to 125°C.

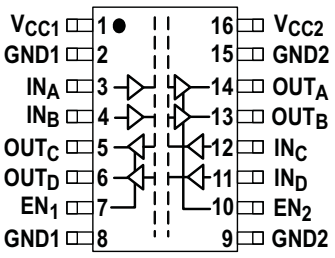
**ISO7240A**




**ISO7241A**




**ISO7242A**



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## FUNCTION DIAGRAM

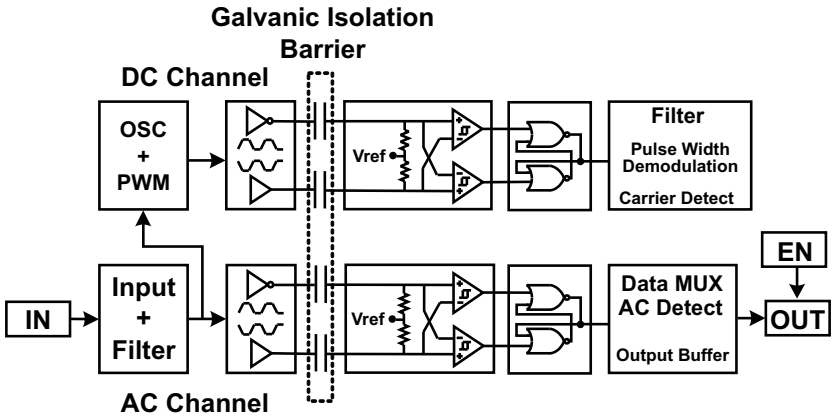



**Table 1. Device Function Table ISO724x (1)**

| INPUT $V_{CC}$ | OUTPUT $V_{CC}$ | INPUT (IN) | OUTPUT ENABLE (EN) | OUTPUT (OUT) |
|---|---|---|---|---|
| PU | PU | H | H or Open | H |
| | | L | H or Open | L |
| | | X | L | Z |
| | | Open | H or Open | H |
| PD | PU | X | H or Open | H |
| PD | PU | X | L | Z |

(1) PU = Powered Up; PD = Powered Down ; X = Irrelevant; H = High Level; L = Low Level

## AVAILABLE OPTIONS

| PRODUCT | SIGNALING RATE | INPUT THRESHOLD | CHANNEL CONFIGURATION | MARKED AS | ORDERING NUMBER(1) |
|---|---|---|---|---|---|
| ISO7240ADW | 1 Mbps | ~1.5 V (TTL) (CMOS compatible) | 4/0 | ISO7240A | ISO7240ADW (rail) |
| | | | | | ISO7240ADWR (reel) |
| ISO7241ADW | 1 Mbps | ~1.5 V (TTL) (CMOS compatible) | 3/1 | ISO7241A | ISO7241ADW (rail) |
| | | | | | ISO7241ADWR (reel) |
| ISO7242ADW | 1 Mbps | ~1.5 V (TTL) (CMOS compatible) | 2/2 | ISO7242A | ISO7242ADW (rail) |
| | | | | | ISO7242ADWR (reel) |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

| | | | | | VALUE | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage(2), $V_{CC1}$, $V_{CC2}$ | | | | –0.5 to 6 | V |
| $V_I$ | Voltage at IN, OUT, EN | | | | –0.5 to 6 | V |
| $I_O$ | Output current | | | | ±15 | mA |
| ESD | Electrostatic discharge | Human Body Model | JEDEC Standard 22, Test Method A114-C.01 | All pins | ±4 | kV |
| | | Field-Induced-Charged Device Model | JEDEC Standard 22, Test Method C101 | | ±1 | |
| | | Machine Model | ANSI/ESDS5.2-1996 | | ±200 | V |
| $T_J$ | Maximum junction temperature | | | | 170 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal and are peak voltage values.

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage(1), $V_{CC1}$, $V_{CC2}$ | | 3.15 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | | 4 | mA |
| $I_{OL}$ | Low-level output current | | –4 | | | mA |
| $t_{ui}$ | Input pulse width | ISO724xA | 1 | | | µs |
| $1/t_{ui}$ | Signaling rate | ISO724xA | 0 | | 1000 | kbps |
| $V_{IH}$ | High-level input voltage (IN) (EN on all devices) | ISO724xA | 2 | | $V_{CC}$ | V |
| $V_{IL}$ | Low-level input voltage (IN) (EN on all devices) | | 0 | | 0.8 | V |
| $T_J$ | Junction temperature | | | | 150 | °C |
| H | External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification | | | | 1000 | A/m |

(1) For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V.
For the 3-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 3.15 V to 3.6 V.

## IEC 60747-5-2 INSULATION CHARACTERISTICS(1)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | SPECIFICATIONS | UNIT |
|---|---|---|---|---|
| $V_{IORM}$ | Maximum working insulation voltage | | 560 | V |
| $V_{PR}$ | Input to output test voltage | After Input/Output Safety Test Subgroup 2/3<br>$V_{PR} = V_{IORM} \times 1.2$, t = 10 s,<br>Partial discharge < 5 pC | 672 | V |
| | | Method a, $V_{PR} = V_{IORM} \times 1.6$,<br>Type and sample test with t = 10 s,<br>Partial discharge < 5 pC | 896 | V |
| | | Method b1, $V_{PR} = V_{IORM} \times 1.875$,<br>100 % Production test with t = 1 s,<br>Partial discharge < 5 pC | 1050 | V |
| $V_{IOTM}$ | Transient overvoltage | t = 60 s | 4000 | V |
| $R_S$ | Insulation resistance | $V_{IO}$ = 500 V at $T_S$ | $>10^9$ | Ω |
| | Pollution degree | | 2 | |

(1) Climatic Classification 40/125/21

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 5-V[1] OPERATION

, over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | |
| $I_{CC1}$ | ISO7240A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | 1 | 3 | mA |
| | | 1 Mbps | | | 1 | 3 | |
| | ISO7241A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 6.5 | 11 | mA |
| | | 1 Mbps | | | | | |
| | ISO7242A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 10 | 16 | mA |
| | | 1 Mbps | | | 10 | 16 | |
| $I_{CC2}$ | ISO7240A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | 15 | 22 | mA |
| | | 1 Mbps | | | 16 | 22 | |
| | ISO7241A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 13 | 20 | mA |
| | | 1 Mbps | | | 13 | 20 | |
| | ISO7242A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 10 | 16 | mA |
| | | 1 Mbps | | | 10 | 16 | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | | EN at 0 V, Single channel | | 0 | | μA |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –4 mA, See Figure 1 | $V_{CC}$ – 0.8 | | | V |
| | | | $I_{OH}$ = –20 μA, See Figure 1 | $V_{CC}$ – 0.1 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4 mA, See Figure 1 | | | 0.4 | V |
| | | | $I_{OL}$ = 20 μA, See Figure 1 | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | | IN from 0 V to $V_{CC}$ | | | 10 | μA |
| $I_{IL}$ | Low-level input current | | | –10 | | | |
| $C_I$ | Input capacitance to ground | | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | 2 | | pF |
| CMTI | Common-mode transient immunity | | $V_I$ = $V_{CC}$ or 0 V, See Figure 4 | 25 | 50 | | kV/μs |

(1) For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V.
For the 3-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 3.15 V to 3.6 V.

## SWITCHING CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | See Figure 1 | 40 | | 95 | ns |
| PWD | Pulse-width distortion[1] $\lvert t_{PHL} - t_{PLH} \rvert$ | | | | 10 | |
| $t_{sk(o)}$ | Channel-to-channel output skew [2] | | | | 2 | ns |
| $t_r$ | Output signal rise time | See Figure 1 | | 2 | | ns |
| $t_f$ | Output signal fall time | | | 2 | | |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | | 15 | 20 | |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | | 15 | 20 | |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | | 15 | 20 | |
| $t_{fs}$ | Failsafe output delay time from input power loss | See Figure 3 | | 12 | | μs |

(1) Also referred to as pulse skew.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | | |
| $I_{CC1}$ | ISO7240A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | | 1 | 3 | mA |
| | | 1 Mbps | | | | 1 | 3 | |
| | ISO7241A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | 6.5 | 11 | mA |
| | | 1 Mbps | | | | | | |
| | ISO7242A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | 10 | 16 | mA |
| | | 1 Mbps | | | | 10 | 16 | |
| $I_{CC2}$ | ISO7240A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | | 9.5 | 15 | mA |
| | | 1 Mbps | | | | 10 | 15 | |
| | ISO7241A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | 8 | 13 | mA |
| | | 1 Mbps | | | | 8 | 13 | |
| | ISO7242A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | 6 | 10 | mA |
| | | 1 Mbps | | | | 6 | 10 | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | | EN at 0 V, Single channel | | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –4 mA, See Figure 1 | ISO7240A | $V_{CC}$ – 0.4 | | | V |
| | | | | ISO724x (5-V side) | $V_{CC}$ – 0.8 | | | |
| | | | $I_{OH}$ = –20 µA, See Figure 1 | | $V_{CC}$ – 0.1 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4 mA, See Figure 1 | | | | 0.4 | V |
| | | | $I_{OL}$ = 20 µA, See Figure 1 | | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | | IN from 0 V to $V_{CC}$ | | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | | –10 | | | |
| $C_I$ | Input capacitance to ground | | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | | 2 | | pF |
| CMTI | Common-mode transient immunity | | $V_I$ = $V_{CC}$ or 0 V, See Figure 4 | | 25 | 50 | | kV/µs |

(1) For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V.
For the 3-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 3.15 V to 3.6 V.

## SWITCHING CHARACTERISTICS: $V_{CC1}$ at 5-V, $V_{CC2}$ at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | See Figure 1 | 40 | | 100 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | | | | 11 | |
| $t_{sk(o)}$ | Channel-to-channel output skew (2) | | | | 3 | ns |
| | | | | 0 | 1 | |
| $t_r$ | Output signal rise time | See Figure 1 | | 2 | | ns |
| $t_f$ | Output signal fall time | | | 2 | | |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | | 15 | 20 | |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | | 15 | 20 | |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | | 15 | 20 | |
| $t_{fs}$ | Failsafe output delay time from input power loss | See Figure 3 | | 18 | | µs |

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ at 3.3-V, $V_{CC2}$ at 5-V(1) OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | | |
| $I_{CC1}$ | ISO7240A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | | 0.5 | 1 | mA |
| | | 1 Mbps | | | | 1 | 2 | |
| | ISO7241A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | 4 | 7 | mA |
| | | 1 Mbps | | | | 4 | 7 | |
| | ISO7242A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | 6 | 10 | mA |
| | | 1 Mbps | | | | 6 | 10 | |
| $I_{CC2}$ | ISO7240A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_2$ at 3 V | | | 15 | 22 | mA |
| | | 1 Mbps | | | | 16 | 22 | |
| | ISO7241A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | 13 | 20 | mA |
| | | 1 Mbps | | | | 13 | 20 | |
| | ISO7242A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, All channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | | 10 | 16 | mA |
| | | 1 Mbps | | | | 10 | 16 | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | | EN at $V_{CC}$, Single channel | | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –4 mA, See Figure 1 | ISO7240A | $V_{CC}$ – 0.4 | | | V |
| | | | | ISO724x (5-V side) | $V_{CC}$ – 0.8 | | | |
| | | | $I_{OH}$ = –20 µA, See Figure 1 | | $V_{CC}$ – 0.1 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4 mA, See Figure 1 | | | | 0.4 | V |
| | | | $I_{OL}$ = 20 µA, See Figure 1 | | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | | IN from 0 V to $V_{CC}$ | | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | | –10 | | | |
| $C_I$ | Input capacitance to ground | | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | | 2 | | pF |
| CMTI | Common-mode transient immunity | | $V_I$ = $V_{CC}$ or 0 V, See Figure 4 | | 25 | 50 | | kV/µs |

(1) For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V.
For the 3-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 3.15 V to 3.6 V.

## SWITCHING CHARACTERISTICS: $V_{CC1}$ at 3.3-V and $V_{CC2}$ at 5-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | See Figure 1 | 40 | | 100 | ns |
| PWD | Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$ | | | | 11 | |
| $t_{sk(o)}$ | Channel-to-channel output skew (2) | | | | 2.5 | ns |
| | | | | 0 | 1 | |
| $t_r$ | Output signal rise time | See Figure 1 | | 2 | | ns |
| $t_f$ | Output signal fall time | | | 2 | | |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | | 15 | 20 | |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | | 15 | 20 | |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | | 15 | 20 | |
| $t_{fs}$ | Failsafe output delay time from input power loss | See Figure 3 | | 12 | | µs |

(1) Also known as pulse skew
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

## ELECTRICAL CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 3.3 V[1] OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | |
| $I_{CC1}$ | ISO7240A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_2$ at 3 V | | 0.5 | 1 | mA |
| | | 1 Mbps | | | 1 | 2 | |
| | ISO7241A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 4 | 7 | mA |
| | | 1 Mbps | | | 4 | 7 | |
| | ISO7242A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 6 | 10 | |
| | | 1 Mbps | | | 6 | 10 | |
| $I_{CC2}$ | ISO7240A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_2$ at 3 V | | 9.5 | 15 | mA |
| | | 1 Mbps | | | 10 | 15 | |
| | ISO7241A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 8 | 13 | mA |
| | | 1 Mbps | | | 8 | 13 | |
| | ISO7242A | Quiescent | $V_I$ = $V_{CC}$ or 0 V, all channels, no load, $EN_1$ at 3 V, $EN_2$ at 3 V | | 6 | 10 | |
| | | 1 Mbps | | | 6 | 10 | |
| **ELECTRICAL CHARACTERISTICS** | | | | | | | |
| $I_{OFF}$ | Sleep mode output current | | EN at 0 V, single channel | | 0 | | µA |
| $V_{OH}$ | High-level output voltage | | $I_{OH}$ = –4 mA, See Figure 1 | $V_{CC}$ – 0.4 | | | V |
| | | | $I_{OH}$ = –20 µA, See Figure 1 | $V_{CC}$ – 0.1 | | | |
| $V_{OL}$ | Low-level output voltage | | $I_{OL}$ = 4 mA, See Figure 1 | | | 0.4 | V |
| | | | $I_{OL}$ = 20 µA, See Figure 1 | | | 0.1 | |
| $V_{I(HYS)}$ | Input voltage hysteresis | | | | 150 | | mV |
| $I_{IH}$ | High-level input current | | IN from 0 V or $V_{CC}$ | | | 10 | µA |
| $I_{IL}$ | Low-level input current | | | –10 | | | |
| $C_I$ | Input capacitance to ground | | IN at $V_{CC}$, $V_I$ = 0.4 sin (4E6πt) | | 2 | | pF |
| CMTI | Common-mode transient immunity | | $V_I$ = $V_{CC}$ or 0 V, See Figure 4 | 25 | 50 | | kV/µs |

(1) For the 5-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 4.5 V to 5.5 V.
For the 3-V operation, $V_{CC1}$ or $V_{CC2}$ is specified from 3.15 V to 3.6 V.

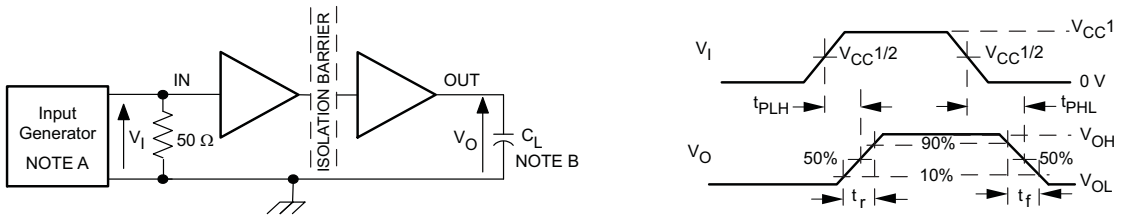
## SWITCHING CHARACTERISTICS: $V_{CC1}$ and $V_{CC2}$ at 3.3-V OPERATION

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay | See Figure 1 | 45 | | 110 | ns |
| PWD | Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ [1] | | | | 12 | |
| $t_{sk(o)}$ | Channel-to-channel output skew [2] | | | | 3.5 | ns |
| | | | | 0 | 1 | |
| $t_r$ | Output signal rise time | See Figure 1 | | 2 | | |
| $t_f$ | Output signal fall time | | | 2 | | |
| $t_{PHZ}$ | Propagation delay, high-level-to-high-impedance output | See Figure 2 | | 15 | 20 | ns |
| $t_{PZH}$ | Propagation delay, high-impedance-to-high-level output | | | 15 | 20 | |
| $t_{PLZ}$ | Propagation delay, low-level-to-high-impedance output | | | 15 | 20 | |
| $t_{PZL}$ | Propagation delay, high-impedance-to-low-level output | | | 15 | 20 | |
| $t_{fs}$ | Failsafe output delay time from input power loss | See Figure 3 | | 18 | | µs |

(1) Also referred to as pulse skew.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

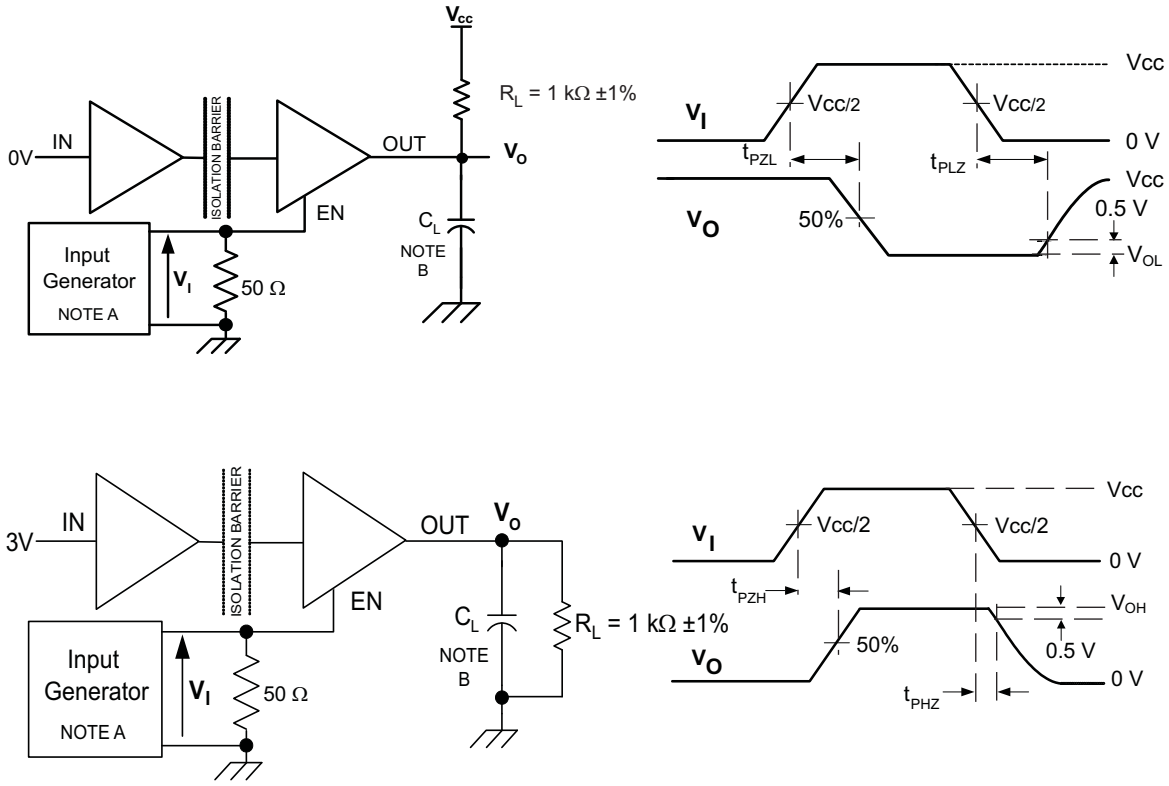
## PARAMETER MEASUREMENT INFORMATION




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms**

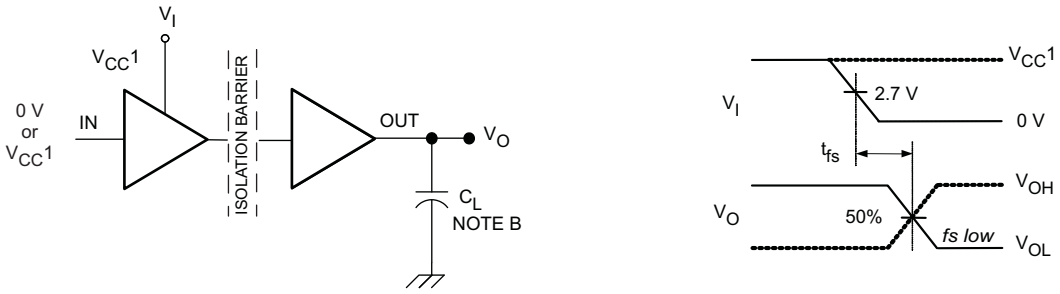



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

B. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

**Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform**

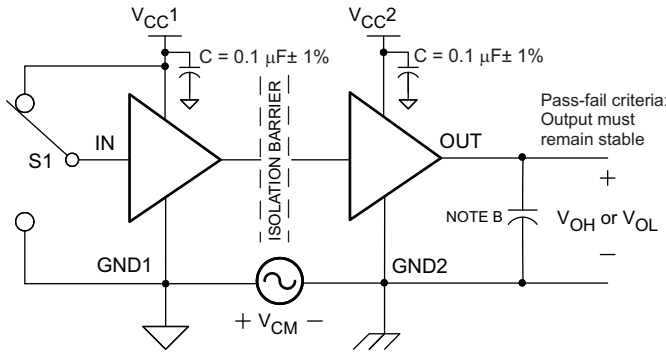
## PARAMETER MEASUREMENT INFORMATION (continued)




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

**Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms**




A. $C_L$ = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns, $Z_O$ = 50Ω.

**Figure 4. Common-Mode Transient Immunity Test Circuit and Voltage Waveform**

# DEVICE INFORMATION

## PACKAGE CHARACTERISTICS

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| L(I01) | Minimum air gap (Clearance) | Shortest terminal-to-terminal distance through air | 8.34 | | | mm |
| L(I02) | Minimum external tracking (Creepage) | Shortest terminal-to-terminal distance across the package surface | 8.1 | | | mm |
| $C_{TI}$ | Tracking resistance (comparative tracking index) | DIN IEC 60112/VDE 0303 Part 1 | ≥ 175 | | | V |
| | Minimum Internal Gap (Internal Clearance) | Distance through the insulation | 0.008 | | | mm |
| $R_{IO}$ | Isolation resistance | Input to output, $V_{IO}$ = 500 V, all pins on each side of the barrier tied together creating a two-terminal device | | $>10^{12}$ | | Ω |
| $C_{IO}$ | Barrier capacitance Input to output | $V_I$ = 0.4 sin (4E6πt) | | 2 | | pF |
| $C_I$ | Input capacitance to ground | $V_I$ = 0.4 sin (4E6πt) | | 2 | | pF |

## IEC 60664-1 RATINGS TABLE

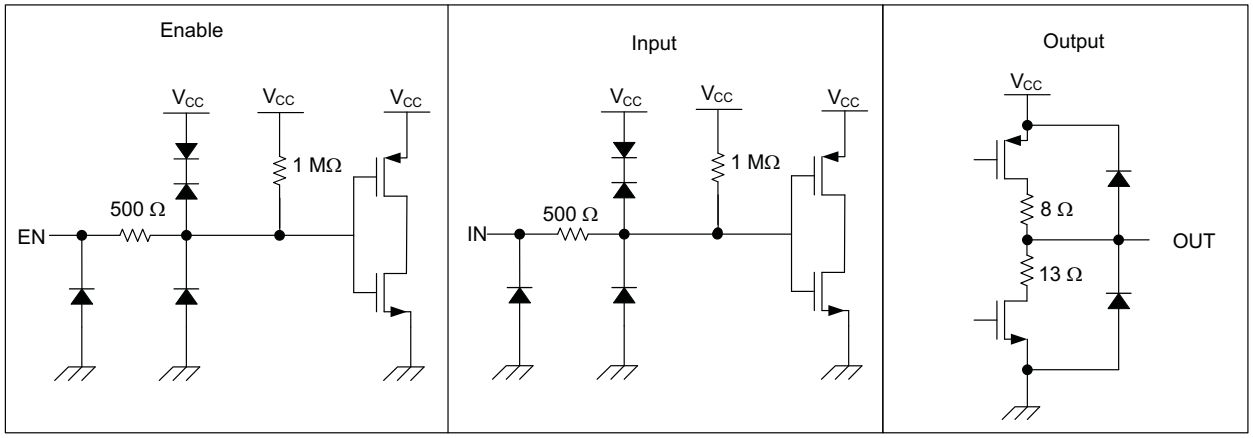
| PARAMETER | TEST CONDITIONS | SPECIFICATION |
|---|---|---|
| Basic isolation group | Material group | IIIa |
| Installation classification | Rated mains voltage ≤150 VRMS | I-IV |
| | Rated mains voltage ≤300 VRMS | I-III |

## REGULATORY INFORMATION

| VDE | CSA | UL |
|---|---|---|
| Certified according to IEC 60747-5-2 | Approved under CSA Component Acceptance Notice | Recognized under 1577 Component Recognition Program(1) |
| File Number: 40016131 | File Number: 1698195 | File Number: E181974 |

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

## DEVICE I/O SCHEMATICS



## THERMAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction-to-air | Low-K Thermal Resistance(1) | | 168 | | °C/W |
| | | High-K Thermal Resistance | | 96.1 | | |
| $\theta_{JB}$ | Junction-to-Board Thermal Resistance | | | 61 | | °C/W |
| $\theta_{JC}$ | Junction-to-Case Thermal Resistance | | | 48 | | °C/W |
| $P_D$ | Device Power Dissipation | $V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150°C$, $C_L = 15$ pF, Input a 50% duty cycle square wave | | | 220 | mW |

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

## TYPICAL CHARACTERISTIC CURVES

**INPUT VOLTAGE THRESHOLD vs FREE-AIR TEMPERATURE**

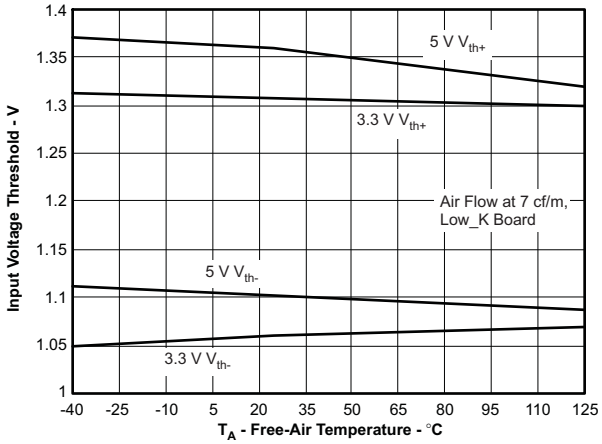



Figure 5.

**$V_{CC1}$ FAILSAFE THRESHOLD vs FREE-AIR TEMPERATURE**

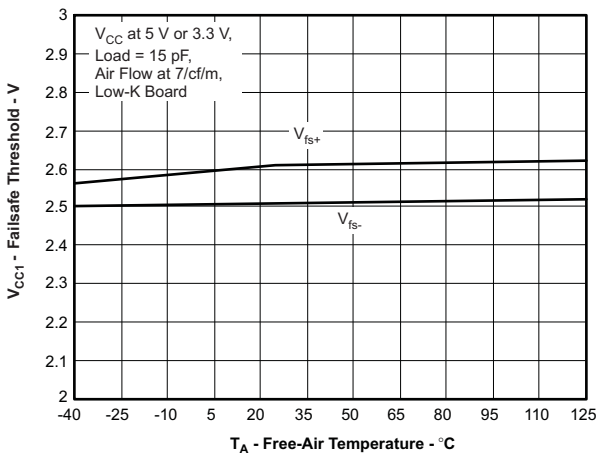



Figure 6.

**HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

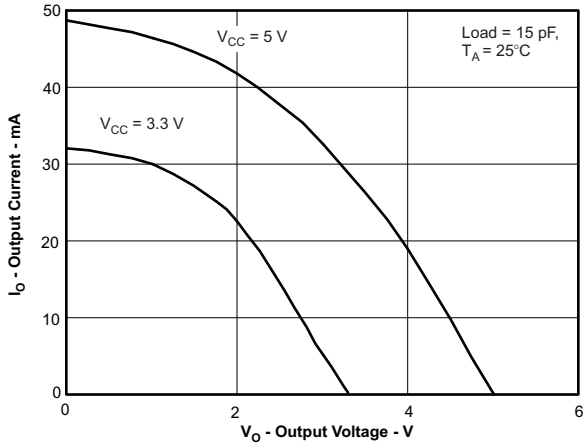



Figure 7.

**LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE**

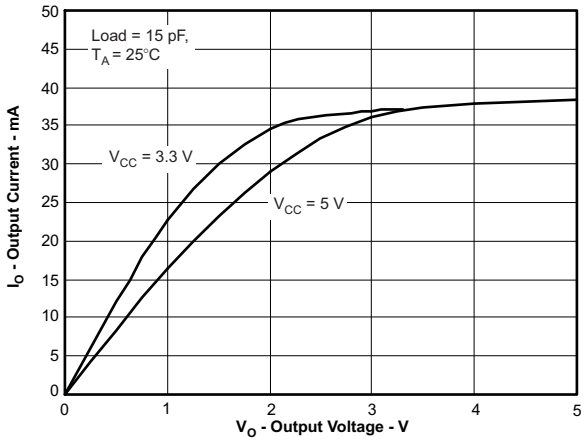



Figure 8.

## APPLICATION INFORMATION

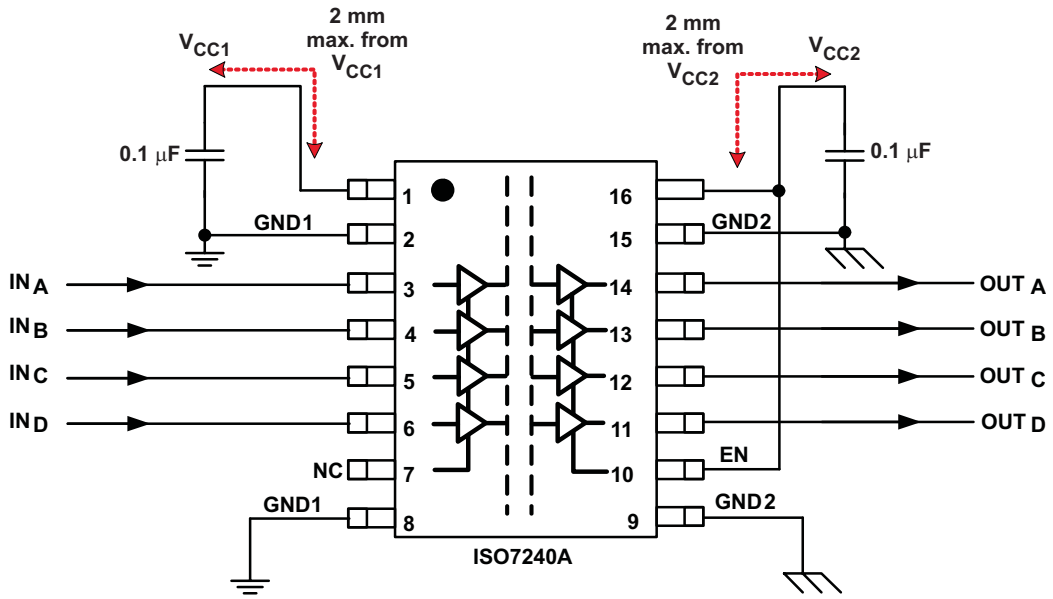



**Figure 9. Typical ISO7240A Application Circuit**

## LIFE EXPECTANCY vs. WORKING VOLTAGE

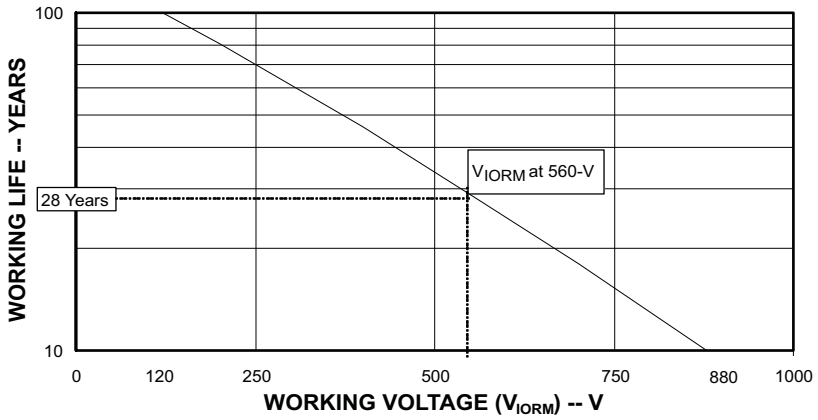



**Figure 10. Time-Dependant Dielectric Breakdown Testing Results**

## PRODUCT NOTIFICATION

An ISO724xA anomaly occurs when a negative-going pulse below the specified 1 μs minimum bit width is input to the device. The output locks in a logic-low condition until the next rising edge occurs after a 1 μs period.

Positive noise edges in pulses of less than the minimum specified 1 μs have no effect on the device, and are properly filtered.

To prevent noise from interfering with ISO724xA performance, it is recommended that an appropriately sized capacitor be placed on each input of the device

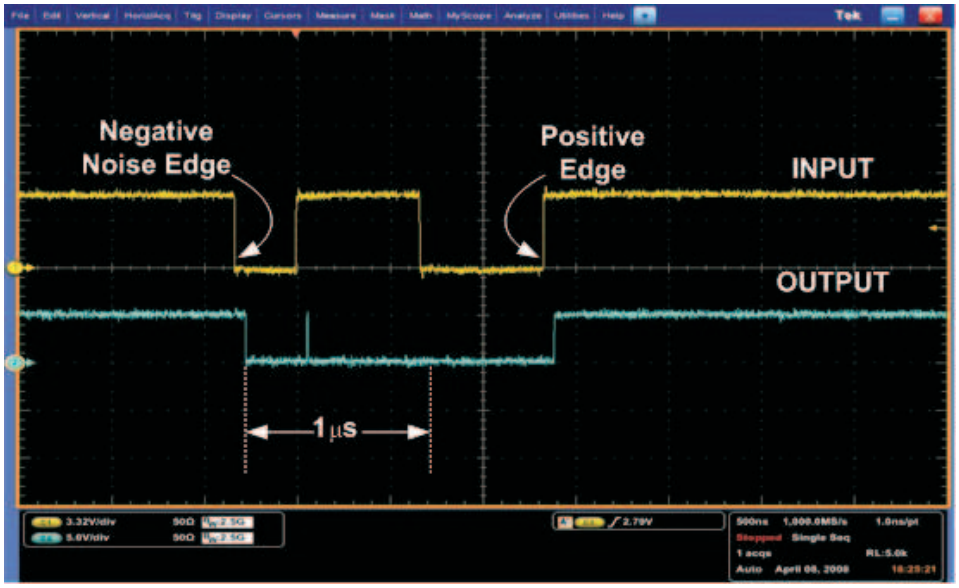



**Figure 11. ISO724xA Anomaly**

## REVISION HISTORY

**Changes from Original (May 2008) to Revision A** **Page**

- Changed In the PACKAGE CHARACTERISTICS table, line 1, change $L_{(IO1)}$ MIN value from 7.7mm to 8.34mm. ..... 10

**Changes from Revision A (July 2008) to Revision B** **Page**

- Added information to the 1st Feature bullet to include CSA and IEC 60950-1 certification ..... 1
- Changed Figure 9 From: 20mm max.from $V_{CCx}$ To: 2mm max. from $V_{CCx}$. ..... 12

**Changes from Revision B (December 2008) to Revision C** **Page**

- Changed $I_{CC1}$ for Quiescent and 1Mbps From: 10mA To: 11mA ..... 4
- Changed $I_{CC1}$ for Quiescent and 1Mbps From: 10mA To: 11mA ..... 5

**Changes from Revision C (March 2009) to Revision D** **Page**

- Changed The Input circuit in the DEVICE I/O SCHEMATICS illustration. ..... 10

**Changes from Revision D (December 2009) to Revision E** **Page**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7240ADW | NRND | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7240A | |
| ISO7240ADWG4 | NRND | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7240A | |
| ISO7240ADWR | NRND | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7240A | |
| ISO7241ADW | NRND | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7241A | |
| ISO7241ADWR | NRND | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7241A | |
| ISO7241ADWRG4 | NRND | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7241A | |
| ISO7242ADW | NRND | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7242A | |
| ISO7242ADWR | NRND | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | ISO7242A | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF ISO7241A :**

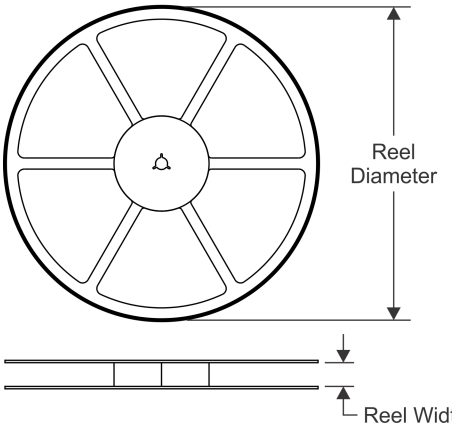
- Enhanced Product : ISO7241A-EP

NOTE: Qualified Version Definitions:

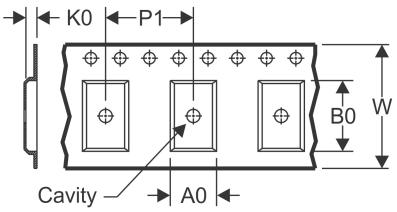
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

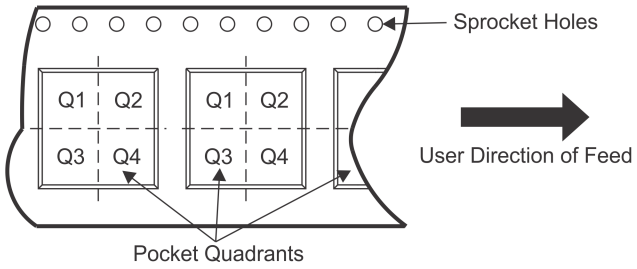



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

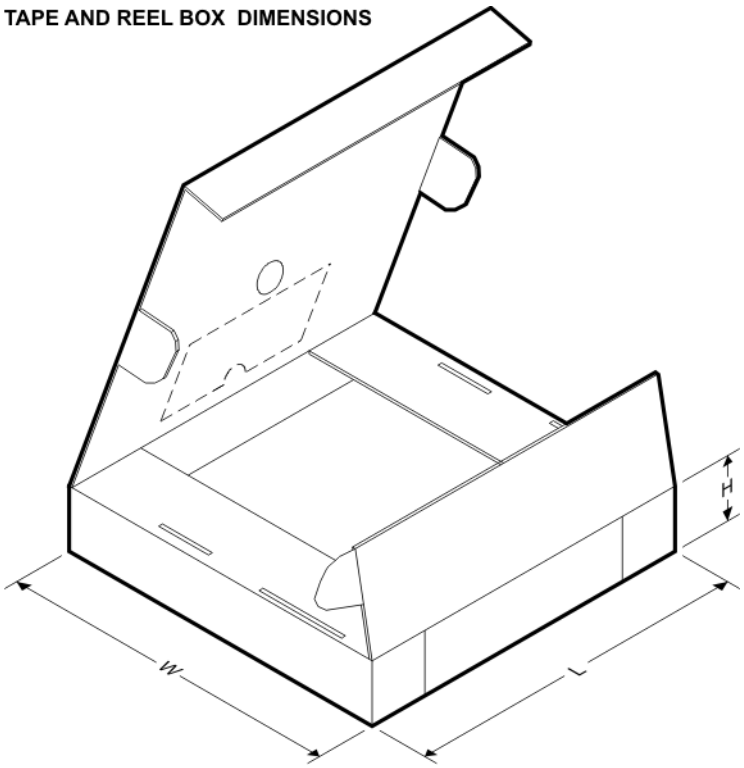
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISO7240ADWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7241ADWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| ISO7242ADWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ISO7240ADWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO7241ADWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| ISO7242ADWR | SOIC | DW | 16 | 2000 | 350.0 | 350.0 | 43.0 |

# GENERIC PACKAGE VIEW

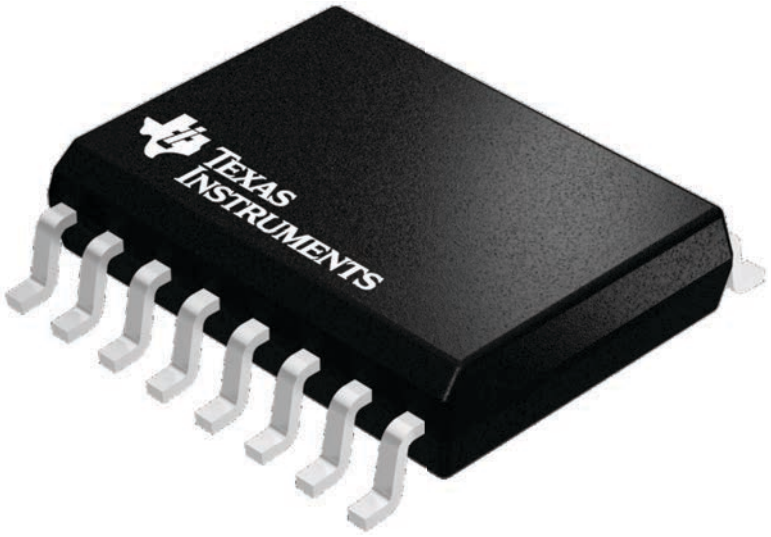
## DW 16

## SOIC - 2.65 mm max height

**7.5 x 10.3, 1.27 mm pitch**

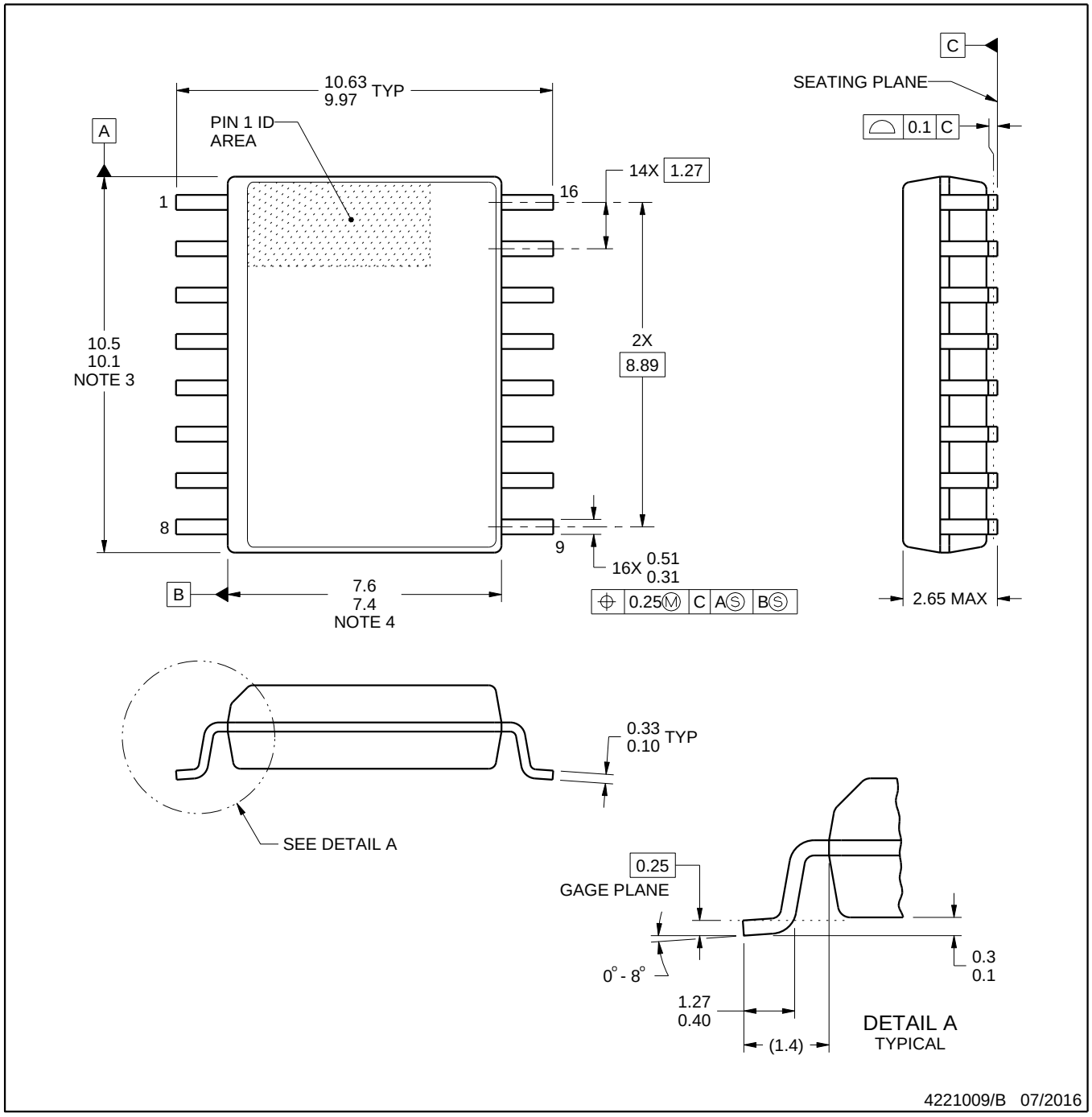
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



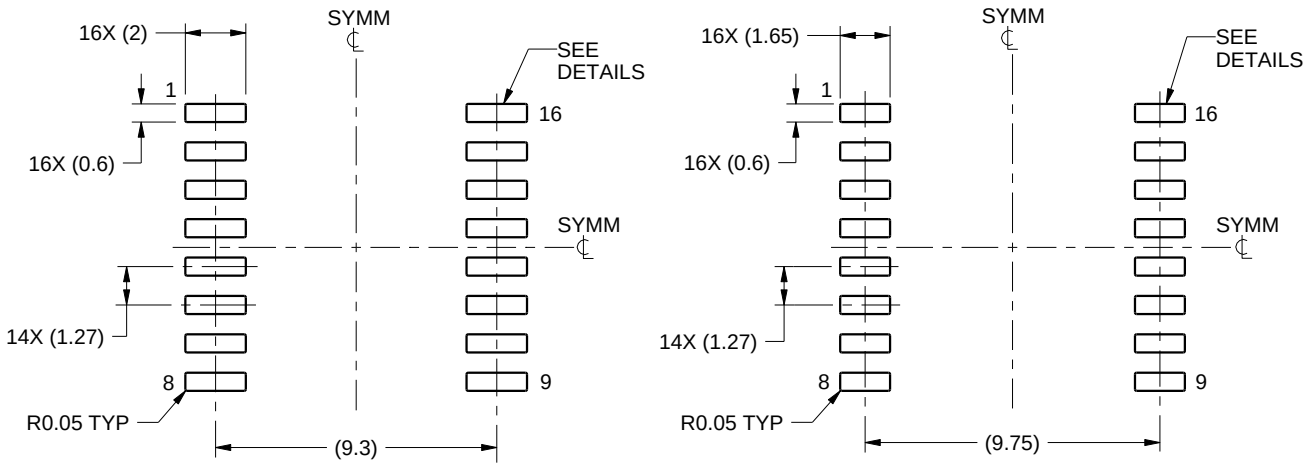

4224780/A

SOIC




NOTES:

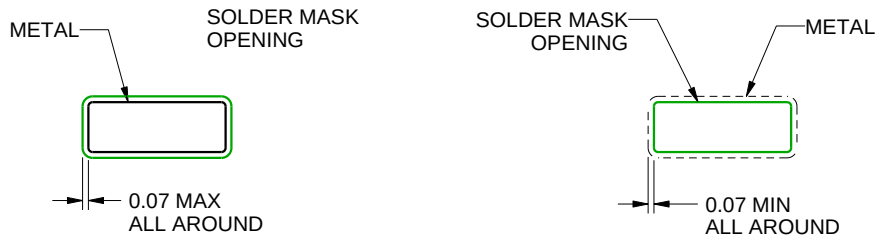
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X




NON SOLDER MASK DEFINED

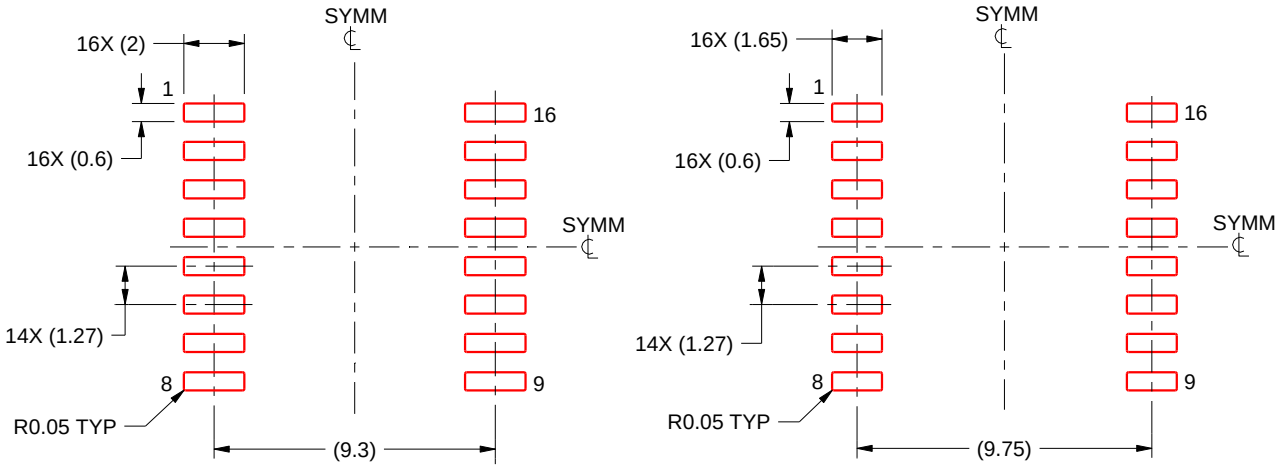
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265