8 x 4 Wideband Video Crosspoint Array

DESCRIPTION

The DG884 contains a matrix of 32 T-switches configured in an 8 x 4 crosspoint array. Any of the IN/OUT pins may be used as an input or output. Any of the IN pins may be switched to any or simultaneously to all OUT pins.

The DG884 is built on a proprietary D/CMOS process that combines low capacitance switching DMOS FETs with low power CMOS control logic and drivers. The ground lines between adjacent signal input pins help to reduce crosstalk. The low on-resistance and low on-capacitance of the DG884 make it ideal for video and wideband signal routing.

Control data is loaded individually into four Next Event latches. When all Next Event latches have been programmed, data is transferred into the Current Event latches via a SALVO command. Current Event latch data readback is available to poll array status.

Output disable capabilities make it possible to parallel multiple DG884s to form larger switch arrays. DIS outputs provide control signals used to place external buffers in a power saving mode.

For additional information see applications note AN504 (FaxBack document number 70610).

FEATURES

- Routes Any Input to Any Output
- Wide Bandwidth: 300 MHz
- Low Crosstalk: - 85 dB at 5 MHz
- Double Buffered TTL-Compatible Latches with Readback
- Low $r_{DS(on)}$: 45 Ω
- Optional Negative Supply

Pb-free Available

RoHS* COMPLIANT

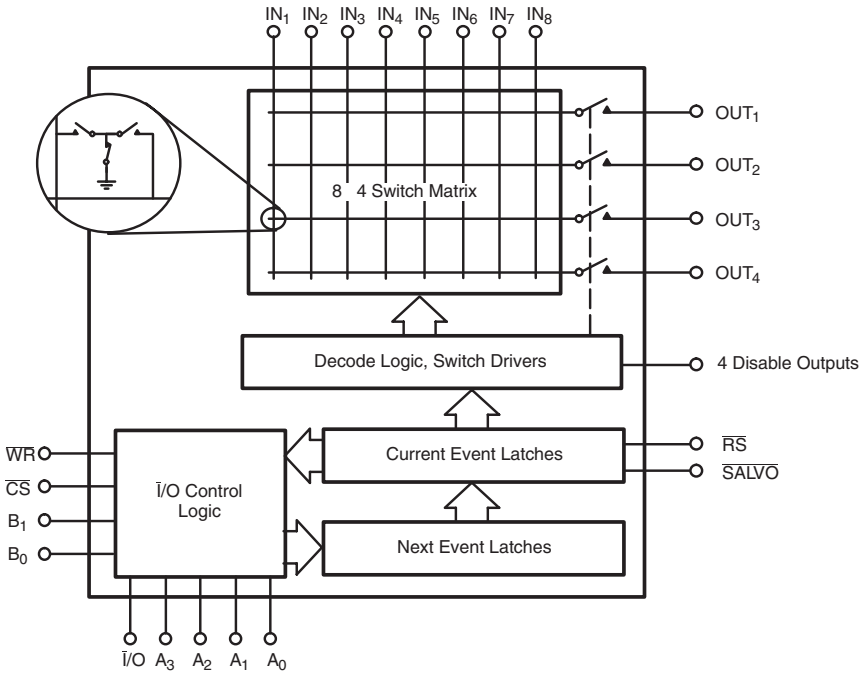
BENEFITS

- Reduced Board Space
- Improved System Bandwidth
- Improved Channel Off-Isolation
- Simplified Logic Interfacing
- Allows Bipolar Signal Swings
- Reduced Insertion Loss
- High Reliability

APPLICATIONS

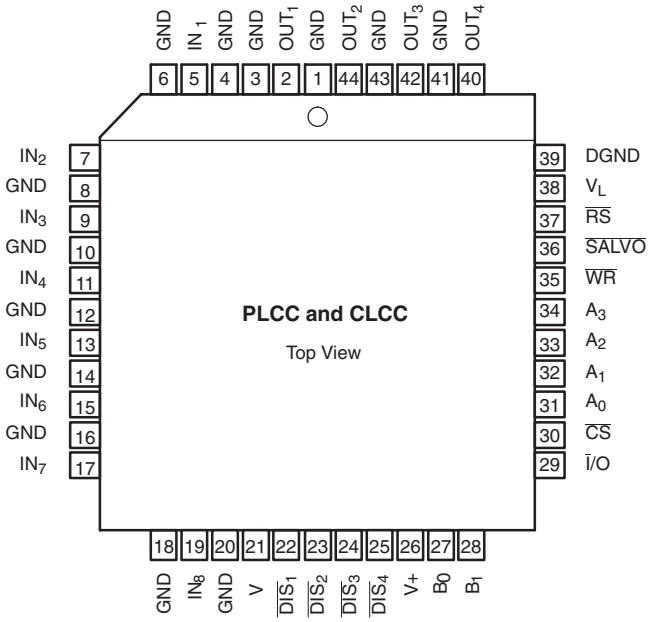
- Wideband Signal Routing and Multiplexing
- High-End Video Systems
- NTSC, PAL, SECAM Switchers
- Digital Video Routing
- ATE Systems

FUNCTIONAL BLOCK DIAGRAM



* Pb containing terminations are not RoHS compliant, exemptions may apply

PIN CONFIGURATION AND ORDERING INFORMATION



ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
- 40 to 85 °C	44-Pin PLCC	DG884DN DG884DN-E3

TRUTH TABLE I					
$\overline{RS}$	I/O	$\overline{CS}$	$\overline{WR}$	$\overline{SALVO}$	Actions
1	0	1	↓	1	No change to Next Event latches
1	0	0	↓	1	Next Event latches loaded as defined in table below
1	0	0	0	1	Next Event latches are transparent
1	0	0	↑	1	Next Event data latched-in
1	0	X	1	↓	Data in all Next Event latches is simultaneously loaded into the Current Event latches, i.e., all new crosspoint addresses change simultaneously when $\overline{SALVO}$ goes low
1	0	0	X	0	Current Event latches are transparent
1	0	X	1	↑	Current Event data latched-in
1	0	0	0	0	Both next and Current Event latches are transparent
1	1	1	1	1	A_0, A_1, A_2, A_3 - High impedance
1	1	0	1	1	A_0, A_1, A_2, A_3 become outputs and reflect the contents of the Current Event latches B_0, B_1 determine which Current Event latches are being read
0	X	X	1	1	All crosspoints opened (but data in Next Event latches is preserved)

All other states are not recommended.

TRUTH TABLE II

$\overline{WR}$	B_1	B_0	A_3	A_2	A_1	A_0	Next Event Latches
0	0	0	1	0	0	0	IN_1 to OUT_1 Loaded
				0	0	1	IN_2 to OUT_1 Loaded
				0	1	0	IN_3 to OUT_1 Loaded
				0	1	1	IN_4 to OUT_1 Loaded
				1	0	0	IN_5 to OUT_1 Loaded
				1	0	1	IN_6 to OUT_1 Loaded
				1	1	0	IN_7 to OUT_1 Loaded
				1	1	1	IN_8 to OUT_1 Loaded
			0	X	X	X	Turn Off OUT_1 Loaded
	0	1	1	0	0	0	IN_1 to OUT_2 Loaded
				0	0	1	IN_2 to OUT_2 Loaded
				0	1	0	IN_3 to OUT_2 Loaded
				0	1	1	IN_4 to OUT_2 Loaded
				1	0	0	IN_5 to OUT_2 Loaded
				1	0	1	IN_6 to OUT_2 Loaded
				1	1	0	IN_7 to OUT_2 Loaded
				1	1	1	IN_8 to OUT_2 Loaded
			0	X	X	X	Turn Off OUT_2 Loaded
	1	0	1	0	0	0	IN_1 to OUT_3 Loaded
				0	0	1	IN_2 to OUT_3 Loaded
				0	1	0	IN_3 to OUT_3 Loaded
				0	1	1	IN_4 to OUT_3 Loaded
				1	0	0	IN_5 to OUT_3 Loaded
				1	0	1	IN_6 to OUT_3 Loaded
				1	1	0	IN_7 to OUT_3 Loaded
				1	1	1	IN_8 to OUT_3 Loaded
			0	X	X	X	Turn Off OUT_3 Loaded
	1	1	1	0	0	0	IN_1 to OUT_4 Loaded
				0	0	1	IN_2 to OUT_4 Loaded
				0	1	0	IN_3 to OUT_4 Loaded
				0	1	1	IN_4 to OUT_4 Loaded
				1	0	0	IN_5 to OUT_4 Loaded
				1	0	1	IN_6 to OUT_4 Loaded
				1	1	0	IN_7 to OUT_4 Loaded
				1	1	1	IN_8 to OUT_4 Loaded
			0	X	X	X	Turn Off OUT_4 Loaded

Notes:
When $\overline{WR}$ = 0 Next Event latches are transparent. Each crosspoint is addressed individually, e.g., to connect IN_1 to OUT_1 thru OUT_4 requires A_0, A_1, A_2 = 0 to be latched with each combination of B_0, B_1. When $\overline{RS}$ = 0, all four $\overline{DIS}$ outputs pull low simultaneously.

ABSOLUTE MAXIMUM RATINGS

Parameter		Limit	Unit
V+ to GND		- 0.3 to 21	V
V+ to V-		- 0.3 to 21	
V- to GND		- 10 to 0.3	
V_L to GND		0 to (V+) + 0.3	
Digital Inputs		(V-) - 0.3 to (V_L) + 0.3 or 20 mA, whichever occurs first	
V_S, V_D		(V-) - 0.3 to (V-) + 14 or 20 mA, whichever occurs first	
Current (any terminal) Continuous		20	mA
Current (S or D) Pulsed 1 ms 10 % Duty		40	
Storage Temperature	(A Suffix)	- 65 to 150	°C
	(D Suffix)	- 65 to 125	
Operating Temperature	(A Suffix)	- 55 to 125	
	(D Suffix)	- 40 to 85	
Power Dissipation (Package)[a]	44-Pin Quad J Lead PLCC[b]	450	mW
	44-Pin Quad J Lead Hermetic CLCC[c]	1200	

Notes:
a. All leads soldered or welded to PC Board.
b. Derate 6 mW/°C above 75 °C
c. Derate 16 mW/°C above 75 °C.

SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V- = - 3 V, V_L = 5 V, $\overline{RS}$ = 2.0 V, $\overline{SALVO}$, $\overline{CS}$, $\overline{WR}$, I/O = 0.8 V	Temp[b]	Typ[c]	A Suffix - 55 to 125 °C Min[d]	A Suffix - 55 to 125 °C Max[d]	D Suffix - 40 to 85 °C Min[d]	D Suffix - 40 to 85 °C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}	V- = - 5 V	Full		- 5	8	- 5	8	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = - 10 mA, V_D = 0 V, V_{AIH} = 2.0 V, V_{AIL} = 0.8 V, Sequence Each Switch On	Room Full	45		90 120		90 120	Ω
Resistance Match Between Channels	$\Delta r_{DS(on)}$		Room	3		9		9	
Source Off Leakage Current	$I_{S(off)}$	V_S = 8 V, V_D = 0 V, $\overline{RS}$ = 0.8 V	Room Full		- 20 - 200	20 200	- 20 - 200	20 200	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = 0 V, V_S = 8 V, $\overline{RS}$ = 0.8 V	Room Full		- 20 - 200	20 200	- 20 - 200	20 200	
Total Switch On Leakage Current	$I_{D(on)}$	V_S = V_D = 8 V	Room Full		- 20 - 2000	20 2000	- 20 - 200	20 200	
Digital Input/Output									
Input Voltage High	V_{AIH}		Full		2		2		V
Input Voltage Low	V_{AIL}		Full			0.8		0.8	
Address Input Current	I_{AI}	V_{AI} = 0 V or 2 V or 5 V	Room Full	0.1	- 1 - 10	1 10	- 1 - 10	1 10	µA
Address Output Current	I_{AO}	V_{AO} = 2.7 V, See Truth Table	Room	- 600		- 200		- 200	
		V_{AO} = 0.4 V, See Truth Table	Room	1500	500		500		
DIS Pin Sink Current	I_{DIS}		Room	1.5					mA
Dynamic Characteristics									
On State Input Capacitance[e]	$C_{S(on)}$	1 In to 1 Out, See Figure 11	Room	30				40	pF
		1 In to 4 Out, See Figure 11	Room	120				160	
Off State Input Capacitance[e]	$C_{S(off)}$	See Figure 11	Room	8		20		20	
Off State Output Capacitance[e]	$C_{D(off)}$		Room	10		20		20	
Transition Time	t_{TRANS}	See Figure 5	Room					300	ns
Break-Before-Make Interval	t_{OPEN}		Full			10		10	
$\overline{SALVO}$, $\overline{WR}$ Turn On Time	t_{ON}	R_L = 1 kΩ, C_L = 35 pF, 50 % Control to 90 % Output, See Figure 3	Room Full			300 500		300	
$\overline{SALVO}$, $\overline{WR}$ Turn Off Time	t_{OFF}		Room Full			175 300		175	
Charge Injection	Q	See Figure 6	Room	- 100					pC
Matrix Disabled Crosstalk	$X_{TALK(DIS)}$	R_{IN} = R_L = 75 Ω, f = 5 MHz, See Figure 10	Room	- 82					dB
Adjacent Input Crosstalk	$X_{TALK(AI)}$	R_{IN} = 10 Ω, R_L = 10 kΩ, f = 5 MHz, See Figure 9	Room	- 85					
All Hostile Crosstalk	$X_{TALK(AH)}$	R_{IN} = 10 Ω, R_L = 10 kΩ, f = 5 MHz, See Figure 8	Room	- 66					
Bandwidth	BW	R_L = 50 Ω, See Figure 7	Room	300					MHz

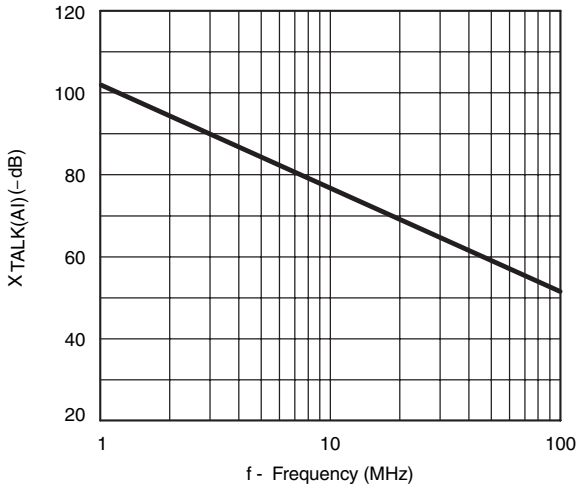
SPECIFICATIONS[a]

Parameter	Symbol	Test Conditions Unless Specified V+ = 15 V, V- = - 3 V, V_L = 5 V, $\overline{RS}$ = 2.0 V, $\overline{SALVO}$, $\overline{CS}$, $\overline{WR}$, $\overline{I}$/O = 0.8 V	Temp[b]	Typ[c]	A Suffix - 55 to 125 °C Min[d]	A Suffix - 55 to 125 °C Max[d]	D Suffix - 40 to 85 °C Min[d]	D Suffix - 40 to 85 °C Max[d]	Unit
Power Supplies									
Positive Supply Current	I+	All Inputs at GND or 2 V, $\overline{RS}$ = 2 V	Room Full	1.5		3 6		3 6	mA
Negative Supply Current	I-		Room Full	- 1.5	- 3 - 5		- 3 - 5		
Digital GND Supply Current	I_{DG}		Full	- 275	- 750		- 750		µA
Logic Supply Current	I_L		Full	200		500		500	
Functional Operating Supply Voltage Range[e]	V+ to V-	See Operating Voltage Range (Typical Characteristics) page 6	Full		13	20	13	20	V
	V- to GND		Full		- 5.5	0	- 5.5	0	
	V+ to GND		Full		10	20	10	20	
Minimum Input Timing Requirements									
Address Write Time	t_{AW}	See Figure 1	Full	20	50		50		ns
Minimum $\overline{WR}$ Pulse Width	t_{WP}		Full	50	100		100		
Write Address Time	t_{WA}		Full	- 10	10		10		
Chip Select Write Time	t_{CW}		Full	50	100		100		
Write Chip Select Time	t_{WC}		Full	25	75		75		
Minimum $\overline{SALVO}$ Pulse Width	t_{SP}		Full	50	100		100		
$\overline{SALVO}$ Write Time	t_{SW}		Full	- 10	10		10		
Write $\overline{SALVO}$Time	t_{WS}		Room	20			50		
Input Output Time	t_{IO}		Room	150	200		200		
Address Output Time	t_{AO}		Room	150	200		200		
Chip Select Output Time	t_{CO}		Room	150	200		200		
Chip Select Address Time	t_{CA}		Room	60			100		
Reset to $\overline{SALVO}$	t_{RS}		Full		50		50		
I/O Address Input Time	t_{IA}		Room	50					

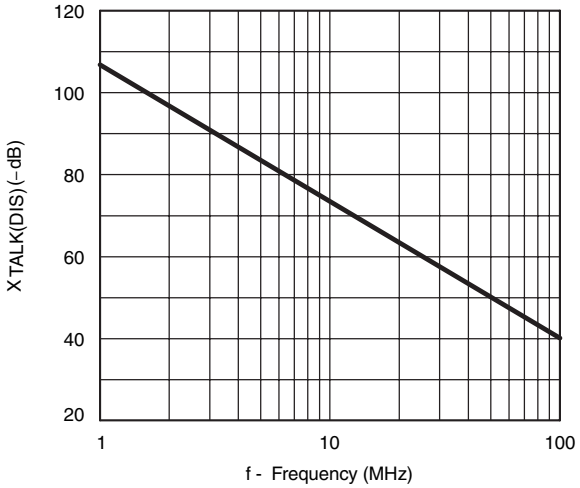
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25 °C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

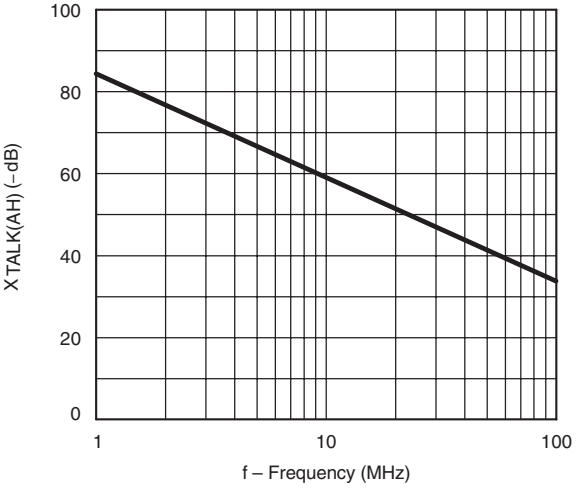
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



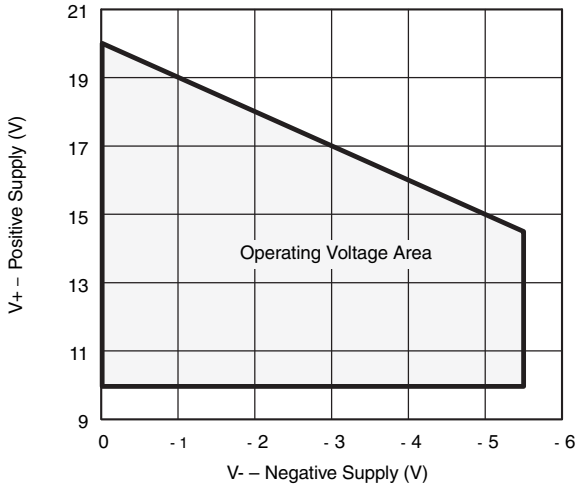
Adjacent Input Crosstalk



Matrix Disabled Crosstalk



All Hostile Crosstalk



Operating Voltage Area

TIMING DIAGRAMS

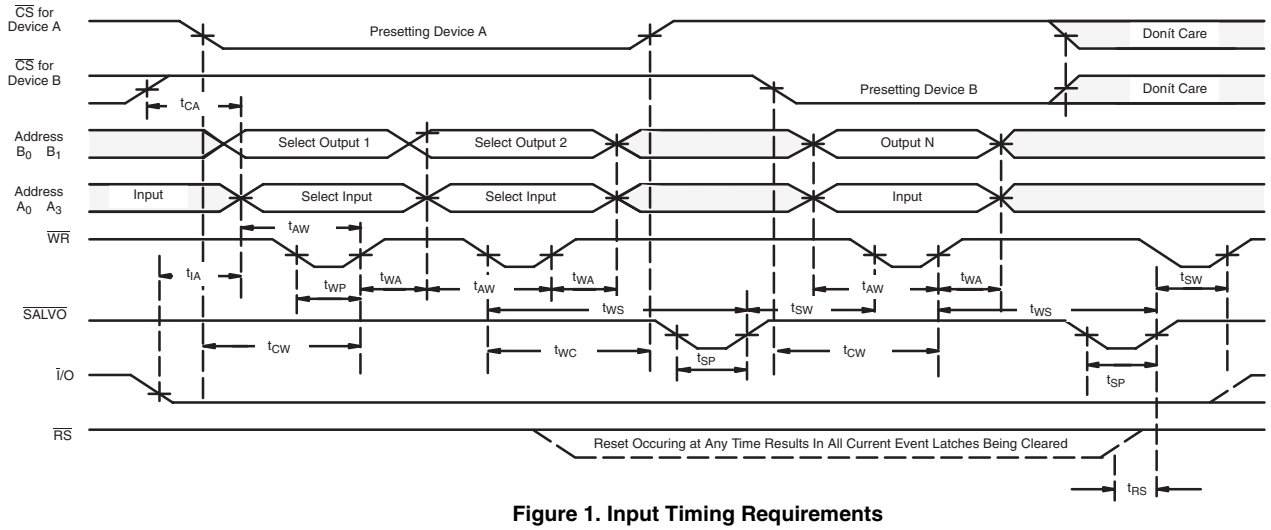


Figure 1. Input Timing Requirements

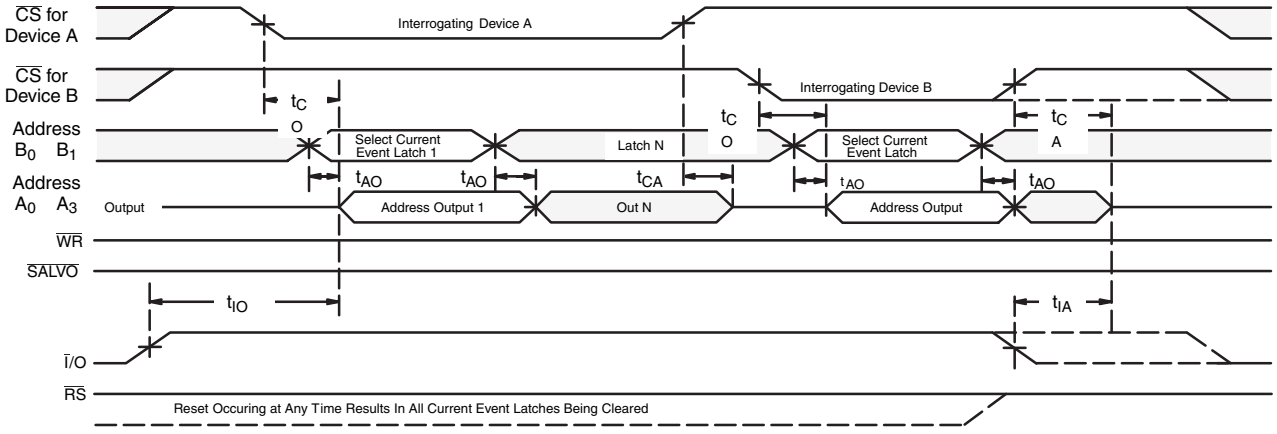


Figure 2. Output Timing Requirements

PARAMETER DEFINITIONS		
Symbol	**Parameter**	**Description**
T_{AW}	Address to Write	Minimum time address must be valid before $\overline{WR}$ goes high
T_{WA}	Write to Address	Minimum time address must remain valid after $\overline{WR}$ pulse goes high
T_{WP}	$\overline{WR}$ Pulse	Minimum time of $\overline{WR}$ pulse width to write address into Next Event latches
T_{CW}	Chip Select to $\overline{WR}$	Minimum time chip select must be valid before a $\overline{WR}$ pulse
T_{WC}	$\overline{WR}$ to Chip Select	Minimum time chip select must remain valid after $\overline{WR}$ pulse
T_{SP}	$\overline{SALVO}$ Pulse	Minimum time of $\overline{SALVO}$ pulse width
T_{WS}	$\overline{WR}$ to $\overline{SALVO}$	Minimum time from $\overline{WR}$ pulse to $\overline{SALVO}$to load new address
T_{SW}	$\overline{SALVO}$ to $\overline{WR}$	Minimum time from $\overline{SALVO}$ pulse to $\overline{WR}$ to load current address
T_{IA}	$\overline{I}$/O to Address In	Minimum time $\overline{I}$/O must be valid before address applied
T_{RS}	$\overline{RS}$ to $\overline{SALVO}$	Minimum time $\overline{RS}$ must be valid before $\overline{SALVO}$ pulse
T_{IO}	$\overline{I}$/O to Output	Minimum time $\overline{I}$/O must be valid before address output valid
T_{AO}	Address to Output	Minimum time address B_X must be valid until address A_X output valid
T_{CO}	$\overline{CS}$ to Output	Minimum time $\overline{CS}$ must be valid until A_X output is valid
T_{CA}	$\overline{CS}$ to Address In	Minimum time $\overline{CS}$ must be valid before address applied if $\overline{I}$/O is high

TEST CIRCUITS

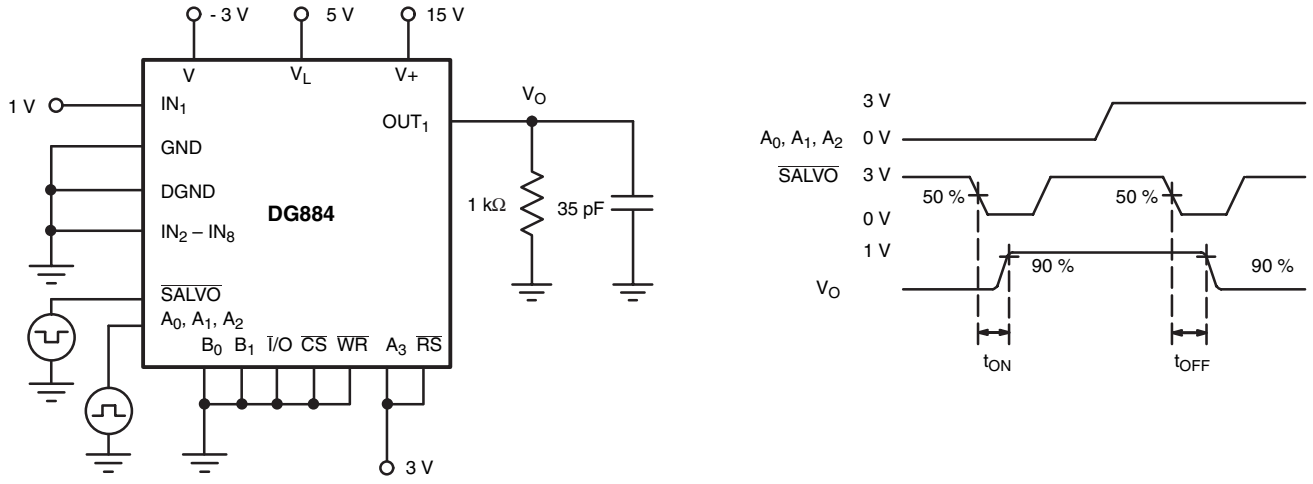


Figure 3. $\overline{\text{SALVO}}$ Turn On/Off Time

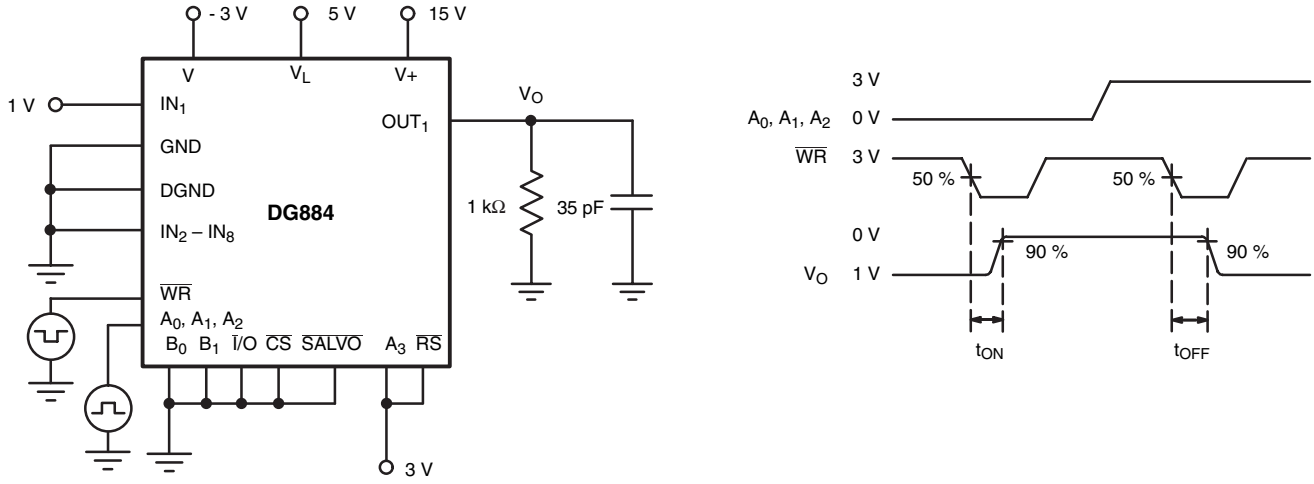


Figure 4. $\overline{\text{WR}}$ Turn On/Off Time

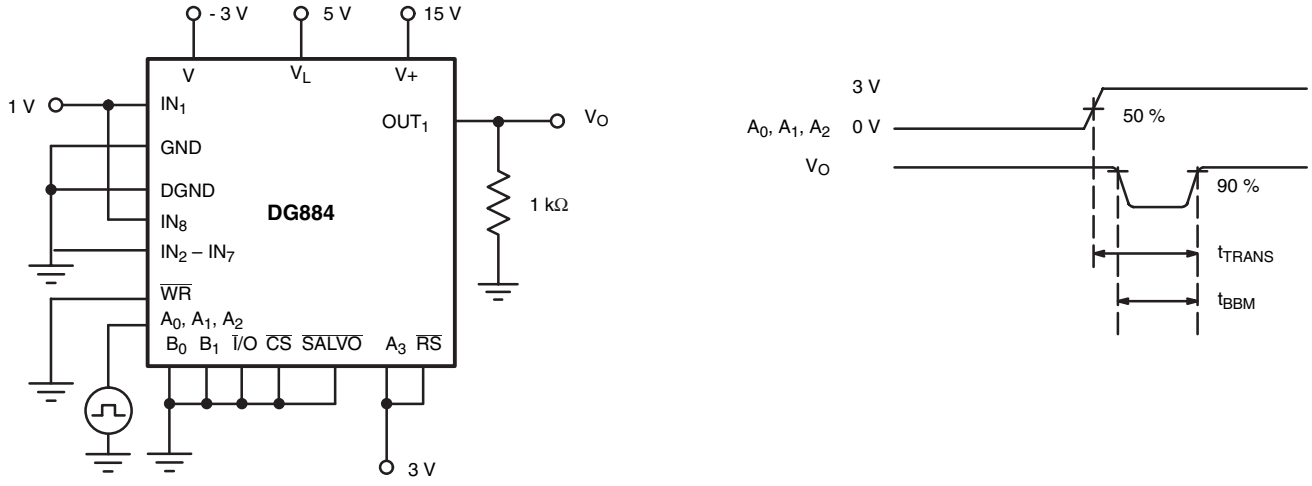


Figure 5. Transition Time and Break-Before-Make Interval

TEST CIRCUITS

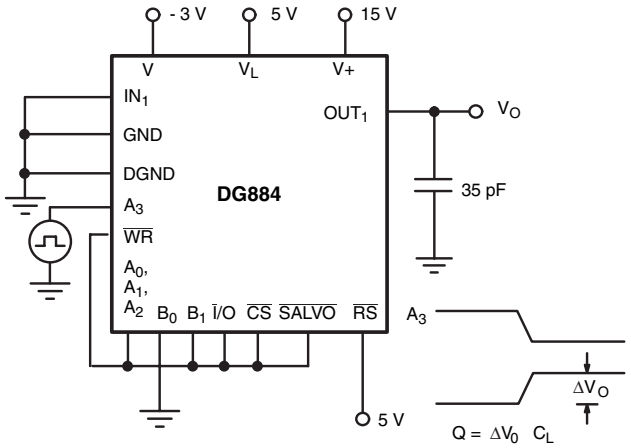


Figure 6. Charge Injection

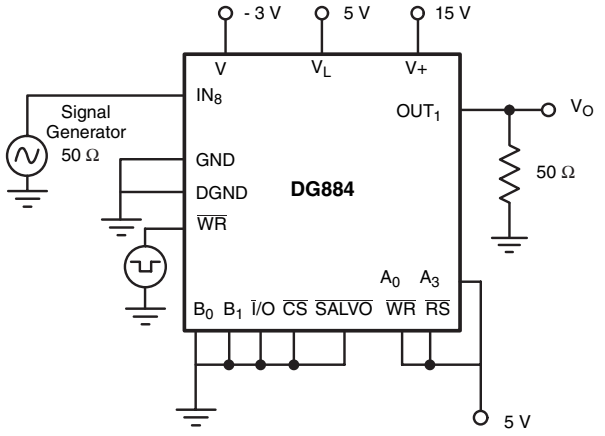


Figure 7. -3 dB Bandwidth

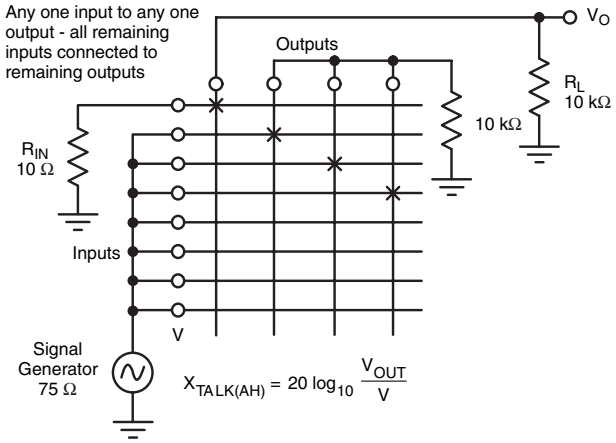


Figure 8. All Hostile Crosstalk

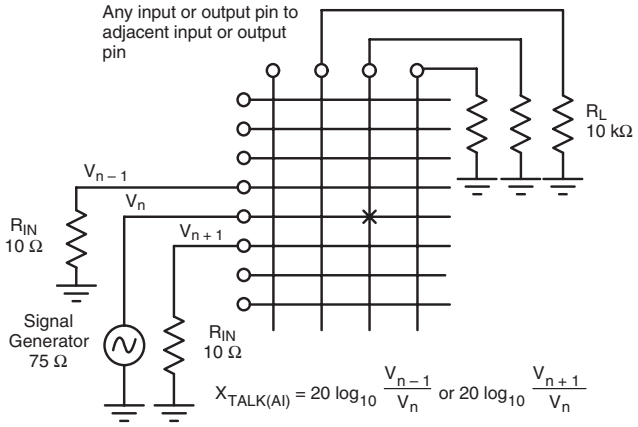


Figure 9. Adjacent Input Crosstalk

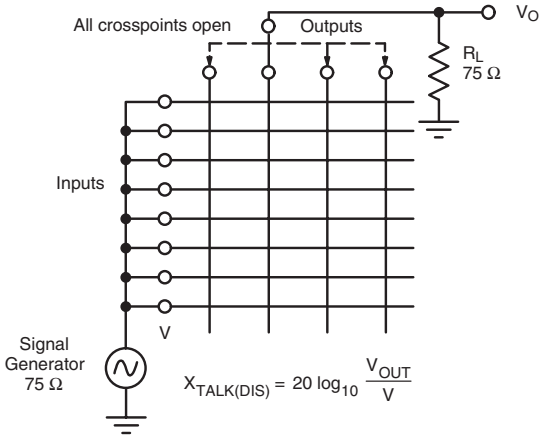


Figure 10. Matrix Disabled Crosstalk

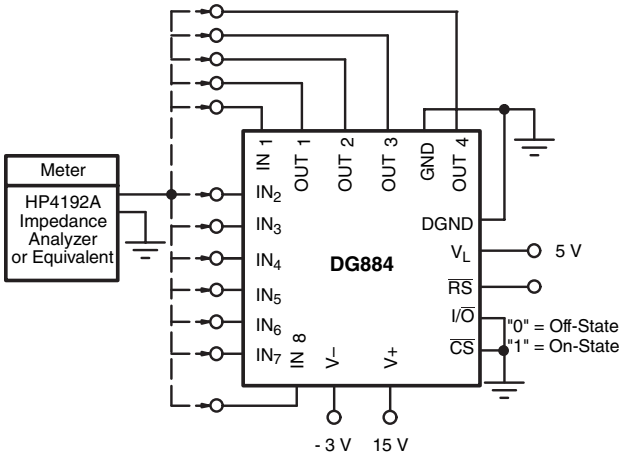


Figure 11. On-State and Off-State Capacitances

PIN DESCRIPTION		
Pin	**Symbol**	**Description**
1, 3, 4, 6, 8, 10, 12, 14, 16, 18, 20, 41, 43	GND	Analog Signal Ground
39	DGND	Digital Ground
26	V+	Positive Supply Voltage
21	V-	Negative Supply Voltage
38	V_L	Logic Supply Voltage - generally 5 V
5, 7, 9, 11, 13, 15, 17, 19	IN_1 to IN_8	8 Analog Input Channels
2, 40, 42, 44	OUT_1 to OUT_4	4 Analog Output Channels
29	$\overline{I}$/O	Determines whether data is being written into the Next Event latches or read from the Current Event latches
30	CS	Chip Select - a logic input
31, 32, 33, 34	A_0, A_1, A_2, A_3	IN Address - logic inputs or outputs as defined by $\overline{I}$/O pin, select one of eight IN channels
27, 28	B_0, B_1	OUT Address - logic inputs, select one of four OUT channels
35	$\overline{WR}$	Write command that latches A_0, A_1, A_2, A_3 into the Next Event latches
36	$\overline{SALVO}$	Master write command, that in one action, transfers all the data from Next Event latches into Current Event latches
37	RS	Reset - a low will clear the Current Event latches
22, 23, 24, 25	$\overline{DIS}_1$ to $\overline{DIS}_4$	Open drain disable outputs - these outputs pull low when the corresponding OUT channel is off

DEVICE DESCRIPTION

The DG884 is the world's first monolithic wideband crosspoint array that operates from dc to > 100 MHz. The DG884 offers the ability to route any one of eight input signals to any one of four OUT pins. Any input can be routed to one, two, three or four OUTs simultaneously with no risk of shorting inputs together (guaranteed by design).

Each crosspoint is configured as a "T" switch in which DMOS FETs are used due to their excellent low resistance and low capacitance characteristics. Each OUT line has a series switch that minimizes capacitive loading when the OUT is off.

Interfacing

The DG884 was designed to allow complex matrices to be developed while maintaining a simple control interface. The status of the $\overline{I}$/O pin determines whether the DG884 is being written to or read from (see Figures 1 and 2).

In order to WRITE to an individual latch, $\overline{CS}$ and $\overline{I}$/O need to be low, while $\overline{RS}$, $\overline{WR}$ and $\overline{SALVO}$ must be high. The IN to OUT path is selected by using address A_0 through A_3 to define the IN line and address B_0 and B_1 to define the OUT line. That is, The IN defined by A_0 through A_3 is electrically connected to the OUT defined by B_0, B_1. This chosen path is loaded into the Next Event latches when $\overline{WR}$ goes low and returns high again. This operation is repeated up to three more times if other crosspoint connections need to be changed.

Upon completing all crosspoint connections that are to be changed in a single device, other DG884s can be similarly preset by taking the $\overline{CS}$ pin low on the appropriate device. When all DG884s are preset, the Current Event latches are simultaneously changed by a single $\overline{SALVO}$ command applied to all devices. In this manner the crosspoint configuration of any number of devices can be simultaneously updated.

$\overline{DIS}$ Outputs

Four open drain disable OUTs are provided to control external line drivers or to provide visual or electrical signaling. For example, any or all of the DIS OUTs can directly interface with a CLC410 Video Amplifier to place it into a high impedance, low-power standby mode when the corresponding OUT is not being used. (See Figure 15). The $\overline{DIS}$ outputs are low and sink to V- when corresponding OUT is open or $\overline{RS}$ is low.

Reset

The reset function ($\overline{RS}$) allows the resetting of all crosspoints to a known state (open). At power up, the reset facility may be used to guarantee that all switches are open. It should be noted that $\overline{RS}$ clears the Current Event latches, but the Next Event latches remain unchanged. This useful facility allows the user to return the matrix to its previous state (prior to reset) by simply applying the $\overline{SALVO}$ command. Alternatively, the user can reprogram the Next Event latches, and then apply the $\overline{SALVO}$ command to reconfigure the matrix to a new state.

DEVICE DESCRIPTION

Readback

The Ī/O facility enables the user to write data to the Next Event latches or to read the contents of the Current Event latches. This feature permits the central controller to periodically monitor the state of the matrix. If a power loss to the controller occurs, the readback feature helps the matrix to recover rapidly. It also offers a means to perform PC board diagnostics both in production and in system operation.

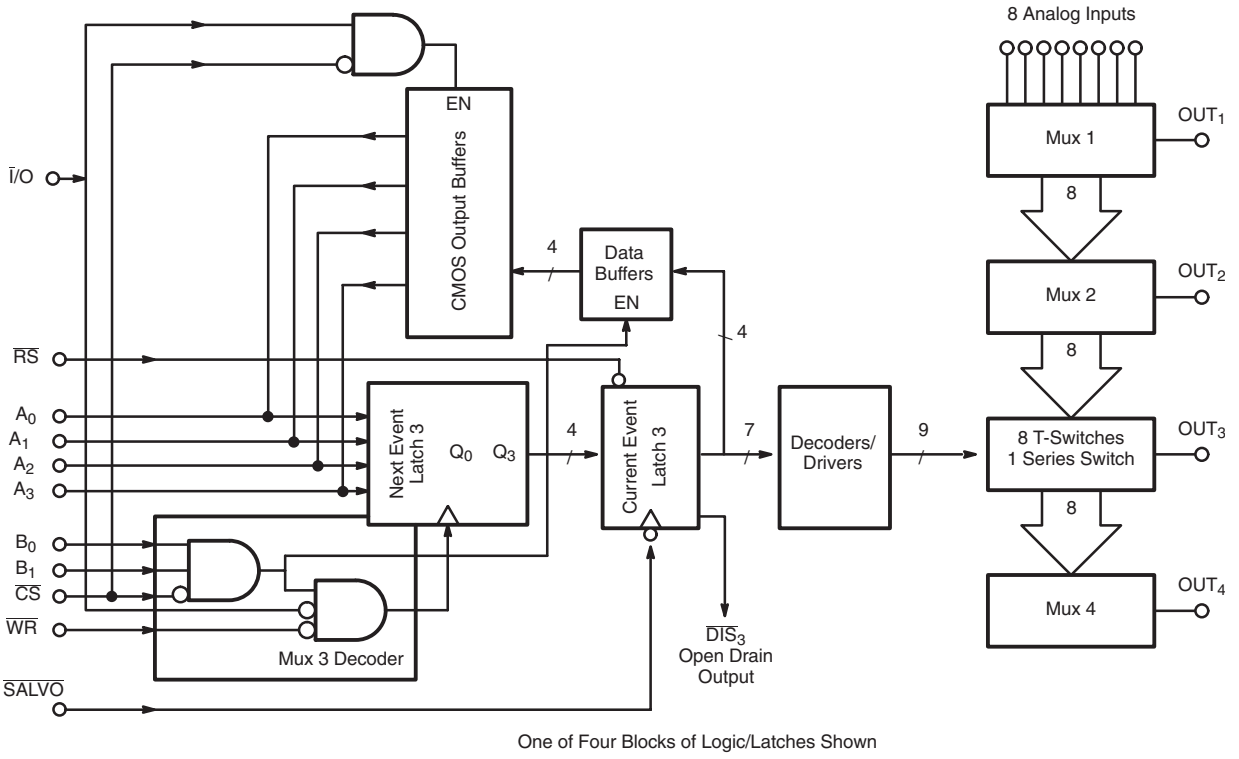


Figure 12. Control Circuitry

APPLICATIONS

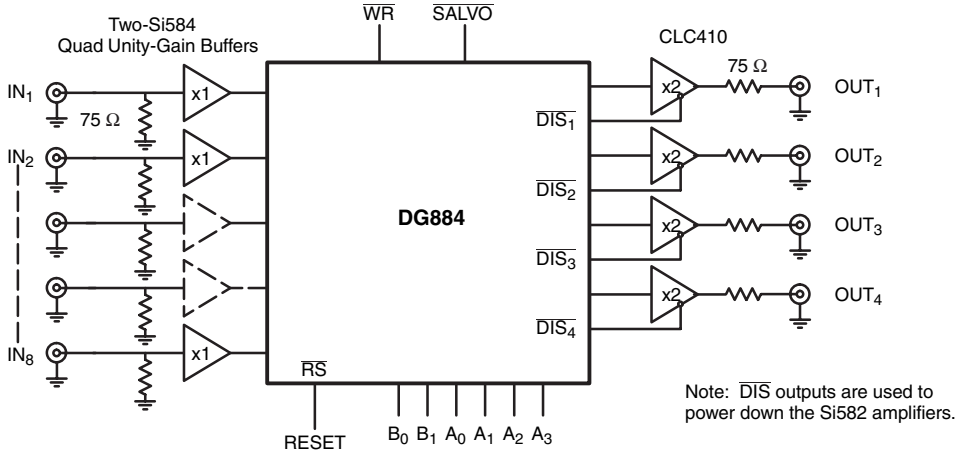


Figure 13. Fully Buffered 8 x 4 Crosspoint

APPLICATIONS

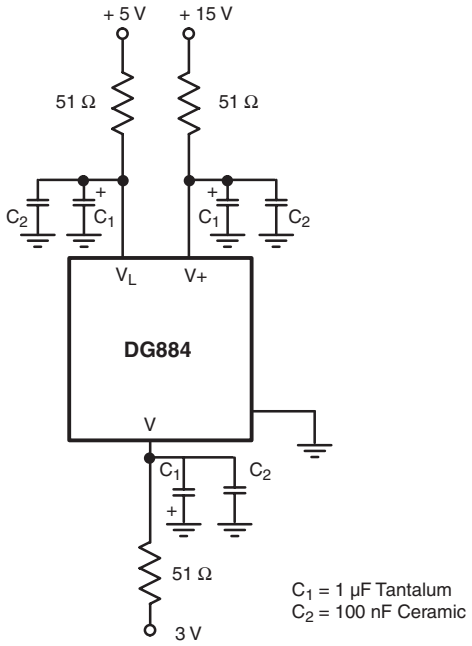


Figure 14. DG884 Power Supply Decoupling

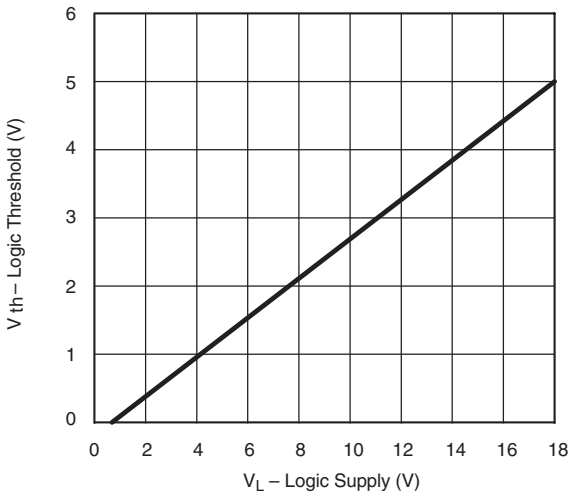


Figure 15. Switching Threshold Voltage vs. V_L

Power Supplies and Decoupling

A useful feature of the DG884 is its power supply flexibility. It can be operated from dual supplies, or a single positive supply (V- connected to 0 V) if required. Allowable operating voltage ranges are shown in Operating Voltage Range (Typical Characteristics) graph, page 6.

Note that the analog signal must not go below V- by more than 0.3 V (see absolute maximum ratings). However, the addition of a V- pin has a number of advantages:

1) It allows flexibility in analog signal handling, i.e. with V- = - 5 V and V+ = 15 V, up to ± 5 V ac signals can be accepted.
2) The value of on-capacitance [$C_{S(on)}$] may be reduced by increasing the value of V-. It is useful to note that optimum video differential phase and gain occur when V- is - 3 V. Note that V+ has no effect on $C_{S(on)}$.
3) V- eliminates the need to bias an ac analog signal using potential dividers and large decoupling capacitors.

It is established RF design practice to incorporate sufficient bypass capacitors in the circuit to decouple the power supplies to all active devices in the circuit. The dynamic performance of the DG884 is adversely affected by poor decoupling of power supply pins. Also, since the substrate of the device is connected to the negative supply, proper decoupling of this pin is essential.

Rules:

1) Decoupling capacitors should be incorporated on all power supply pins (V+, V-, V_L).
2) They should be mounted as close as possible to the device pins.
3) Capacitors should have good high frequency characteristics - tantalum bead and/or monolithic ceramic disc types are suitable.

Recommended decoupling capacitors are 1 to 10 µF tantalum bead, in parallel with 100 nF monolithic ceramic.

4) Additional high frequency protection may be provided by 51 Ω carbon film resistors connected in series with the power supply pins (see Figure 14).

The V_L pin permits interface to various logic types. The device is primarily designed to be TTL or CMOS logic compatible with + 5 V applied to V_L. The actual logic threshold can be raised simply by increasing V_L.

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A typical switching threshold versus V_L is shown in Figure 15.

These devices feature an address readback facility whereby the last address written to the device may be read by the system. This allows improved status monitoring and hand shaking without additional external components.

When the $\overline{I}$/O assigns the address output condition, the A_X address pins can sink or source current for logic low and high, respectively. Note that V_L is the logic high output condition. This point must be respected if V_L is varied for input logic threshold shifting.

Note: Even though these devices are designed to be latchup resistant, V_L must not exceed V+ by more than 0.3 V in operation or during power supply on/off sequencing.

Layout

The PLCC package pinout is optimized so that large crosspoint arrays can be easily implemented with a minimum number of PCB layers (see Figure 16). Crosstalk is minimized and off-isolation is optimized by having ground pins located adjacent to each input and output signal pins. Optimum off-isolation and low crosstalk performance can only be achieved by the proper use of RF layout techniques: avoid sockets, use ground planes, avoid ground loops, bypass the power supplies with high frequency type capacitors (low ESR, low ESL), use striplines to maintain transmission line impedance matching.

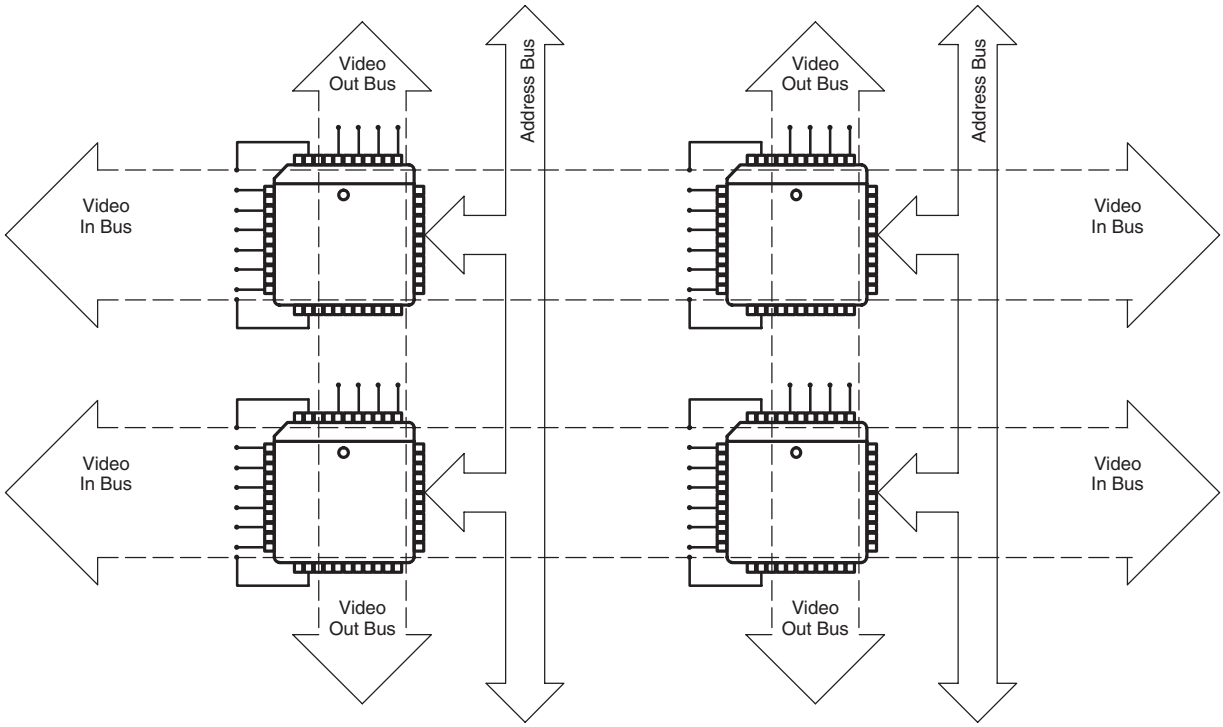

Figure 16. 16 X 8 Expandable Crosspoint Matrix Using DG884

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