



PRODUCT/PROCESS CHANGE NOTIFICATION

PCN APG-ABD/13/8055
Dated 04 Sep 2013

**VND5004ASP30-Eand VND5004BSP30-E: Die Attach Film (DAF)
implementation**

Table 1. Change Implementation Schedule

Forecasted implementation date for change	23-Sep-2013
Forecasted availability date of samples for customer	23-Sep-2013
Forecasted date for STMicroelectronics change Qualification Plan results availability	28-Aug-2013
Estimated date of changed product first shipment	23-Sep-2013

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	VND5004ASP30-E /TR-E and VND5004BSP30-E /TR-E
Type of change	Package assembly material change
Reason for change	Quality Improvement
Description of the change	Please be informend that Die Attach Film (DAF), instead of glue die attach, has been qualified on VND5004ASP30-E and VND5004BSP30-E .
Change Product Identification	Dedicated Finished-Good Codes
Manufacturing Location(s)	1]St Muar - Malaysia

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN APG-ABD/13/8055
Please sign and return to STMicroelectronics Sales Office		Dated 04 Sep 2013
<input type="checkbox"/> Qualification Plan Denied <input type="checkbox"/> Qualification Plan Approved <input type="checkbox"/> Change Denied <input type="checkbox"/> Change Approved	Name:	
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DOCUMENT APPROVAL

Name	Function
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Nicoloso, Riccardo	Product Manager
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VND5004ASP30-E and VND5004BSP30-E: Die Attach Film (DAF) Implementation

WHAT

On VND5004ASP30-E (VH01 internal silicon code) and VND5004BSP30-E (VH02 internal silicon code) products; Die Attach Film (DAF) will be implemented instead of current glue die attach. See below change matrix.

Change Matrix

	Current	New
Frame	MultiPowerSO-30 DualPad	MultiPowerSO-30 DualPad
Wire Bonding	Au 1.2 mils /Al 15 mils	Au 1.2 mils /Al 15 mils
Molding Compound	Sumitomo EME-G600C	Sumitomo EME-G600C
Die attach (Power die)	Soft Solder (Pb/Ag/Sn)	Soft Solder (Pb/Ag/Sn)
Die attach (Control/Signal die)	Glue QMI9507	DAF ADWILL LE-5000P8AS

WHY

Quality Improvement.

WHO

All the Customers that are using VND5004ASP30-E and VND5004BSP30-E products.

WHEN

Change will be implemented according to the following schedule:

- Qualification results: enclosed to this PCN (RR000213CT2235).
- Samples availability: wk39-2013
- Tentative Implementation: wk39-2013

WHERE

Muar Assembly Plant.

VND5004ASP-E (VH01) - MultiPwSO30
Process changes qualification

- CDAF usage on signal die
- DAF usage on signal die
- Die thickness increase

General Informations	
Commercial Product	VND5004ASP-E
Product Line	VH01
Silicon process technology	VIPower M0_5
Package	MultiPowerSO_30

Locations	
Diffusion fab location:	ST CTM6 Catania (Italy)
Diffusion fab location:	ST AMK6 Ang Mo Kio (Singapore)
Assembly plant location	ST Muar (Malaysia)
Test plant location	ST Muar (Malaysia)
Reliability lab location	ST Catania (Italy)

Revision history

REV.	Date of Release	Author	Changes description
0.1	January 29 th 2013	F.Ceraulo	Creation
0.2	April 16 th 2013	F. Ceraulo	Add info related to DAF trial

Reliability and electrical test executed by:

M. Palermo
 Rel. Eng.
 IMS Rel Dept. – APG Support

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- 1. Reliability evaluations overview

1.1 Objectives

Aim of this report is to present the results of the reliability evaluations performed on **VNDE004ASP-E** (VH01 as ST internal line code) in order to qualify some process changes:

- 1) Die thickness increase: from 220 μ m to 280 μ m
- 2) Die attach on signal part: from glue QMI9507 to Conductive Die Attach Film (CDAF)
- 3) Die attach on signal part: from glue QMI9507 to Die Attach Film (DAF)

This product is a 4mohm Dual Channel High Side Driver with analog current sense for Automotive Applications designed in VIPower M0_5 technology, composed by two power dice (VNI4 as ST internal silicon line) diffused in ST AMK6 Ang Mo Kio (Singapore) 6" wafer fab and one signal die (VNG4 as ST internal silicon line) diffused in ST CT6 Catania (Italy) 6" wafer fab. These changes are effective for the MultiPowerSO30 package with the assembly process done in ST Muar (Malaysia).

The reliability evaluation was based on three diffusion lots:

- 1) 1st lot used as reference diffused with 220 μ m as die thickness and assembled with std die attach GLUE QMI9507 for signal part
- 2) 2nd lot used as trial diffused with 280 μ m as die thickness and assembled with new die attach (CDAF)
- 3) 3rd lot used as trial diffused with 220 μ m as die thickness and assembled with new die attach (DAF)

According with the **AEC_Q100 Rev.G** specification for the Accelerated Environment Stress (test Group A) and the Accelerated Lifetime Simulation (test Group B) the following tests were performed: Preconditioning (PC), Temperature Humidity Bias (THB), Autoclave (AC), Thermal Cycling (TC), High Temperature Storage (HTS), High Temperature Operative Life (HTOL), Power Temperature Cycling (PTC).

An ESD (MM, HBM, CDM) and a Latch-UP (LU) characterization was done as Electrical Verification (test Group E).

The Wire Bond Pull/Shear tests (WBP, WBS) as Package Assembly Integrity (test Group C) was also performed.

1.2 Results

All reliability tests has been completed with positive results, neither functional nor parametric rejects were detected at final electrical testing.

The ESD/LU pointed out values aligned with the product's datasheet.

The Wire Bond Pull/Shear tests (WBP, WBS) didn't pointed out neither abnormal break loads nor forbidden failure modes.

Based on the overall positive results we consider the products qualified from a reliability point of view.

- 2. Traceability

➤ Std Lot as reference

Wafer fab information	
Wafer fab manufacturing location	VNG4 (signal): ST CT6 Catania (Italy) VNI4 (power) :ST AMK6 Ang Mo Kio (Singapore)
Wafer diameter (inches)	VNG4 (signal): 6 VNI4 (power): 6
Silicon process technology	VIpower M0_5
Die finishing back side	Ti-Ni-Au
Die size (micron)	VNG4 (signal): 2800 x 1560 VNI4 (power) : 7990 x 4000
Metal levels / materials	VNG4 (signal): 2 levels / Ti/TiN/Ti/AISiCu (3.2 µm last level) VNI4 (power) : 1 level / Ti/AISiCu (4.5 µm)
Die finishing front side	SiN/POLYIMIDE
Diffusion Lots #	VNG4 (signal): 3223145, VNI4 (power): 62230K, 62230L8
Wafer Thickness	VNG4 (signal): 220µm VNI4 (power): 420µm

Assembly Information	
Assembly plant location	ST Muar (Malaysia)
Package description	Multi PowerSO_30
Molding compound	RESIN SUMITOMO EME-G600C
Wires bonding materials/diameters	Au 1.2mils (on signal) / Al 15mils (on power)
Die attach material	GLUE QMI9507 PREFORM Pb/Ag/Sn 97.5/1.5/1
Assembly Lots #	992350LU02

Final Testing Information	
Electrical testing manufacturing location	ST Muar (Malaysia)

Reliability Information	
Reliability test execution location	ST Catania (Italy)

➤ **Trial Lot (280µm die thickness, CDAF)**

Wafer fab information	
Wafer fab manufacturing location	VNG4 (signal): ST CT6 Catania (Italy) VNI4 (power): ST AMK6 Ang Mo Kio (Singapore)
Wafer diameter (inches)	VNG4 (signal): 6 VNI4 (power): 6
Silicon process technology	VIPOWER M0_5
Die finishing back side	Ti-Ni-Au
Die size (micron)	VNG4 (signal): 2800 x 1560 VNI4 (power) : 7990 x 4000
Metal levels / materials	VNG4 (signal): 2 levels / Ti/TiN/Ti/AlSiCu (3.2 µm last level) VNI4 (power): 1 level / Ti/AlSiCu (4.5 µm)
Die finishing front side	SiN/POLYIMIDE
Diffusion Lots #	VNG4 (signal): 3223145B, VNI4 (power) 62230KN, 62230L8B
Wafer Thickness	VNG4 (signal): 280um VNI4 (power): 420um

Assembly Information	
Assembly plant location	ST Muar (Malaysia)
Package description	Multi PowerSO_30
Molding compound	RESIN SUMITOMO EME-G600C
Wires bonding materials/diameters	Au 1.2mils (on signal) / Al 15mils (on power)
Die attach material	HENKEL C115-Conductive Film (cDAF) PREFORM Pb/Ag/Sn 97.5/1.5/1
Assembly Lots #	992350LU04

Final Testing Information	
Electrical testing manufacturing location	ST Muar (Malaysia)

Reliability Information	
Reliability test execution location	ST Catania (Italy)

➤ **Trial Lot (220µm die thickness, DAF)**

Wafer fab information	
Wafer fab manufacturing location	VNG4 (signal): ST CT6 Catania (Italy) VNI4 (power): ST AMK6 Ang Mo Kio (Singapore)
Wafer diameter (inches)	VNG4 (signal): 6 VNI4 (power): 6
Silicon process technology	VIPOWER M0_5
Die finishing back side	Ti-Ni-Au
Die size (micron)	VNG4 (signal): 2800 x 1560 VNI4 (power) : 7990 x 4000
Metal levels / materials	VNG4 (signal): 2 levels / Ti/TiN/Ti/AlSiCu (3.2 µm last level) VNI4 (power): 1 level / Ti/AlSiCu (4.5 µm)
Die finishing front side	SiN/POLYIMIDE
Diffusion Lots #	VNG4 (signal): 3144854, VNI4 (power) 6222TTE, 6222X1X
Wafer Thickness	VNG4 (signal): 220um VNI4 (power): 420um

Assembly Information	
Assembly plant location	ST Muar (Malaysia)
Package description	Multi PowerSO_30
Molding compound	RESIN SUMITOMO EME-G600C
Wires bonding materials/diameters	Au 1.2mils (on signal) / Al 15mils (on power)
Die attach material	Adwill LE5000P8AS (DAF) PREFORM Pb/Ag/Sn 97.5/1.5/1
Assembly Lots #	992291KU01

Final Testing Information	
Electrical testing manufacturing location	ST Muar (Malaysia)

Reliability Information	
Reliability test execution location	ST Catania (Italy)

- 3. Devices characteristics

3.1 Generalities



VND5004A-E VND5004ASP30-E

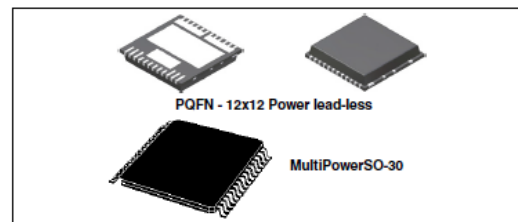
Double 4mΩ high side driver with analog current sense
for automotive applications

Features

Max transient supply voltage	V_{CC}	41V
Operating voltage range	V_{CC}	4.5 to 27V
Max On-State resistance (per ch.)	R_{ON}	4 mΩ
Current limitation (typ)	I_{LIMH}	100A
Off state supply current	I_S	2 μA ⁽¹⁾

1. Typical value with all loads connected

- General
 - Inrush current active management by power limitation
 - Very low stand-by current
 - 3.0V CMOS compatible input
 - Optimized electromagnetic emission
 - Very low electromagnetic susceptibility
 - In compliance with the 2002/95/EC European directive
- Diagnostic functions
 - Proportional load current sense
 - Current sense disable
 - Thermal shutdown indication
- Protection
 - Undervoltage shut-down
 - Overvoltage clamp
 - Load current limitation
 - Thermal shut down
 - Self limiting of fast thermal transients
 - Protection against loss of ground and loss of V_{CC}
 - Reverse battery protection with self switch on of the PowerMOS (see [Application schematic on page 18](#))
 - Electrostatic discharge protection



Application

- All types of resistive, inductive and capacitive loads
- Suitable for power management applications

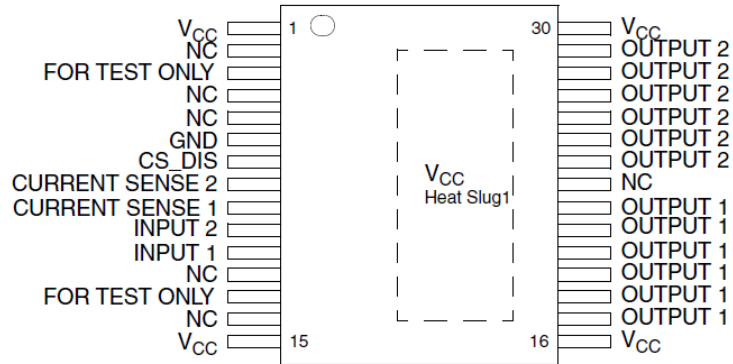
Description

The VND5004ATR-E and VND5004ASP30-E are devices made using STMicroelectronics VIPower technology. They are intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp and load dump protection circuit protect the devices against transients on the V_{CC} pin (see ISO7637 transient compatibility table). These devices integrate an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open. When CS_DIS is driven high, the CURRENT SENSE pin is high impedance. Output current limitation protects the devices in overload condition. In case of long duration overload, the devices limit the dissipated power to a safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as a fault condition disappears.

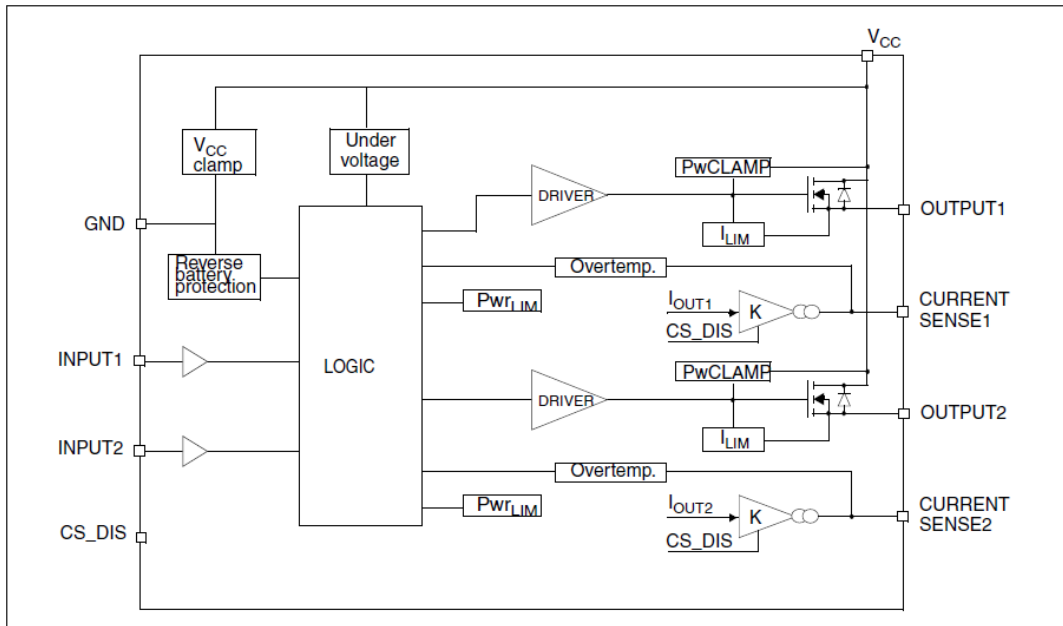
Table 1. Devices summary

Package	Order codes		
	Tube	Tape and Reel	Tray
PQFN-12x12 Power lead-less	-	VND5004ATR-E	VND5004A-E
MultiPowerSO-30	VND5004ASP30-E	VND5004ASP30TR-E	-

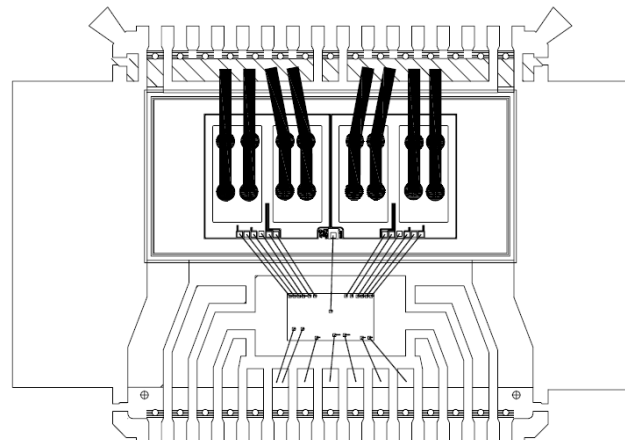
3.2 Pins connection



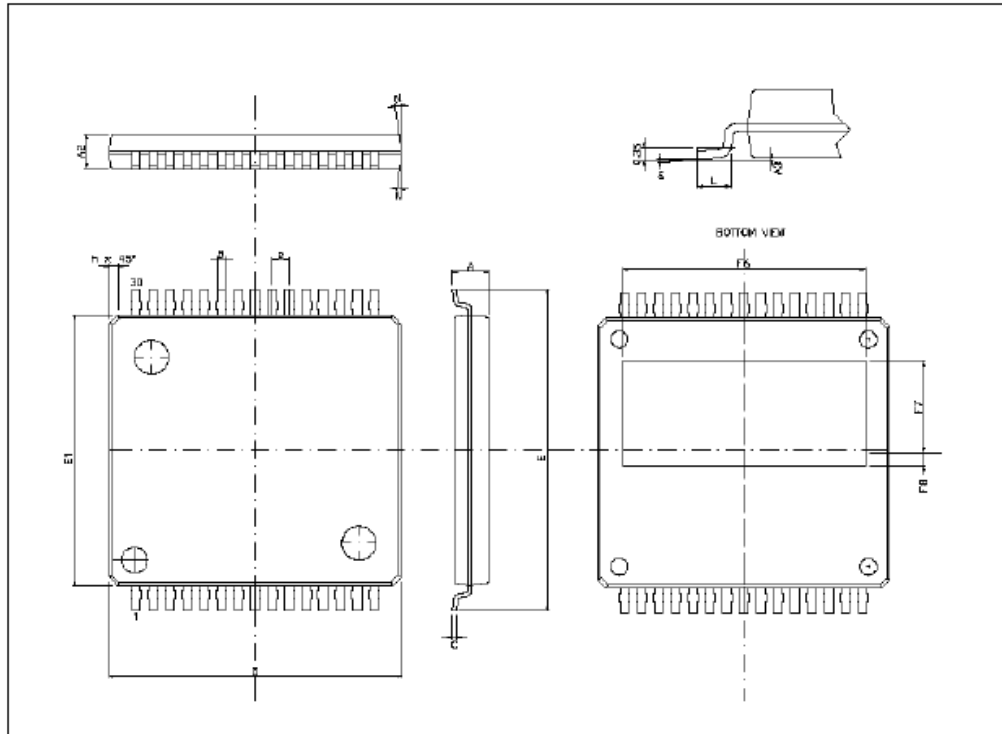
3.3 Blocks diagram



3.4 Bonding diagram



3.5 Package outline/Mechanical data



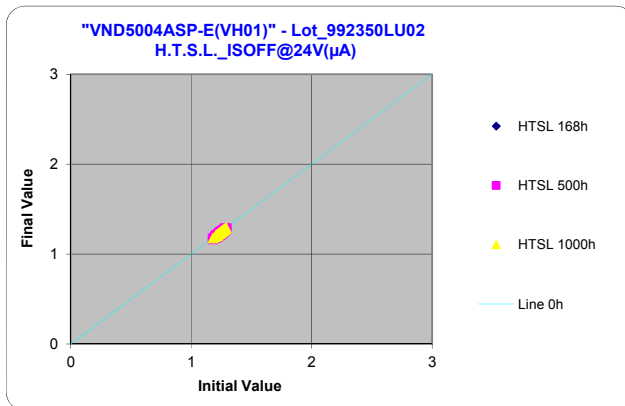
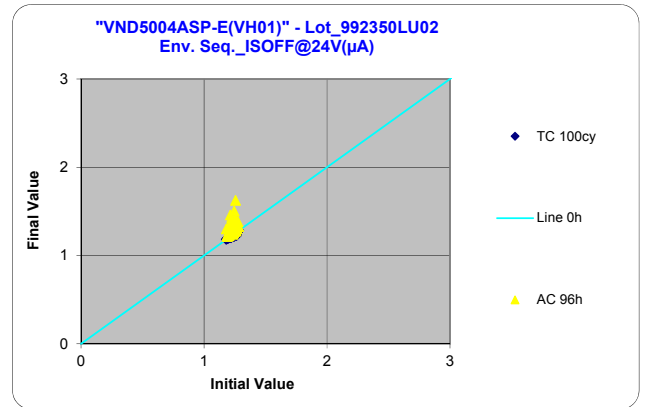
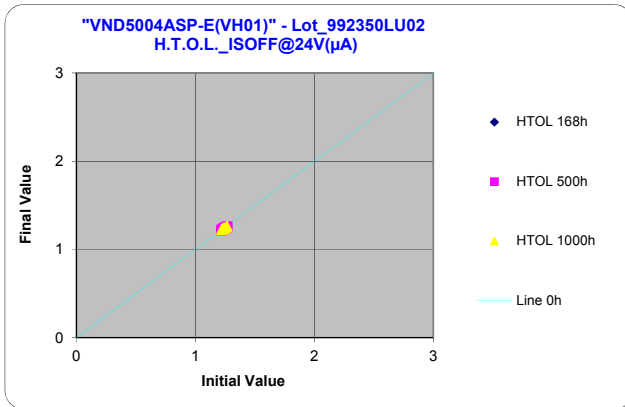
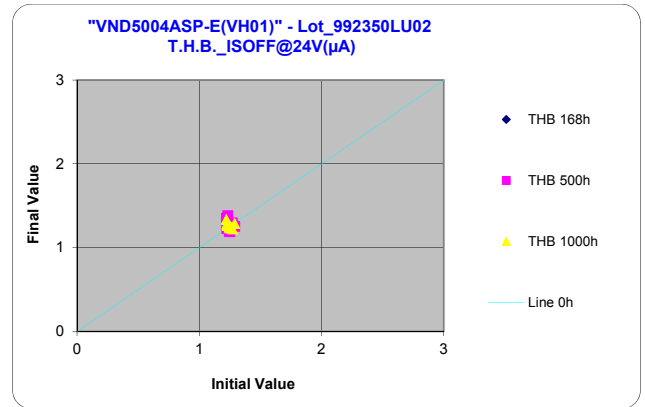
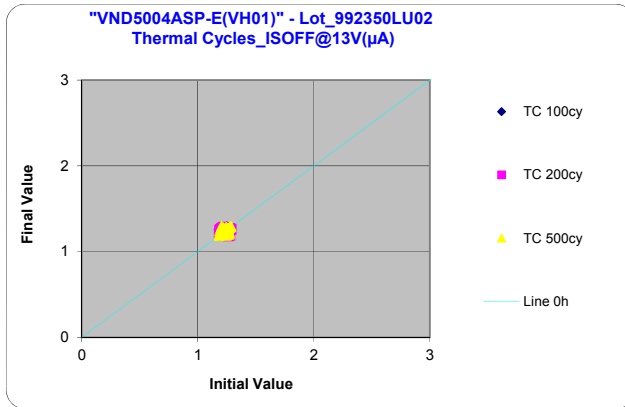
Symbol	Millimeters		
	Min.	Typ.	Max.
A			2.35
A2	1.85		2.25
A3	0		0.1
B	0.42		0.58
C	0.23		0.32
D	17.1	17.2	17.3
E	18.85		19.15
E1	15.9	16	16.1
"e"	1		
F6		14.3	
F7		5.45	
F8		0.73	
L	0.8		1.15
N			10 Deg
S	0 Deg		7 Deg

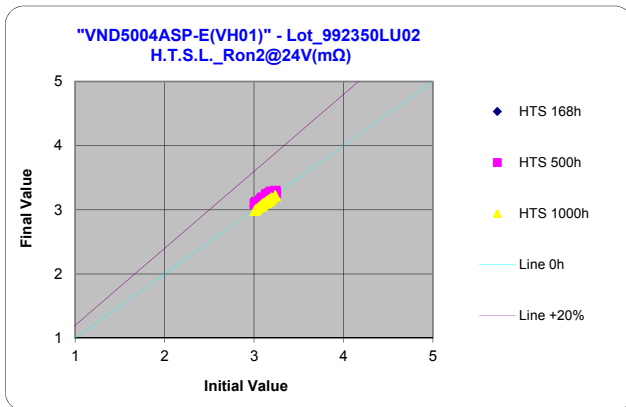
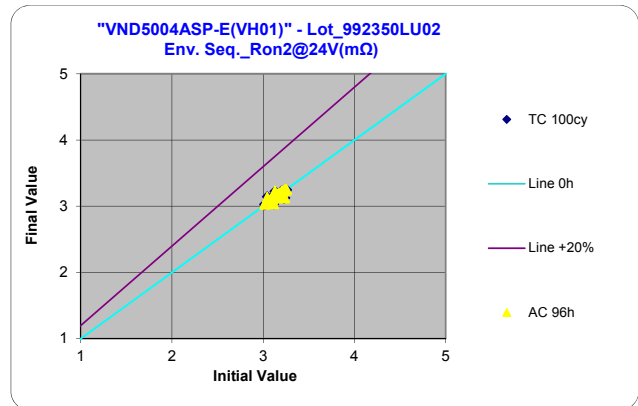
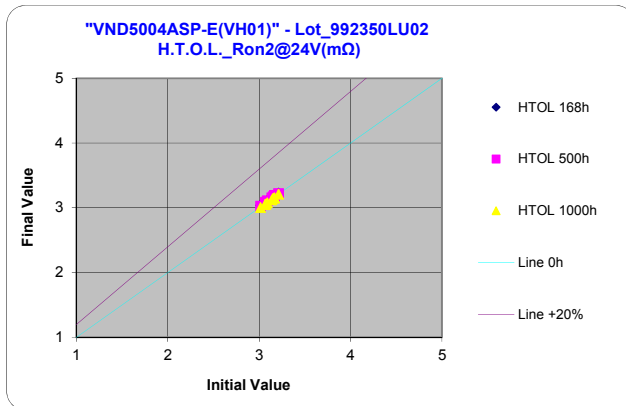
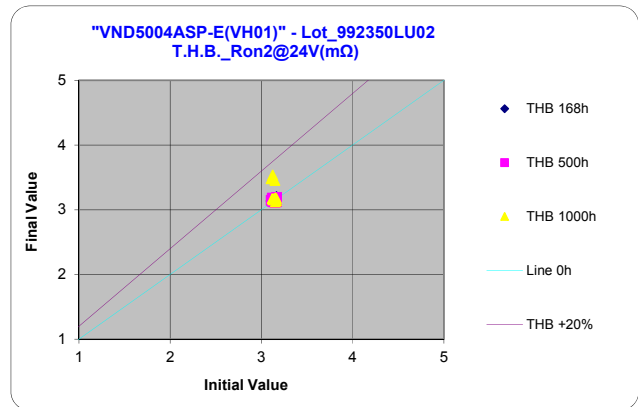
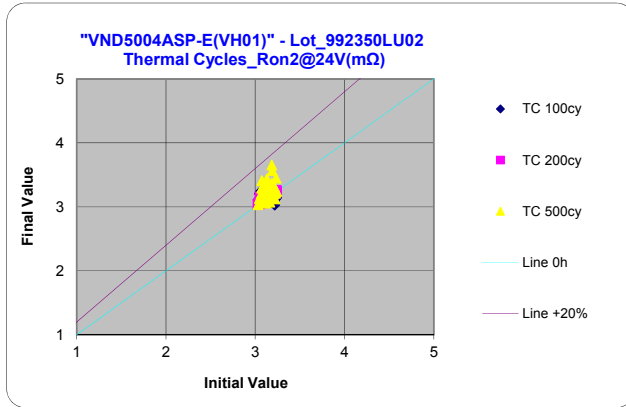
- 4. Reliability qualification plan and results

AEC #	Test Name	STM Test Conditions	Sample Size/ Lots	Results Fails/SS/Lots	Comments
A1	PC Pre Cond	- Preconditioning according to level 3 Jeduc JESD22-A113F including 5 Temperature Cycling Ta=-40°C/+60°C - Reflow according to Jeduc JSTD020D-1	Before THB, AC, TC, PTC, HTOL. Reliability executed on units soldered on PCB		
A2	THB Temp Humidity Bias	Ta=85°C, RH=85%, Vcc=24V for 1000 hours	77/3	0/77/3	
A3	AC Autoclave	ENV. SEQ. Enviromental Sequence TC (Ta=-65°C / +150°C for 100 cycles) + AC (Ta=121°C, Pa=2atm for 96 hours)	77/3	0/77/3	
A4	TC Temp. Cycling	Ta=-65°C / +150°C for 500 cycles	77/3	0/77/3	
A6	HTSL High Temp. Storage Life	Ta=150°C for 1000 hours.	45/3	0/45/3	
A5	PTC Power Temp. Cycling	Per JA105. Ta=-40°C / +125°C for 1000 cycles.	45/1	0/45/1	
B1	HTOL High Temp. Op. Life	Bias Static stress (JESD22-A108): Ta=125°C, Vcc=28V for 1000 hours	77/3	0/77/3	
C1	WBS Wire Bond Shear	Per AEC-Q100-001	30 bonds from minimum 5 of units from 1 lot	All measurement within spec limits	
C2	WBP Wire Bond Pull	Per MIL-STD883, M2011 Condition C or D	30 bonds from minimum 5 of units from 1 lot	All measurement within spec limits	
E2	ESD HBM / MM	HBM=[R=1.5kΩ, C=100pF]	6/1	HBM: ±2KV	
E3	ESD CDM		6/1	CDM: ±750	
E4	LU Latch-Up		6/1	±50mA	

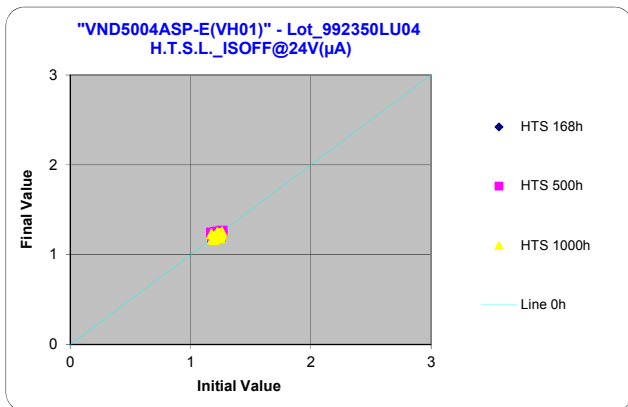
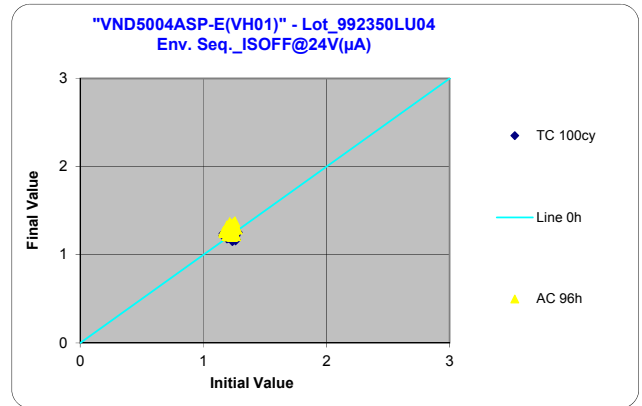
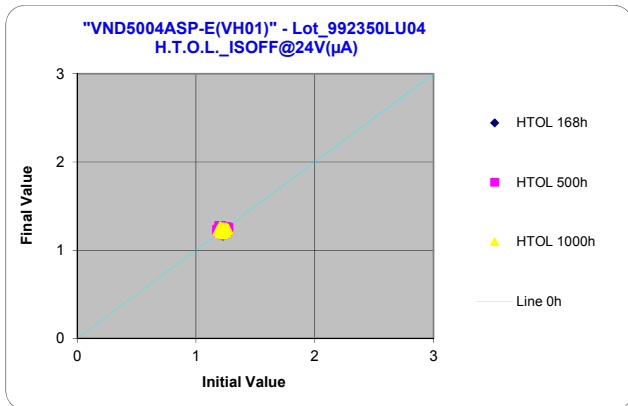
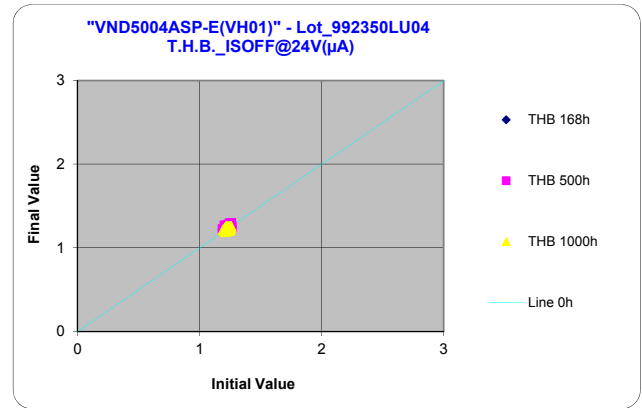
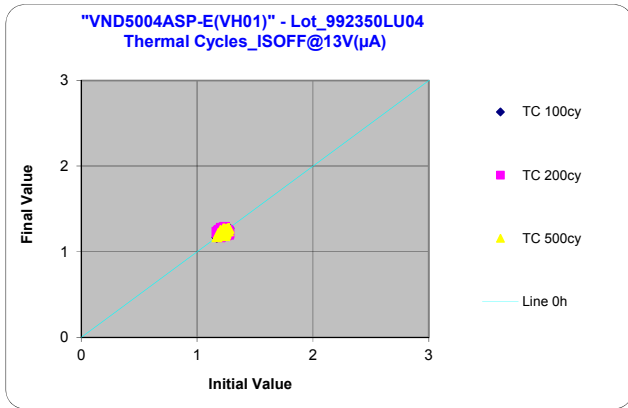
- 5. Electrical drift analysis

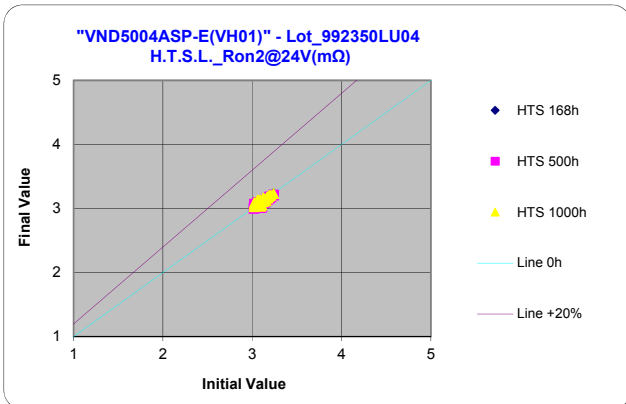
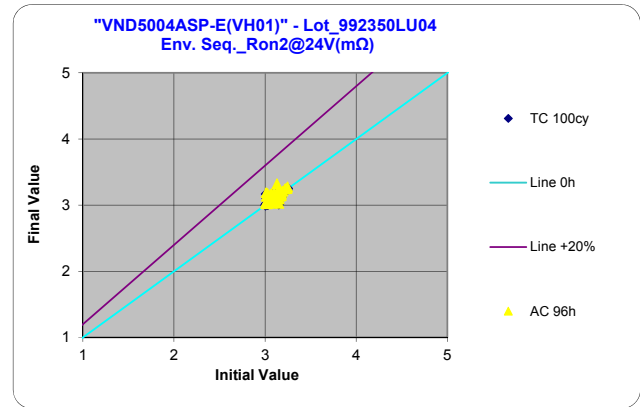
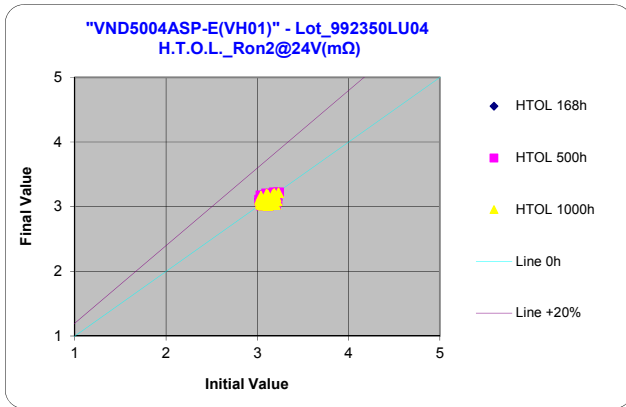
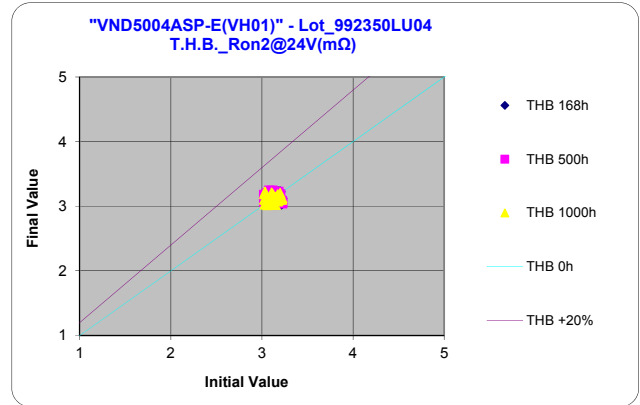
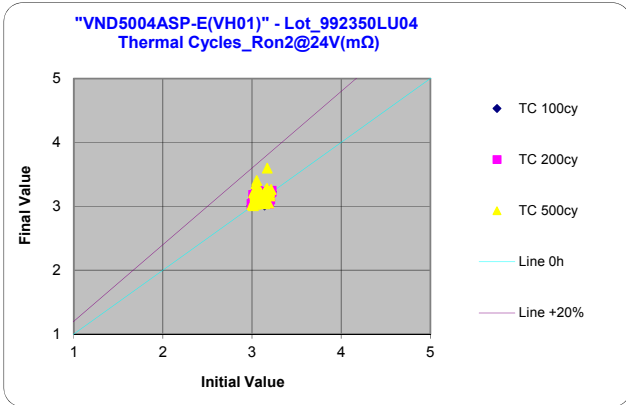
❖ Lot# 992350LU02 (Std Lot)



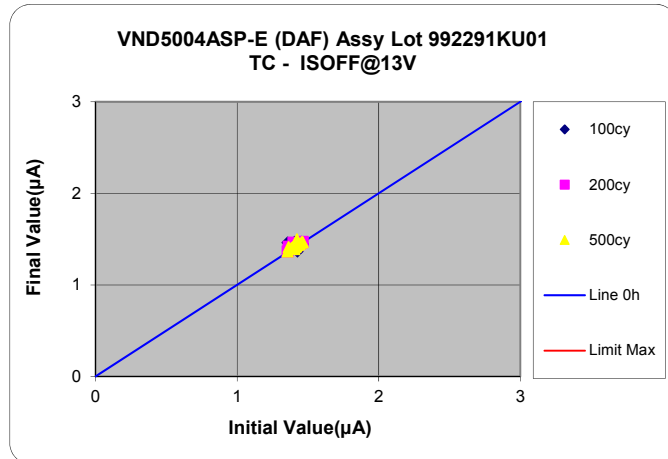
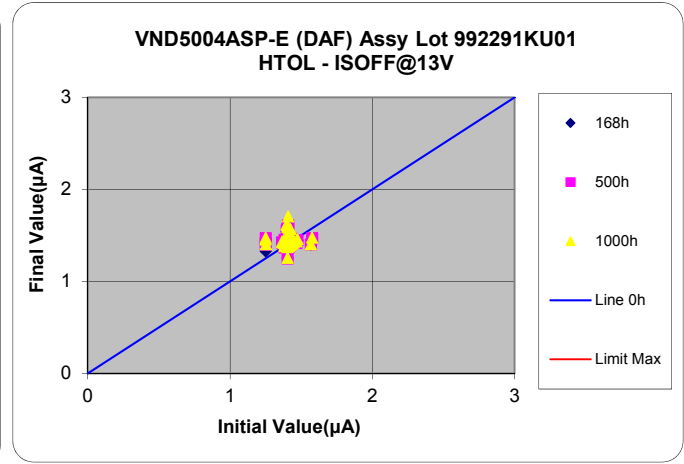
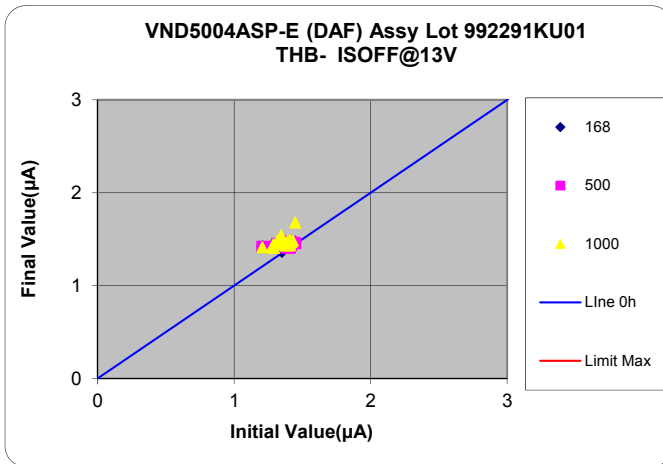


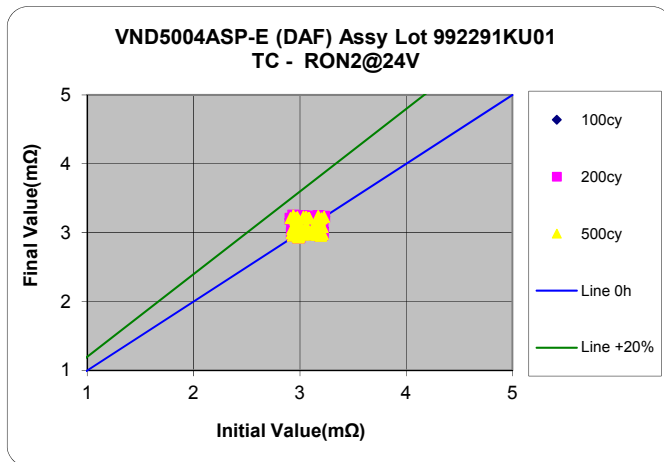
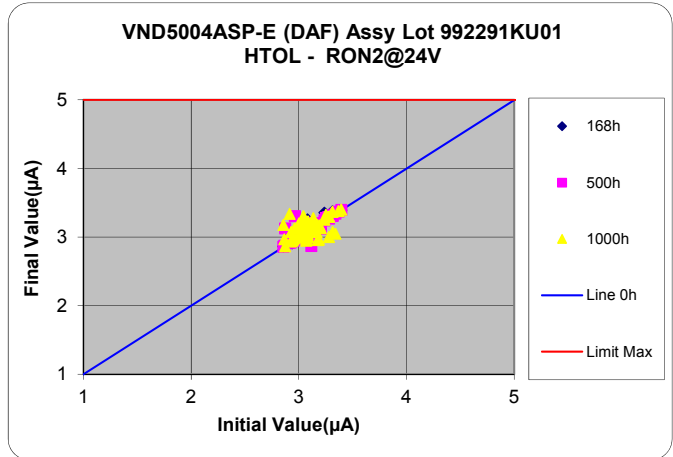
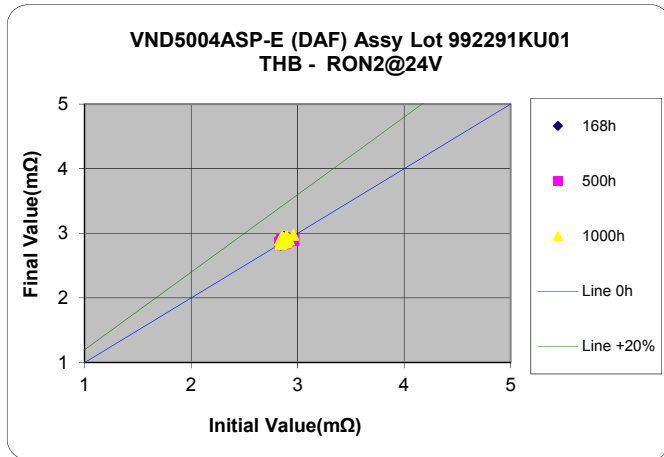
❖ **Lot# 992350LU04 (cDAF Trial Lot)**





❖ Lot# 992291KU01 (DAF Trial Lot)





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Public Products List

PCN Title : VND5004ASP30-Eand VND5004BSP30-E: Die Attach Film (DAF) implementation

PCN Reference : APG-ABD/13/8055

PCN Created on : 29-AUG-2013

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change:

ST COMMERCIAL PRODUCT

VND5004ASP30-E

VND5004ASP30TR-E

VND5004BSP30-E

VND5004BSP30TR-E

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