NCV7601

Quad Driver

This automotive grade product provides a versatile interface between control logic and many types of loads. The inputs accept a wide range of control signal levels while the open−collector outputs feature independent thermal and current limiting. Integral transient suppression diodes are provided at all inputs and outputs.

Features

- Operation in −40°C − 125°C Environment
- TTL/DTL/CMOS Compatible Inputs
- NAND Logic with Common Enable
- $V_{CEX} \geq 60$ V, $V_{CE(SUS)} \geq 40$ V
- $V_{CE(SAT)} \leq 650$ mV @ $I_C = 600$ mA
- Thermally Efficient Fused−Lead Package
- Pin Compatible with:
  - CA3242/CA3262
  - UDx2543/UDx2549/UDx2559
  - L6220/L6221/L9222
- AEC Qualified
- PPAP Capable
- Pb−Free Package is Available*

Typical Applications

- Body and Drivetrain Electronics
- Incandescent Lamp/LED Loads
- Solenoid/Relay/Inductor Loads
- Heater/Resistor Loads
- Stepper/DC Motor Loads

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
V_{CC}	−0.3 to 7.0	V
Logic Input Voltage (INA, INB, INC, IND, ENABLE)	−0.3 to 15	V
Power Output (OUTA, OUTB, OUTC, OUTD)	−0.3 to 60	V
Junction Temperature Range, T_J	−40 to 150	°C
Storage Temperature Range	−55 to 150	°C
ESD Susceptibility (Human Body Model)	2.0	kV
Package Thermal Resistance Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 15 50	 °C/W °C/W
Lead Temperature Soldering: Wave Solder (through hole styles only) (Note 1)	260 peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. 10 second maximum.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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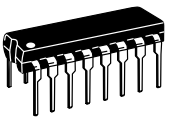
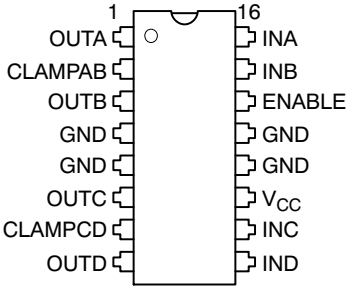


PDIP−16
P SUFFIX
CASE 648

MARKING DIAGRAM

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping
NCV7601P	PDIP−16	25 Units/Rail
NCV7601PG	PDIP−16 (Pb−Free)	25 Units/Rail

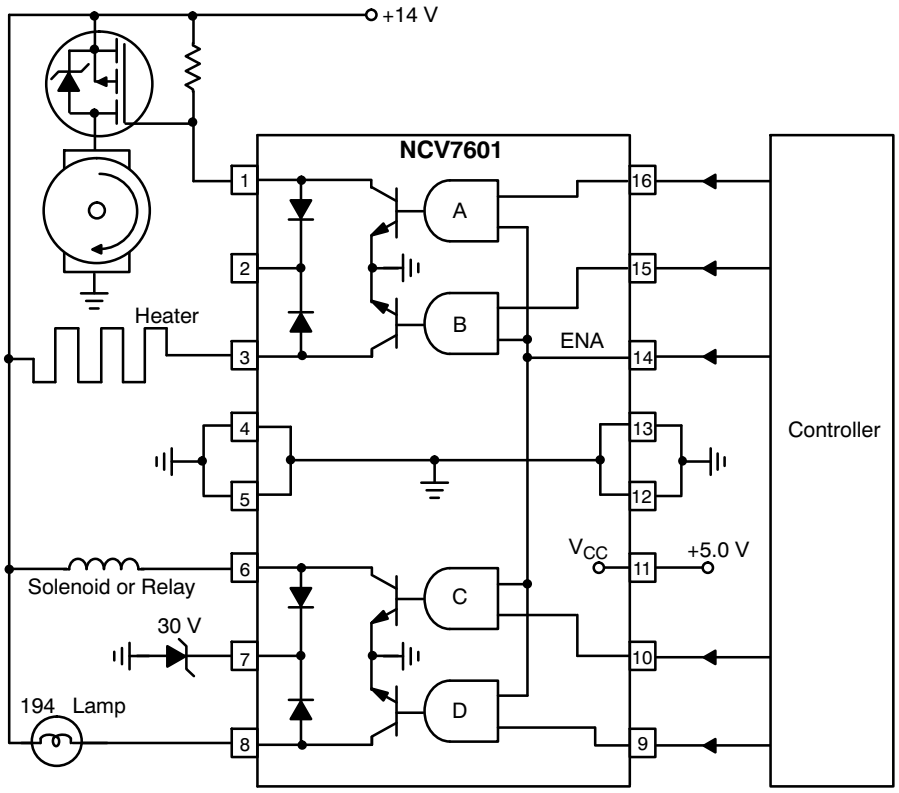


Figure 1. Typical Driver Applications

ELECTRICAL CHARACTERISTICS (4.0 V ≤ V_{CC} ≤ 5.5 V, −40°C ≤ T_J ≤ 125°C, unless otherwise specified.) Note 2

Characteristic	Test Conditions	Min	Typ	Max	Unit
GENERAL					
V_{CC} Supply Current	Outputs Off, V_{CC} = 5.5 V	–	–	5.0	mA
	Note 3 I_{OUT} = 600 mA, V_{CC} = V_{IN} = 5.5 V (four outputs on)	–	–	65	mA
	(one output on)	–	–	20	mA
OUTPUT DRIVERS					
Saturation Voltage	I_{OUT} = 600 mA, V_{IN} = 2.0 V, V_{CC} = 4.0 V	–	–	650	mV
Leakage Current	V_{OUT} = 60 V, V_{IN} = 0.8 V, V_{CC} = 5.5 V	–	–	50	μA
Current Limit	4.5 V < V_{OUT} < 16 V, V_{CC} = 5.0 V	–	–	1.8	A
Thermal Shutdown	–	150	180	210	°C
Sustaining Voltage, $V_{CE(SUS)}$	V_{CC} = 5.5 V	40	–	–	V
CLAMP DIODES					
Forward Voltage	I_F = 1.5 A, V_{CC} = 5.5 V	–	–	2.0	V
Leakage Current	V_R = 60 V, V_{CC} = 5.5 V	–	–	100	μA
INPUT					
Input Current	0 V ≤ V_{IN} ≤ V_{CC}	−2.0	–	10	μA
Input High Voltage	I_{OUT} = 600 mA	2.0	–	–	V
Input Low Voltage	I_{OUT} = 600 mA	–	–	0.8	V
AC CHARACTERISTICS (Note 4)					
Turn−On Delay, Turn−Off Delay	I_{OUT} = 500 mA	–	–	10	μs

2. Designed to meet these characteristics over the stated temperature range, though may not be 100% parametrically tested in production.
3. Pulse test.
4. Input rise time ≤ 10 ns, falltime ≤ 10 ns, measured at 50% points.

PACKAGE PIN DESCRIPTION

PACKAGE PIN #	PIN SYMBOL	FUNCTION
1	OUTA	Driver A Output
2	CLAMPAB	Diode Clamp to Driver A and Driver B
3	OUTB	Driver B Output
4	GND	Ground
5	GND	Ground
6	OUTC	Driver C Output
7	CLAMPCD	Diode Clamp to Driver C and Driver D
8	OUTD	Driver D Output
9	IND	Driver D Input
10	INC	Driver C Input
11	V_{CC}	5.0 V Input Supply Voltage
12	GND	Ground
13	GND	Ground
14	ENABLE	ENABLE Input to all Drivers
15	INB	Driver B Input
16	INA	Driver A Input

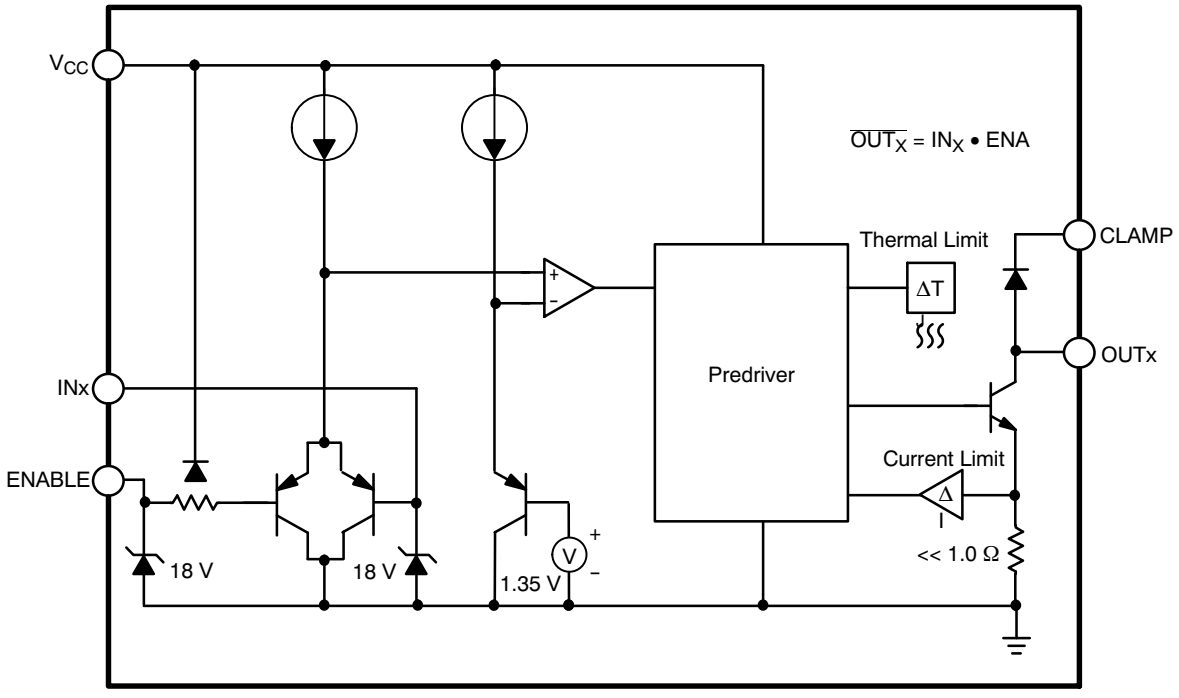


Figure 2. Simplified Block Diagram – Each Driver

TYPICAL PERFORMANCE CHARACTERISTICS

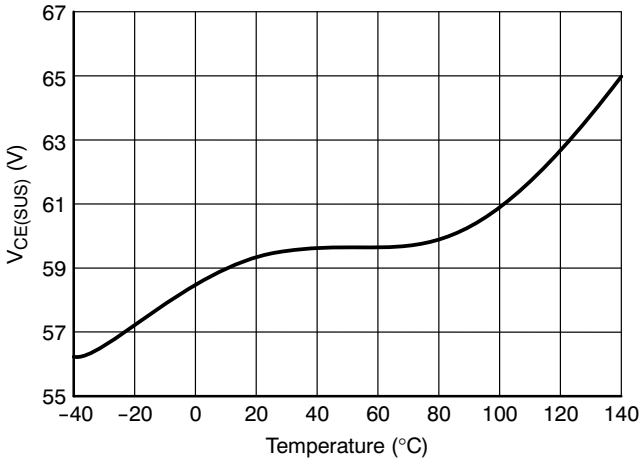


Figure 3. Typical $V_{CE(SUS)}$

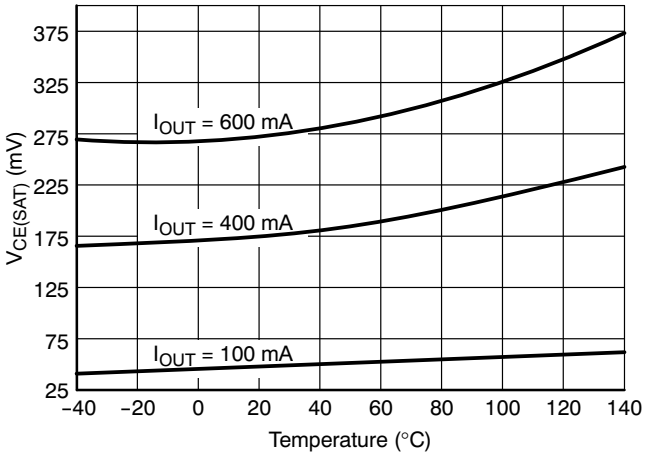


Figure 4. Typical Output On Voltage, V_{CC} = 4.0 V

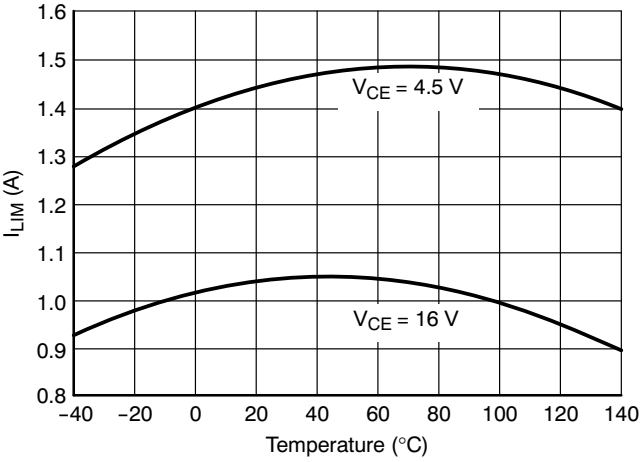


Figure 5. Typical Output Current Limit, V_{CC} = 5.0 V

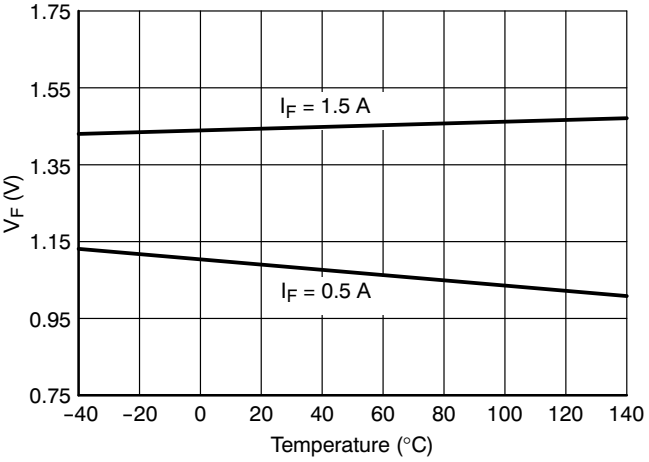


Figure 6. Typical Clamp Diode Forward Voltage

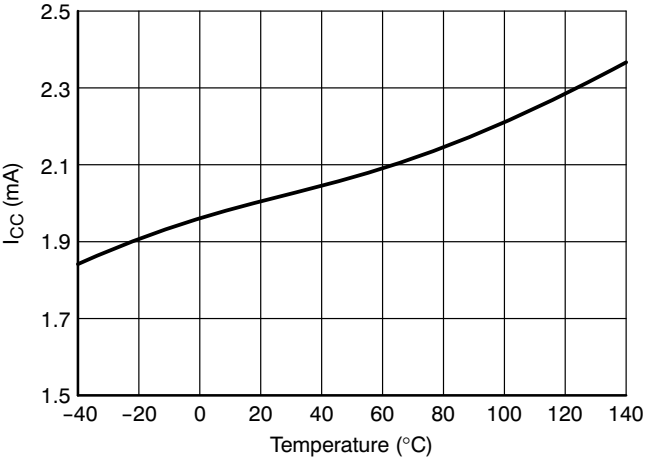


Figure 7. Typical V_{CC} Current – No Outputs On, V_{CC} = 5.5 V

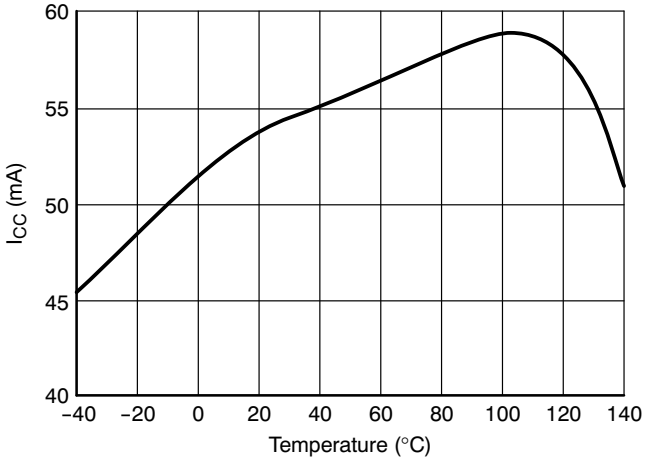


Figure 8. Typical V_{CC} Current – All Outputs On, V_{CC} = 5.5 V, I_{OUT} = 600 mA (Each Output)

TYPICAL PERFORMANCE CHARACTERISTICS

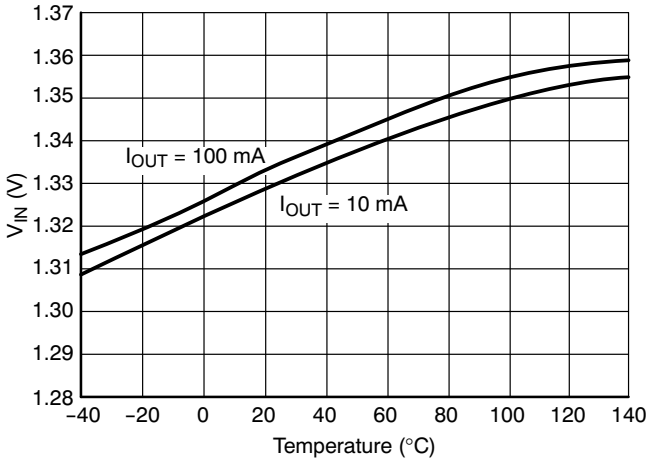


Figure 9. Typical Input Threshold Voltage, V_{CC} = 5.0 V

DETAILED OPERATING DESCRIPTION

The NCV7601 Quad Driver consists of four identical driver sections with output clamp diodes and a common bias generator.

Each driver input (Figure 2) is buffered by a PNP emitter follower for reduced input bias current and features a nominal 18 V Zener input clamp for transient protection. Each input is compared to a separate temperature−compensated reference, which provides a nominal 1.35 V comparison threshold. With the addition of an external series resistor, the inputs can be interfaced directly to +14 V automotive system voltages. Floating inputs are interpreted as high.

Each driver output NPN is supplied with a substantially fixed base current from the +5.0 V V_{CC} pin by a pre−driver. Each pre−driver multiplies a temperature−compensated reference current when its control input and the common enable input is high. Current limit and thermal limit circuits act independently within the pre−driver to reduce base drive to the output NPN. The independent limit operation allows the driver to handle inrush current from lamp loads while protecting the driver from fault conditions that exist long enough to raise the temperature at that driver to its thermal limit threshold. Each driver has its own temperature−sensing device located in close proximity to the output NPN. The separate sensing devices are strategically placed at the corners of the die to reduce interaction between them.

APPLICATIONS INFORMATION

The NCV7601 Quad Driver interfaces high power loads to low power control signals. The four open−collector NAND drivers with common ENABLE are TTL, DTL and CMOS compatible. Any number of drivers may be parallel connected to drive loads greater than each driver's nominal capability. Power for the Quad's control logic and output pre−drive is supplied from the +5.0 V V_{CC} pin, and is proportional to the number of active inputs. Minimum standby power is consumed when the ENABLE input is low. Each driver is individually protected with current limit and thermal limit circuitry. Drivers with fault loads are protected while drivers with normal loads continue to operate, provided that sufficient heat sinking maintains a good thermal gradient between all drivers.

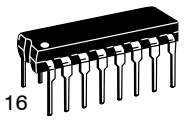
Clamp diodes at each driver output provide a means for managing inductive load transients. The common cathode pin for each driver pair can be connected to the load supply voltage for suppression of minor transients resulting from wiring harness inductances. The use of an external Zener diode or TVS (Transient Voltage Suppressor) device such as the ON Semiconductor 1.5SMCXXXAT3 series is strongly recommended when driving large inductive loads or when load supply transients can be expected to exceed the Quad Driver's $VCE_{(SUS)}$ rating. The use of a TVS device provides an additional benefit by reducing the decay time of inductive loads. More information on safeguarding the Quad's output NPN's and about transient suppression methods and device selection is available in ON Semiconductor application notes "Understanding Power Transistors Breakdown Parameters", document number AN1628/D, "A Review of Transients and their Means Of Suppression", document number AN843/D and "Transient Power Capability of Zener Diodes", document number AN784/D. All application notes are available through the Literature Distribution Center or via our website at http://www.onsemi.com.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

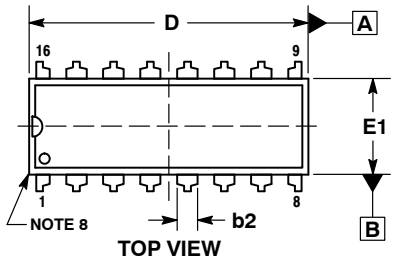
ON Semiconductor®

PDIP−16
CASE 648−08
ISSUE V

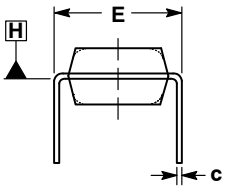
DATE 22 APR 2015



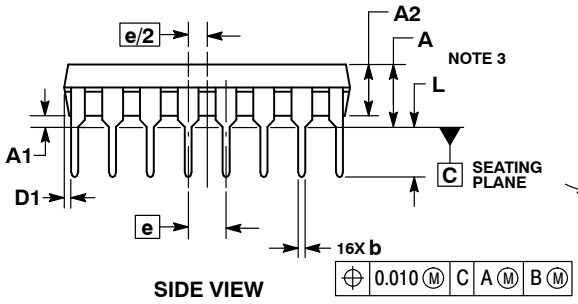
SCALE 1:1



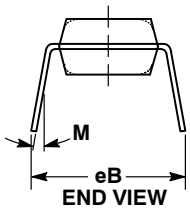
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



END VIEW
NOTE 6

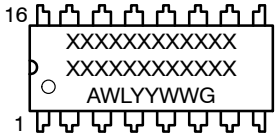
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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