

## DC to 200 MHz Inverting 1:2 Fanout Buffer

### Features

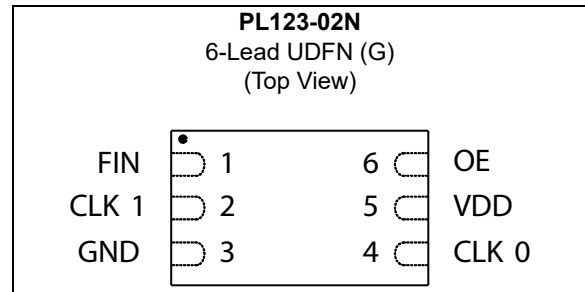
- Supports 3.3V, 2.5V, and 1.8V Power Supplies
- Frequency Support:
  - 3.3V Supplies: DC to 200 MHz
  - 2.5V Supplies: DC to 150 MHz
  - 1.8V Supplies: DC to 100 MHz
- Output Enable (OE) Pin
- LVCMOS Input/Output Accepts SST and non-SST Clock Signals
- Operating Temperature Range from -40°C to +85°C
- Available in a Space-Saving 6-Lead UDFN GREEN/RoHS-Compliant Package

### General Description

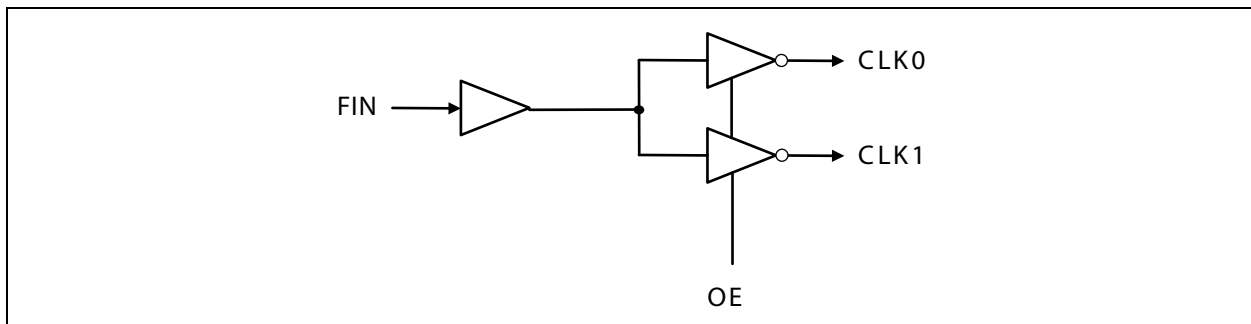
The PL123-02N is a low-cost general purpose 1:2 inverting LVCMOS fanout buffer. An output enable (OE) pin is available to enable the outputs or disable them into an active-low state. When the outputs are disabled, the IC consumes less than 5  $\mu$ A of power. The OE pin incorporates a pull-up resistor, giving a default condition of logic "1".

The input and outputs are LVCMOS levels and operate up to 200 MHz. Input signals with Spread Spectrum Modulation can also be used. The spread spectrum modulation will not be affected by the PL123-02N as the signal passes through the IC. A space-saving 6-lead UDFN package enables designs that require minimal board area.

### Package Type



### Block Diagram



# PL123-02N

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Supply Voltage Range ( $V_{DD}$ ).....	-0.5V to +4.6V
Input Voltage Range ( $V_I$ ).....	-0.5V to $V_{DD} + 0.5V$
Output Voltage Range ( $V_O$ ).....	-0.5V to $V_{DD} + 0.5V$
Soldering Temperature (GREEN Package).....	+260°C
Storage Temperature ( $T_S$ ).....	-65°C to +150°C
Ambient Operating Temperature (Note 1).....	-40°C to +85°C

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:** Operating temperature is guaranteed by design. Parts are tested to commercial grade only.

### AC SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Frequency (Note 1)	$f_{IN}$	DC	—	200	MHz	@ $V_{DD} = 3.3V$ , 15 pF load
			—	150		@ $V_{DD} = 2.5V$ , 15 pF load
			—	100		@ $V_{DD} = 1.8V$ , 15 pF load
Input Voltage Low	$V_{IL}$	—	—	$0.3 \times V_{DD}$	V	—
Input Voltage High	$V_{IH}$	$0.7 \times V_{DD}$	—	—	V	—
Output Enable Time	$t_{EN}$	—	—	2	ms	$T_A = +25^\circ C$ , 15 pF load
Output Rise Time	$t_r$	—	2.0	3.0	ns	15 pF load, 10/90% $V_{DD}$ , 3.3V
Output Fall Time	$t_f$	—	2.0	3.0	ns	15 pF load, 10/90% $V_{DD}$ , 3.3V
Duty Cycle	—	—	—	—	%	Dependent on input duty cycle

**Note 1:** Higher frequencies may be achieved for lower capacitive loads.

### DC SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Current, Dynamic, with Loaded CMOS Output	$I_{DD}$	—	0.8	—	mA	@ $V_{DD} = 3.3V$ , 32 kHz, 15 pF load
		—	0.6	—	mA	@ $V_{DD} = 2.5V$ , 32 kHz, 15 pF load
		—	0.4	—	mA	@ $V_{DD} = 1.8V$ , 32 kHz, 15 pF load
Supply Current, Dynamic, with Loaded Outputs	$I_{DD}$	—	—	5	$\mu A$	When OE = 0
Operating Voltage	$V_{DD}$	1.62	—	3.63	V	—
Output Low Voltage	$V_{OL}$	—	—	0.4	V	$I_{OL} = 4 mA$
Output High Voltage	$V_{OH}$	$V_{DD} - 0.4$	—	—	V	$I_{OH} = -4 mA$
Output Current	$I_{OSD}$	8	—	—	mA	$V_{OL} = 0.4V$ , $V_{OH} = 2.4V$

## 2.0 PIN DESCRIPTION

The descriptions of the pins are listed in [Table 2-1](#).

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Pin Type	Description
1	FIN	I	Reference input pin.
2	CLK1	O	Clock output (inverted).
3	GND	P	GND connection.
4	CLK0	O	Clock output (inverted).
5	VDD	P	VDD connection.
6	OE	I	Output Enable (OE) input. Outputs are enabled when set high. Outputs are in active-low mode when set low.

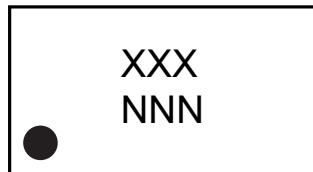
# PL123-02N

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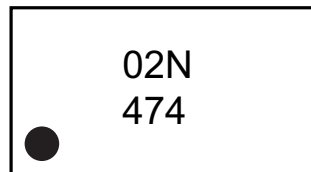
## 3.0 PACKAGING INFORMATION

### 3.1 Package Marking Information

6-Lead UDFN\*



Example

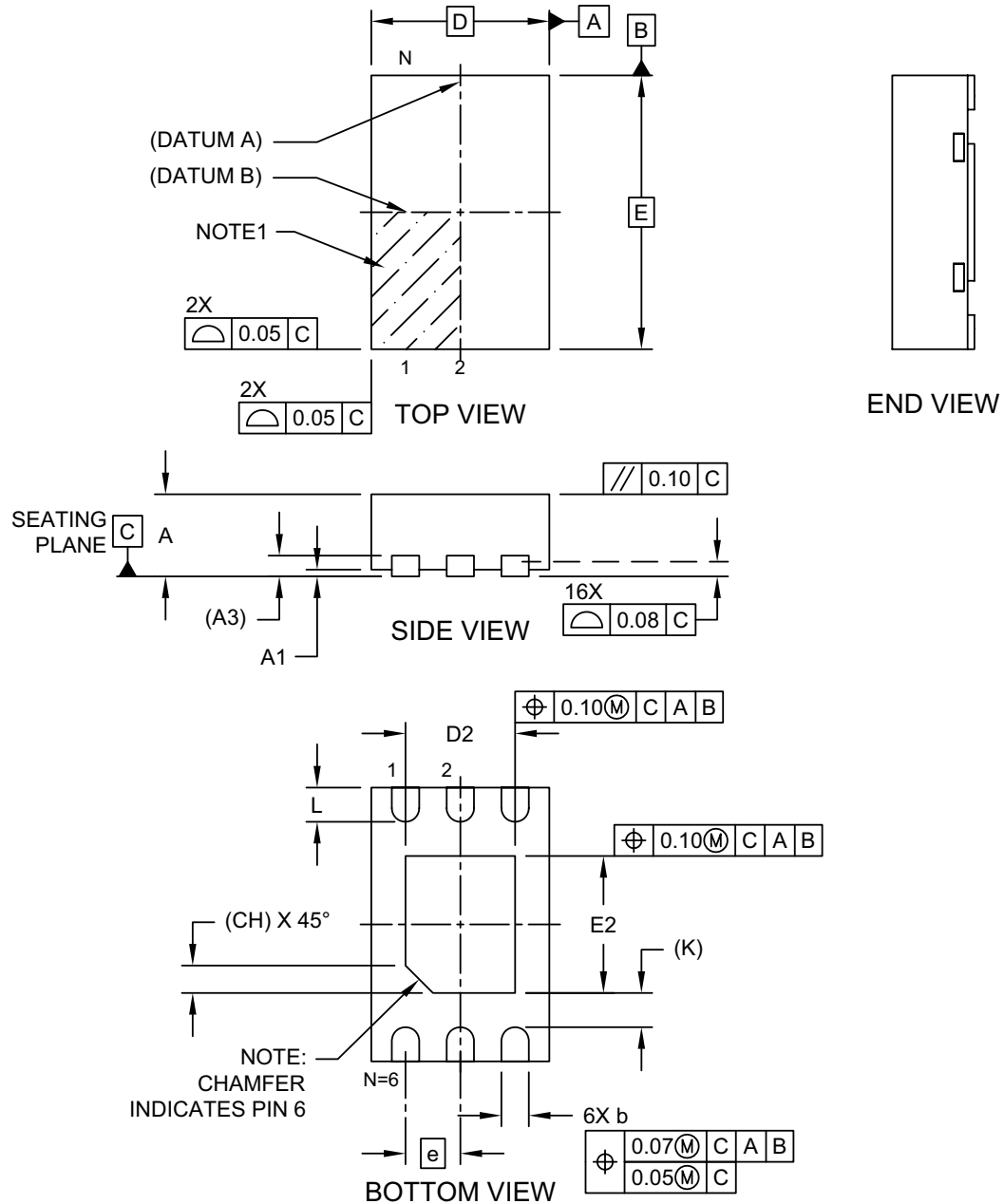


<b>Legend:</b>	XX...X	Product code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	(e3)	This package is Pb-free. The Pb-free JEDEC designator ( ) can be found on the outer packaging for this package. (e3)
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar ( ) and/or Overbar ( ) symbol may not be to scale.	

## 6-Lead UDFN Package Outline and Recommended Land Pattern

### 6-Lead Ultra Thin Dual Flat, No Lead Package (HXA) - 1.3x2x0.60 mm Body [UDFN] Micrel Legacy Package TDFN2013-6LD-PL-1

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

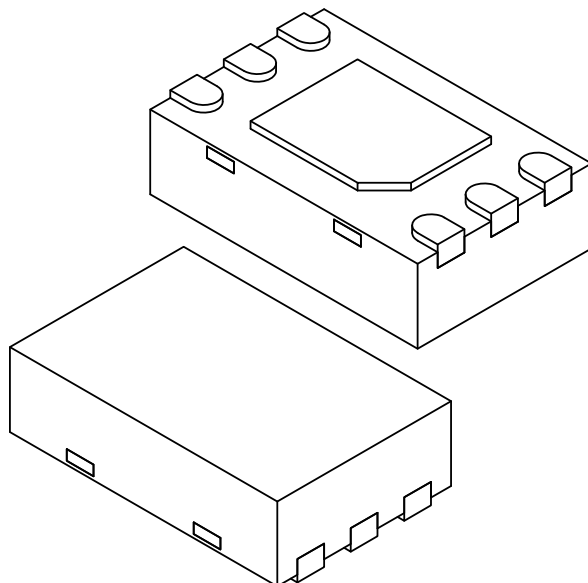


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## 6-Lead Ultra Thin Dual Flat, No Lead Package (HXA) - 1.3x2x0.60 mm Body [UDFN] Micrel Legacy Package TDFN2013-6LD-PL-1

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	6		
Pitch	e	0.40 BSC		
Overall Height	A	0.50	0.55	0.60
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3	0.152 REF		
Overall Length	D	1.30 BSC		
Exposed Pad Length	D2	0.75	0.80	0.85
Overall Width	E	2.00 BSC		
Exposed Pad Width	E2	0.95	1.00	1.05
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.20	0.25	0.30
Exposed Pad Index Chamfer	CH	0.20 REF		
Terminal-to-Exposed-Pad	K	0.25 REF		

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

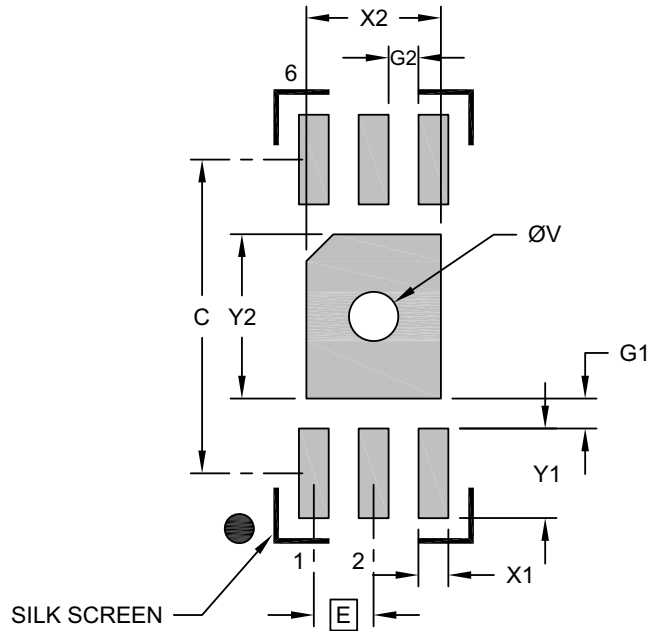
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1245 Rev B Sheet 2 of 2

## 6-Lead Ultra Thin Dual Flat, No Lead Package (HXA) - 1.3x2x0.60 mm Body [UDFN] Micrel Legacy Package TDFN2013-6LD-PL-1

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.40 BSC		
Optional Center Pad Width	X2			0.90
Optional Center Pad Length	Y2			1.10
Contact Pad Spacing	C		2.10	
Contact Pad Width (Xnn)	X1			0.20
Contact Pad Length (Xnn)	Y1			0.60
Contact Pad to Center Pad (Xnn)	G1	0.20		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	

**Notes:**

- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
- For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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NOTES:



## APPENDIX A: REVISION HISTORY

### Revision A (August 2020)

- Converted Micrel document PL123-02N to Microchip data sheet template DS20006402A.
- Minor grammatical text changes throughout.

# PL123-02N

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>X</u>	<u>X</u>	<u>-X</u>	<b>Examples:</b>
Device	Package	Temperature Range	Media Type	
<b>Device:</b>	PL123-02N: DC to 200 MHz Inverting 1:2 Fanout Buffer			a) PL123-02NGC: PL123-02N, 6-Lead UDFN, 0°C to +70°C Temperature Range, 20/Bag b) PL123-02NGC-R: PL123-02N, 6-Lead UDFN, 0°C to +70°C Temperature Range, 3,000/Reel c) PL123-02NGI: PL123-02N, 6-Lead UDFN, -40°C to +85°C Temperature Range, 20/Bag d) PL123-02NGI-R: PL123-02N, 6-Lead UDFN, -40°C to +85°C Temperature Range, 3,000/Reel  <b>Note 1:</b> Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
<b>Package:</b>	G	=	6-Lead UDFN	
<b>Temperature Range:</b>	C	=	0°C to +70°C	
	I	=	-40°C to +85°C	
<b>Media Type:</b>	(blank)	=	20/Bag	
	R	=	3,000/Reel	

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NOTES:

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