PRODUCT/PROCESS CHANGE NOTIFICATION

PCN MMS-MMY/14/8467
Dated 07 May 2014

M24C32, 32-Kbit I2C Bus EEPROM Industrial grade / SO8N, TSSOP8 & UFDFPN8 packages Redesign and upgrade to the CMOSF8H+ process technology

Table 1. Change Implementation Schedule

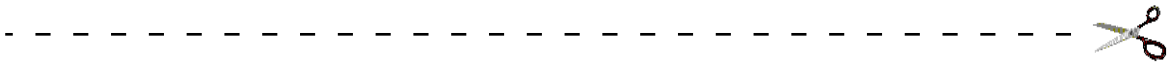
Forecasted implementation date for change	30-Apr-2014
Forecasted availability date of samples for customer	30-May-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	30-Apr-2014
Estimated date of changed product first shipment	06-Aug-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	M24C32 products SO8N, TSSOP8 & UFDFPN8 (industri.)
Type of change	Waferfab process change
Reason for change	Line up to state-of-the-art of process
Description of the change	Redesign and upgrade to the new CMOSF8H+ process technology.
Change Product Identification	Process Technology identifier "T" for CMOSF8H+
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN MMS-MMY/14/8467**
Please sign and return to STMicroelectronics Sales Office	**Dated 07 May 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

.....

.....

.....

.....

.....

.....

.....

.....

DOCUMENT APPROVAL

Name	Function
Leduc, Hubert	Marketing Manager
Rodrigues, Benoit	Product Manager
Pavano, Rita	Q.A. Manager

PRODUCT / PROCESS CHANGE NOTIFICATION

M24C32, 32-Kbit I2C Bus EEPROM
Industrial grade / SO8N, TSSOP8 & UFDFPN8 packages
Redesign and upgrade to the CMOSF8H+ process technology

What is the change?

The **M24C32**, 32-Kbit serial I²C bus EEPROM product family for Industrial grade, assembled in SO8N TSSOP8 & UFDFPN8 packages, currently produced using the CMOSF8H process technology at ST Rousset (France) 8" wafer diffusion plant, has been **redesigned** and will be **upgraded** to the **CMOSF8H+** process technology at the same wafer diffusion plant.

The CMOSF8H+ is closely derived from CMOSF8H (already used for production of densities ranging from 32 Kb to 2 Mb), with a more compact layout, in order to achieve competitive die size.

This upgraded version in CMOSF8H+ allows offering UFDFPN5 (1.4 mm x 1.7 mm while UFDFPN8 is 2 mm x 3 mm).

The new M24C32 in CMOSF8H+ version is functionally compatible with the current CMOSF8H version as per datasheet rev. 21 – July 2012, attached.

Following parameters will be updated in revised datasheet rev. 22:

- Absolute maximum rating: V_{ESD} electrostatic pulse Human Body model:
  - Max 2000 V

Concurrent to this change, the M24C32 in CMOSF8H+ in SO8N, TSSOP8 & UFDFPN8 will be assembled with 0.8 mil Copper wire.

Why?

The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, the qualification of the M24C32 in the new CMOSF8H+ process technology will increase the production capacity throughput and consequently improve the service to our customers.

When?

The production of the upgraded M24C32 with the new CMOSF8H+ will ramp up from June 2014 and shipments can start from August 2014 onward (or earlier upon customer approval).

How will the change be qualified?

The new version of the M24C32 in CMOSF8H+ in SO8N package will be qualified using the standard ST Microelectronics Corporate Procedures for Quality & Reliability.

The **Qualification Report QRMMY1310** is available and included inside this document.

What is the impact of the change?

- Form: Marking change (see **Device marking** paragraph)

- Fit: No change

- Function:

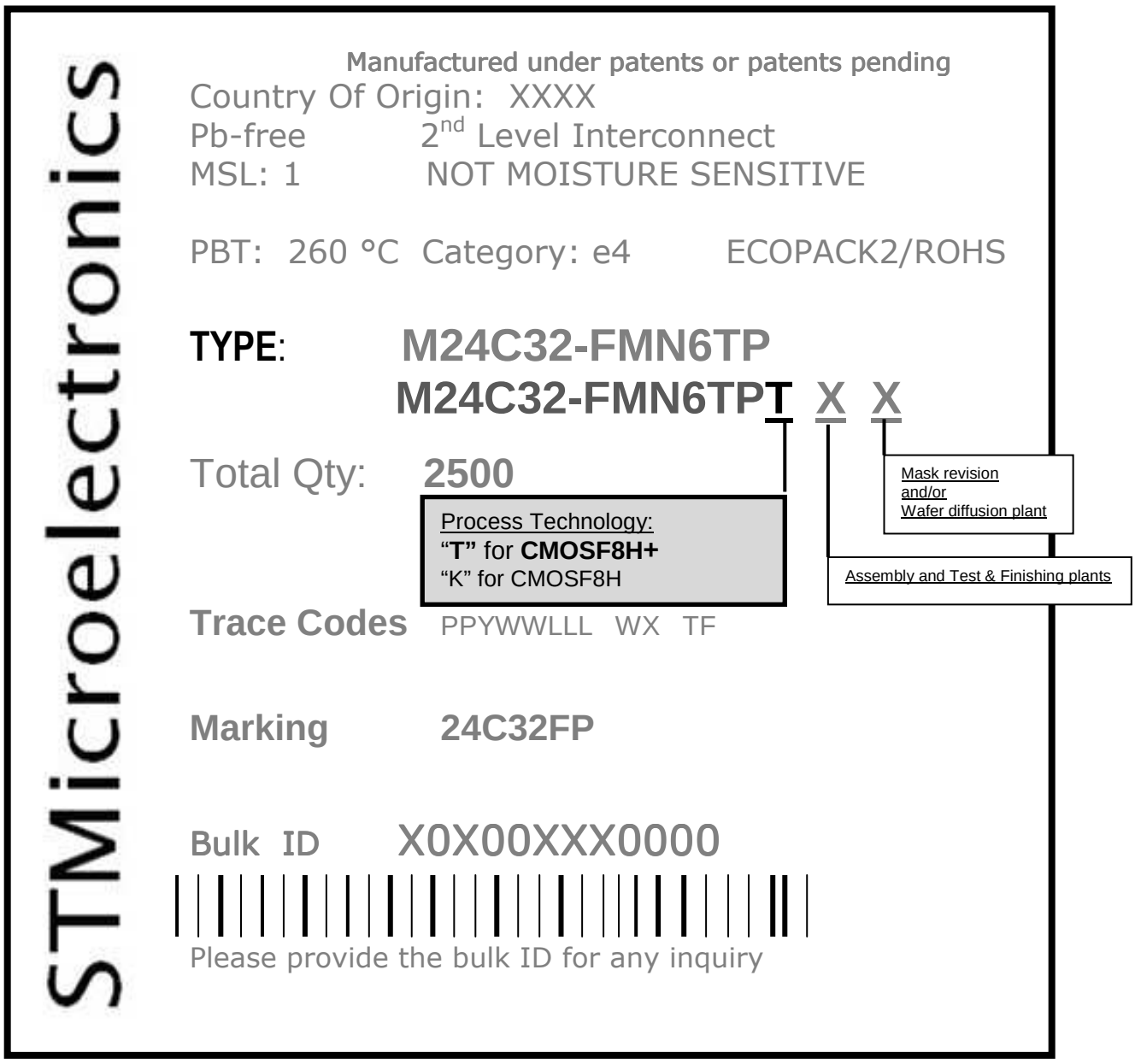
- Change on Absolute maximum rating **V_{ESD} HBM**

How can the change be seen?

- ***BOX LABEL MARKING***

On the BOX LABEL MARKING, the difference is visible inside the **Finished Good Part Number**: the **process technology** identifier is "**T**" for the **upgraded version** in **CMOSF8H+**, this identifier being "K" for the current version in CMOSF8H.

➔ *Example for M24C32-FMN6TP*



How can the change be seen?

- DEVICE MARKING

For the **SO8N**, the difference is visible inside the **trace code** PYWWT where the last digit T for Process Technology is "**T**" for the **upgraded version** in **CMOSF8H+**, this digit being "K" for current CMOSF8H version.

	Upgraded CMOSF8H+	Current CMOSF8H
Example: M24C32-RMN6TP	24C32RP *PYWW***T**	24C32RP *PYWW***K**

	Upgraded CMOSF8H+	Current CMOSF8H
TSSOP8 Example: M24C32-RDW6TP	O 432R**T** *PYWW*	O 432R**K** *PYWW*

For the **UFDFPN8** package, the difference is visible inside the product name.
Example for M24C32-FMC6TG: **upgraded version** in **CMOSF8H+** is **4EFT**, current version being 432D.

	Upgraded CMOSF8H+	Current CMOSF8H
UFDFPN8 Example: M24C32-FMC6TG	O 4**EFT** *PYWW*	O 432F *PYWW*

Appendix A- Product Change Information

Product family / Commercial products:	M24C32 products family assembled in SO8N, TSSOP8 & UFDFPN8 packages / Industrial grade
Customer(s):	All
Type of change:	Wafer fab process technology change
Reason for the change:	Line up to state-of-the-art of process
Description of the change:	Redesign and upgrade to the new CMOSF8H+ Process technology.
Forecast date of the change: (Notification to customer)	Week 18 / 2014
Forecast date of Qualification samples availability for customer(s):	See details in APPENDIX B
Forecast date for the internal STMicroelectronics change, Qualification Report availability:	The **Qualification Report QRMMY1310 is** available and included inside this document.
Marking to identify the changed product:	Process Technology identifier "**T"** for CMOSF8H+
Description of the qualification program:	Standard ST Microelectronics Corporate Procedures for Quality and Reliability
Product Line(s) and/or Part Number(s):	See Appendix B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 31 / 2014

Appendix B: Concerned Commercial Part Numbers:

Commercial Part Numbers	Package	Samples availability
M24C32-FDW6TP	TSSOP8	Week 20 / 2014
M24C32-FMC6TG	UFDFPN8	Available
M24C32-FMN6TP	SO8	Available
M24C32-RDW6TP	TSSOP8	Week 22 / 2014
M24C32-RMN6P	SO8	No samples in tube
M24C32-RMN6TP	SO8	Week 21 / 2014
M24C32-WDW6TP	TSSOP8	Week 22 / 2014
M24C32-WMN6P	SO8	No samples in tube
M24C32-WMN6TP	SO8	Week 22 / 2014

(*) Following product line rationalization, we recommend customer to use **–R** version (1.8 V – 5.5 V) when *–W* (2.5 V – 5.5 V) is used.
For instance, **M24C32-RDW6TP should be preferred** to *M24C32-WDW6TP*.

Appendix C: Qualification Report:

See following pages

QRMMY1310
Qualification report

New design / M24C32-F M24C32-R M24C32-W using the CMOSF8H+ technology at the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M24C32-FDW6TP M24C32-FMC6TG M24C32-RDW6TP M24C32-RMN6P M24C32-RMN6TP M24C32-WDW6TP M24C32-WMN6P M24C32-WMN6TP
Product description	32-Kbit serial I²C bus EEPROM
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H+
Wafer fabrication location	RS8F - ST Rousset 8”, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore subcontractor Ardentec, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
	Subcon Amkor, Philippines	Subcon Amkor, Philippines
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
	Subcon Amkor, Philippines	Subcon Amkor, Philippines
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines
	Subcon Amkor, Philippines	Subcon Amkor, Philippines
UFDFPN5 (MLP5) 1.7 x 1.4 mm	ST Calamba, Philippines	ST Calamba, Philippines

Reliability / Qualification assessment: All available data are positive

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new design M24C32-F, M24C32-R and M24C32-W using the CMOSF8H+ silicon process technology at the ST Rousset 8” diffusion fab.

The CMOSF8H+ is closely derived from CMOSF8H silicon process technology (already used for production of EEPROM densities ranging from 32 Kb to 2 Mb), with a more compact layout, in order to achieve a competitive die size.

The CMOSF8H+ technology is already qualified in the ST Rousset 8” fab using M24C16 as driver product.

The voltage and temperature ranges covered by this document are:

- 2.5 to 5.5 V at –40 to 85 °C for -W devices
- 1.8 to 5.5 V at –40 to 85 °C for -R devices
- 1.7 to 5.5 V at –40 to 85 °C for -F devices

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion plant.

1.2 Conclusion

The new design M24C32-F, M24C32-R and M24C32-W using the CMOSF8H+ silicon process technology at the ST Rousset 8” diffusion fab has passed all ESD and Latch-up requirements. Reliability trials are still on going, and all available data are positive.

Refer to *Section 3: Reliability test results* for details on the test results.

2 Device characteristics

Device description

The M24C32-x devices are I^2C-compatible electrically erasable programmable memories (EEPROM). They are organized as 4 Kb × 8 bits respectively.

The device behaves as a slave in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a Start condition, generated by the bus master. The Start condition is followed by a device select code and a Read/Write bit (RW) terminated by an acknowledge bit.

When writing data to the memory, the device inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy.

The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The CMOSF8H+ process technology has been qualified on 3 lots using the driver product M24C16 (refer to qualification report QRMMY1126).

The M24C32 is designed with the similar architecture and same technology as the driver product M24C16. Qualification of M24C32 benefits from the family approach (1 lot).

The product vehicles used for the die qualification are presented in *Table 3*.

Table 3. Product vehicles used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24C16	CMOSF8H+	ST Rousset 8”	CDIP8	Engineering assy (1)
M24C32 (2)	CMOSF8H+	ST Rousset 8”	CDIP8	Engineering assy (1)

1. CDIP8 is an engineering ceramic package used only for die-oriented reliability trials.
2. Qualification on 3 lots using the driver product M24C16 - Qualification of M24C32 benefits from the family approach (1 lot).

The product vehicle used for package qualification is presented in *Table 4*.

Table 4. Product vehicles used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24C32 (1)	CMOSF8H+	ST Rousset 8”	SO8N	ST Shenzhen / Subcon Amkor
			TSSOP8	ST Shenzhen / Subcon Amkor
			UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba / Subcon Amkor
			UFDFPN5 (MLP5) 1.7 x 1.4 mm	ST Calamba

1. Qualification on 3 lots using the driver product M24C16 - Qualification of M24C32 benefits from the family approach (1 lot).

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests.
- in *Table 6* for SO8N ST Shenzhen / subcontractor Amkor package-oriented tests.
- in *Table 7* for TSSOP8 ST Shenzhen / subcontractor Amkor package-oriented tests.
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba / subcontractor Amkor package-oriented tests.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)

Test	Test short description (1)								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24C16			M24C32(2)
						Lot 1	Lot 2	Lot 3	Lot 1
EDR	High temperature operating life after endurance								
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTOL 150 °C, 6V	80	1	168 hrs	0/80	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80	0/80
					1008 hrs	0/80	0/80	0/80	0/80
	Data retention after endurance								
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTSL at 150 °C	80	1	168 hrs	0/80	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80	0/80
					1008 hrs	0/80	0/80	0/80	0/80
LTOL	Low temperature operating life								
	JESD22-A108	–40 °C, 6 V	80	1	168 hrs	0/80	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80	0/80
					1008 hrs	0/80	0/80	0/80	0/80
HTSL	High temperature storage life								
	JESD22-A103	Retention bake at 200 °C	80	1	168 hrs	0/80	0/80	0/80	0/80
					504 hrs	0/80	0/80	0/80	0/80
					1008 hrs	0/80	0/80	0/80	0/80
WEB	Program/erase endurance cycling + bake								
	Internal spec.	5 million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	1	5 million cycles / 48 hrs	0/80(3)	0/80(3)	0/80(3)	0/80 (3)
ESD HBM	Electrostatic discharge (human body model)								
	AEC-Q100-002 JEDEC JS-001-2012	C = 100 pF, R= 1500 Ω	27	1	N/A	Pass 3000 V	Pass 3000 V	Pass 3000 V	Pass 2000 V

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package) (continued)

Test	Test short description [1]								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24C16			M24C32[2]
						Lot 1	Lot 2	Lot 3	Lot 1
ESD MM	Electrostatic discharge (machine model)								
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	12	1	N/A	Pass 200 V	Pass 200 V	Pass 200 V	Pass 150 V
LU	Latch-up (current injection and overvoltage stress)								
	AEC-Q100-004 JESD78B	At 150 °C	6	1	N/A	Class II - Level A	Class II - Level A	Class II - Level A	Class II - Level A

1. See *Table 9: List of terms* for definitions of abbreviations.
2. Qualification on 3 lots using the driver product M24C16 - Qualification of M24C32 benefits from the family approach (1 lot).
3. First rejects after 10 million cycles.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen & subcontractor Amkor)

Test	Test short description[1]								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24C16			M24C32[2]
						Lot 1	Lot 2	Lot 3	Lot 1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	1	N/A	0/1145	0/1145	0/1145	Results FC W23
THB[3]	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	Results FC W31
					2008 hrs	0/80	0/80	0/80	Results FC W38
TC[3]	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +150 °C	80	1	1000 cycles	0/80	0/80	0/80	Results FC W28
TMSK[3]	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25	0/25	0/25	Results FC W28
AC[3]	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80	0/80	0/80	Results FC W28
HTSL[3]	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	Results FC W31
					2008 hrs	0/80	0/80	0/80	Results FC W38
ELFR[3]	Early life failure rate								
	AEC-Q100-008	HTOL at 150 °C, 6V	800	1	48 hrs	0/800	0/800	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	PASS > 1500V	-	-	Results FC W25

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the driver product M24C16 - Qualification of M24C32 benefits from the family approach (1 lot).
3. THB-, TC-, TMSK-, AC-, HTSL and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen & subcontractor Amkor)

Test	Test short description[1]								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24C16			M24C32[2]
						Lot 1	Lot 2	Lot 3	Lot 1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	1	N/A	0/1145	0/1145	0/1145	Results FC W23
THB[3]	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	Results FC W31
					2008 hrs	0/80	0/80	0/80	Results FC W38
TC[3]	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +150 °C	80	1	1000 cycles	0/80	0/80	0/80	Results FC W28
TMSK[3]	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25	0/25	0/25	Results FC W28
AC[3]	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80	0/80	0/80	Results FC W28
HTSL[3]	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	Results FC W31
					2008 hrs	0/80	0/80	0/80	Results FC W38
ELFR[3]	Early life failure rate								
	AEC-Q100-008	HTOL at 150 °C, 6V	800	1	48 hrs	0/800	0/800	0/800	-
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	PASS > 1500V	-	-	Results FC W25

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the driver product M24C16 - Qualification of M24C32 benefits from the family approach (1 lot).
3. THB-, TC-, TMSK-, AC-, HTSL and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba & subcontractor Amkor)

Test	Test short description[1]								
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size			
						M24C16			M24C32[2]
						Lot 1	Lot 2	Lot 3	Lot 1
PC	Preconditioning: moisture sensitivity level 1								
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	1	N/A	0/345	0/345	0/345	Results FC W26
THB[3]	Temperature humidity bias								
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80	0/80	0/80	Results FC W34
					2008 hrs	0/80	0/80	0/80	Results FC W41
TC[3]	Temperature cycling								
	AEC-Q100-JESD22-A104	–65 °C / +150 °C	80	1	1000 cycles	0/80	0/80	0/80	Results FC W31
TMSK[3]	Thermal shocks								
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25	0/25	0/25	Results FC W31
AC[3]	Autoclave (pressure pot)								
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80	0/80	0/80	Results FC W31
HTSL[3]	High temperature storage life								
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80	0/80	0/80	Results FC W34
					2008 hrs	0/80	0/80	0/80	Results FC W41
ESD CDM	Electrostatic discharge (charge device model)								
	AEC-Q100-011 JESD22-C101	Field induced charging method	18	1	N/A	PASS > 1500V	-	-	Results FC W28

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Qualification on 3 lots using the driver product M24C16 - Qualification of M24C32 benefits from the family approach (1 lot).
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
24-Apr-2014	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

M24C32-W M24C32-R M24C32-F M24C32-X M24C32-DF

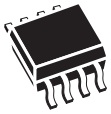
32-Kbit serial I²C bus EEPROM

Datasheet – production data

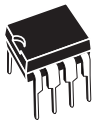
Features

- Compatible with all I²C bus modes:
  - 1 MHz
  - 400 kHz
  - 100 kHz
- Memory array:
  - 32 Kbit (4 Kbytes) of EEPROM
  - Page size: 32 bytes
  - Additional Write lockable page (M24C32-D order codes)
- Single supply voltage:
  - 1.7 V to 5.5 V over –40 °C / +85 °C
  - 1.6 V to 5.5 V over –20 °C / +85 °C
- Write:
  - Byte Write within 5 ms (10 ms when V_{CC} = 1.6 V)
  - Page Write within 5 ms (10 ms when V_{CC} = 1.6 V)
- Random and sequential Read modes
- Write protect of the whole memory array
- Enhanced ESD/Latch-Up protection
- More than 4 million Write cycles
- More than 200-year data retention
- Packages:
  - RoHS compliant and halogen-free (ECOPACK®)

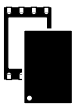
TSSOP8 (DW)
169 mil width



SO8 (MN)
150 mil width



PDIP8 (BN)



UFDFPN8
(MB, MC)

Contents

List of tables

List of figures

1 Description

The M24C32 is a 32-Kbit I^2C-compatible EEPROM (Electrically Erasable PROgrammable Memory) organized as 4 K × 8 bits.

The M24C32-W can operate with a supply voltage from 2.5 V to 5.5 V, the M24C32-R can operate with a supply voltage from 1.8 V to 5.5 V, and the M24C32-F and M24C32-DF can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C / +85 °C; while the M24C32-X can operate with a supply voltage from 1.6 V to 5.5 V over an ambient temperature range of -20 °C / +85 °C.

The M24C32-D offers an additional page, named the Identification Page (32 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

Figure 1. Logic diagram

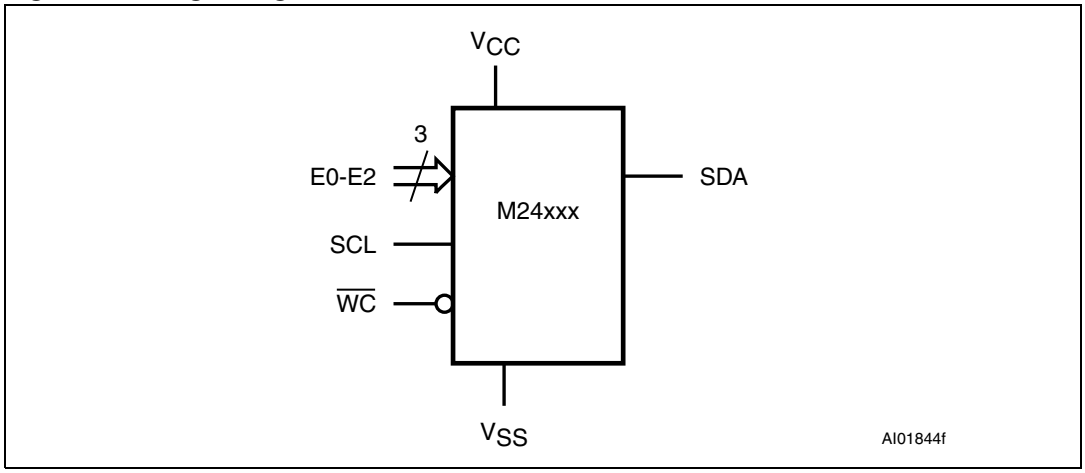
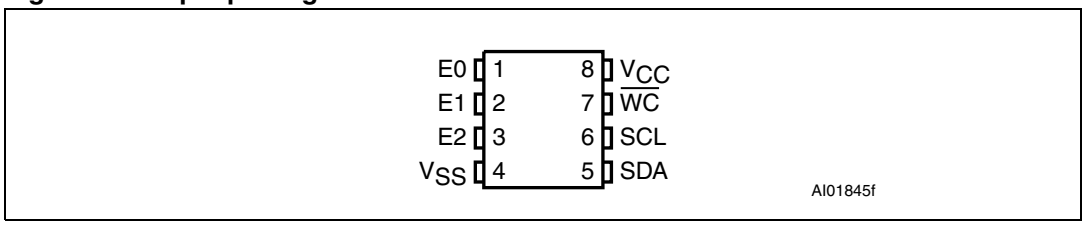


Table 1. Signal names

Signal name	Function	Direction
E2, E1, E0	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
$\overline{WC}$	Write Control	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. 8-pin package connections



1. See *Section 9: Package mechanical data* for package dimensions, and how to identify pin 1.

2 Signal description

2.1 Serial Clock (SCL)

The signal applied on the SCL input is used to strobe the data available on SDA(in) and to output the data on SDA(out).

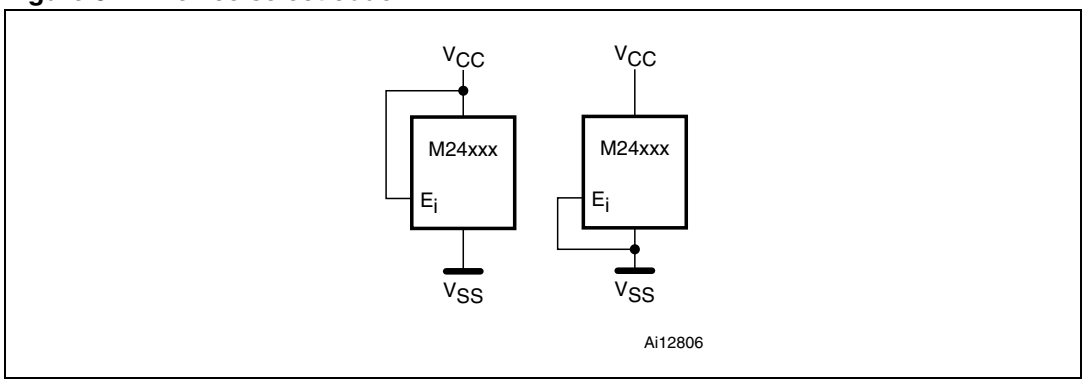
2.2 Serial Data (SDA)

SDA is an input/output used to transfer data in or data out of the device. SDA(out) is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull-up resistor must be connected from Serial Data (SDA) to V_{CC} (*Figure 11* indicates how to calculate the value of the pull-up resistor).

2.3 Chip Enable (E2, E1, E0)

(E2,E1,E0) input signals are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code (see *Table 2*). These inputs must be tied to V_{CC} or V_{SS}, as shown in *Figure 3*. When not connected (left floating), these inputs are read as low (0).

Figure 3. Device select code



2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven high. Write operations are enabled when Write Control ($\overline{WC}$) is either driven low or left floating.

When Write Control ($\overline{WC}$) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} (ground)

V_{SS} is the reference for the V_{CC} supply voltage.

2.6 Supply voltage (V_{CC})

2.6.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see Operating conditions in *Section 8: DC and AC parameters)*. In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_W).

2.6.2 Power-up conditions

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters)* and the rise time must not vary faster than 1 V/µs.

2.6.3 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included.

At power-up, the device does not respond to any instruction until V_{CC} has reached the internal reset threshold voltage. This threshold is lower than the minimum V_{CC} operating voltage (see Operating conditions in *Section 8: DC and AC parameters*). When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode; however, the device must not be accessed until V_{CC} reaches a valid and stable DC voltage within the specified [V_{CC}(min), V_{CC}(max)] range (see Operating conditions in *Section 8: DC and AC parameters*).

In a similar way, during power-down (continuous decrease in V_{CC}), the device must not be accessed when V_{CC} drops below V_{CC}(min). When V_{CC} drops below the internal reset threshold voltage, the device stops responding to any instruction sent to it.

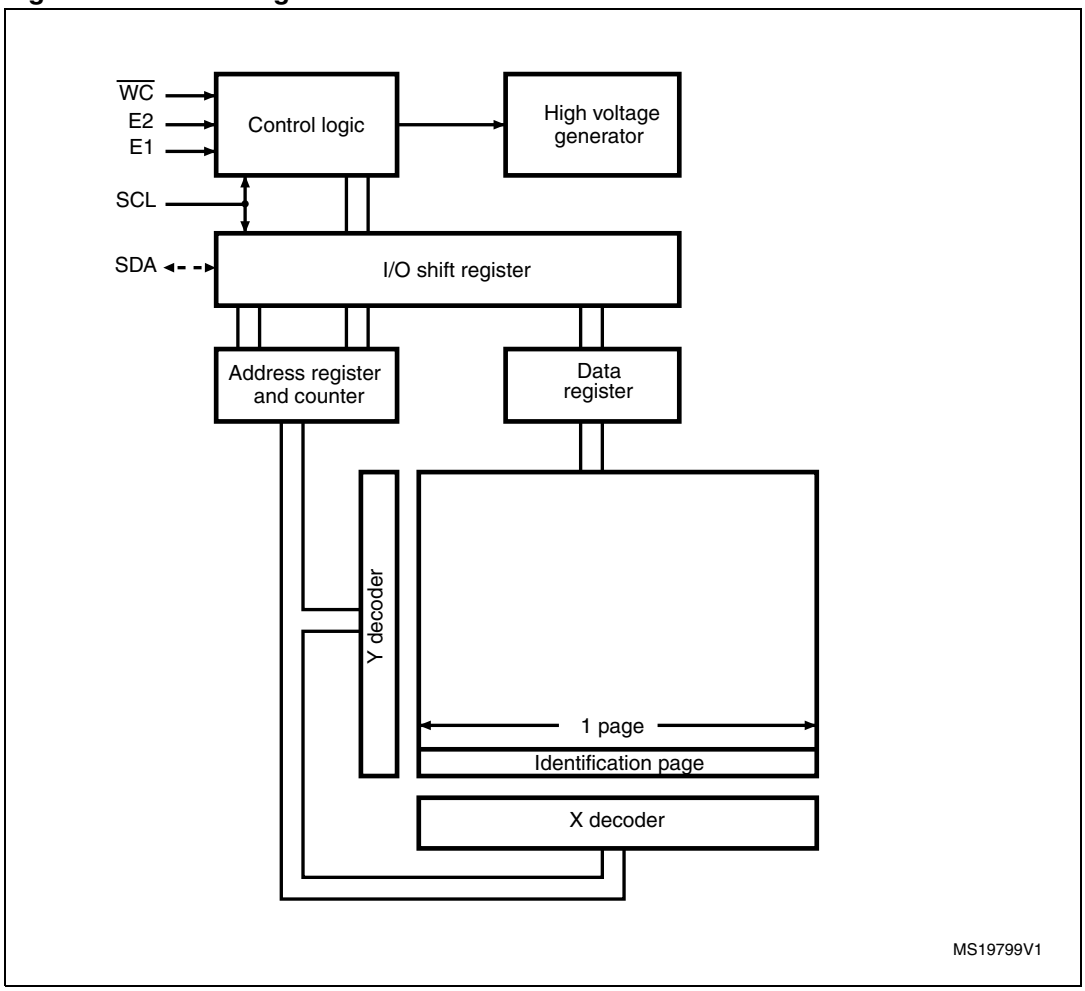
2.6.4 Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that there is no internal write cycle in progress).

3 Memory organization

The memory is organized as shown below.

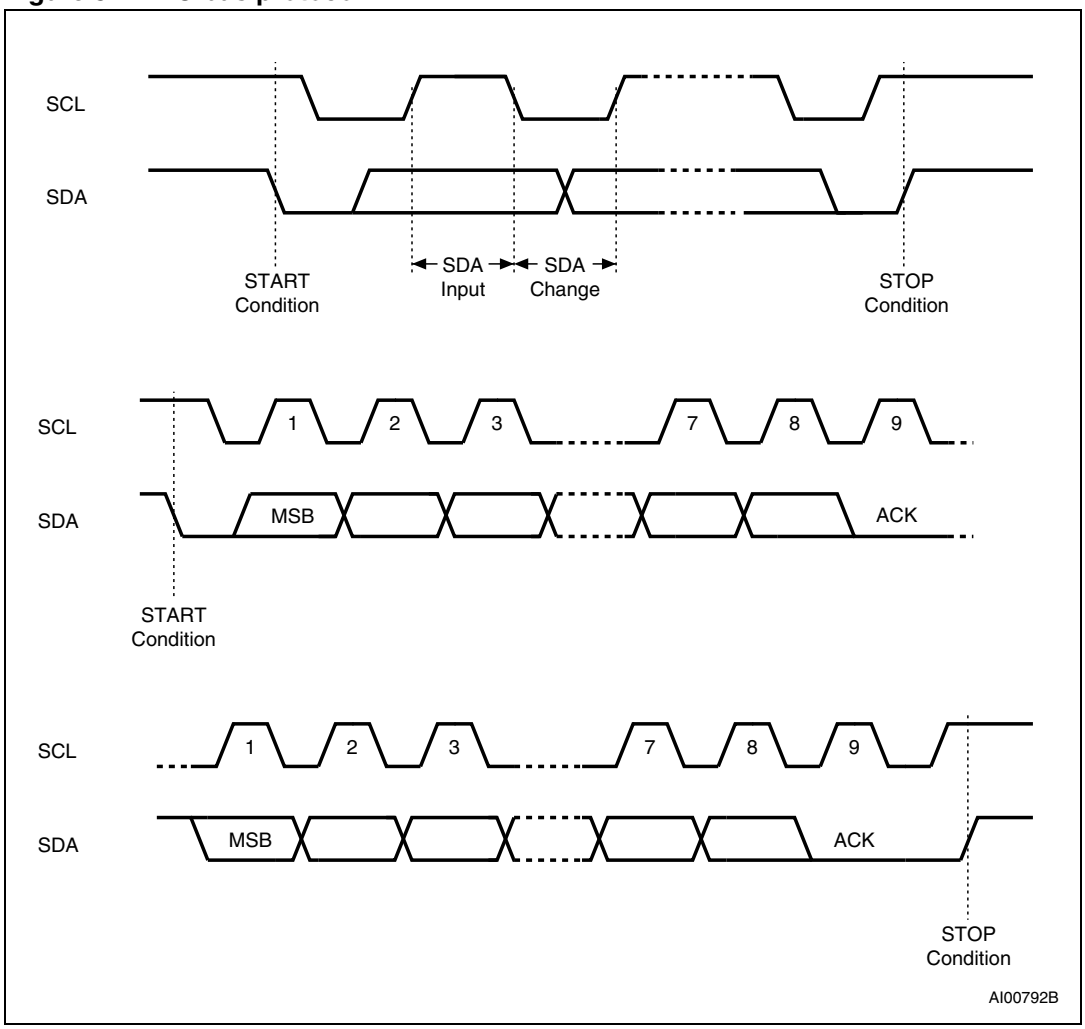
Figure 4. Block diagram



4 Device operation

The device supports the I²C protocol. This is summarized in *Figure 5*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The device is always a slave in all communications.

Figure 5. I²C bus protocol



4.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer instruction. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition.

4.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read instruction that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode.

A Stop condition at the end of a Write instruction triggers the internal Write cycle.

4.3 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

4.4 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9^{th} clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

4.5 Device addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), most significant bit first).

Table 2. Device select code

	Device type identifier(1)				Chip Enable address(2)			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code when addressing the memory array	1	0	1	0	E2	E1	E0	RW
Device select code when accessing the Identification page	1	0	1	1	E2	E1	E0	RW

1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared .

When the device select code is received, the device only responds if the Chip Enable address is the same as the value on its Chip Enable E2,E1,E0 inputs.

The 8th bit is the Read/Write bit (RW). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, the device deselects itself from the bus, and goes into Standby mode.

5 Instructions

5.1 Write operations

Following a Start condition the bus master sends a device select code with the R/$\overline{W}$ bit (R$\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 6*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Table 3. Most significant address byte

A15	A14	A13	A12	A11	A10	A9	A8

Table 4. Least significant address byte

A7	A6	A5	A4	A3	A2	A1	A0

When the bus master generates a Stop condition immediately after a data byte Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal Write cycle t_W is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition and the successful completion of an internal Write cycle (t_W), the device internal address counter is automatically incremented to point to the next byte after the last modified byte.

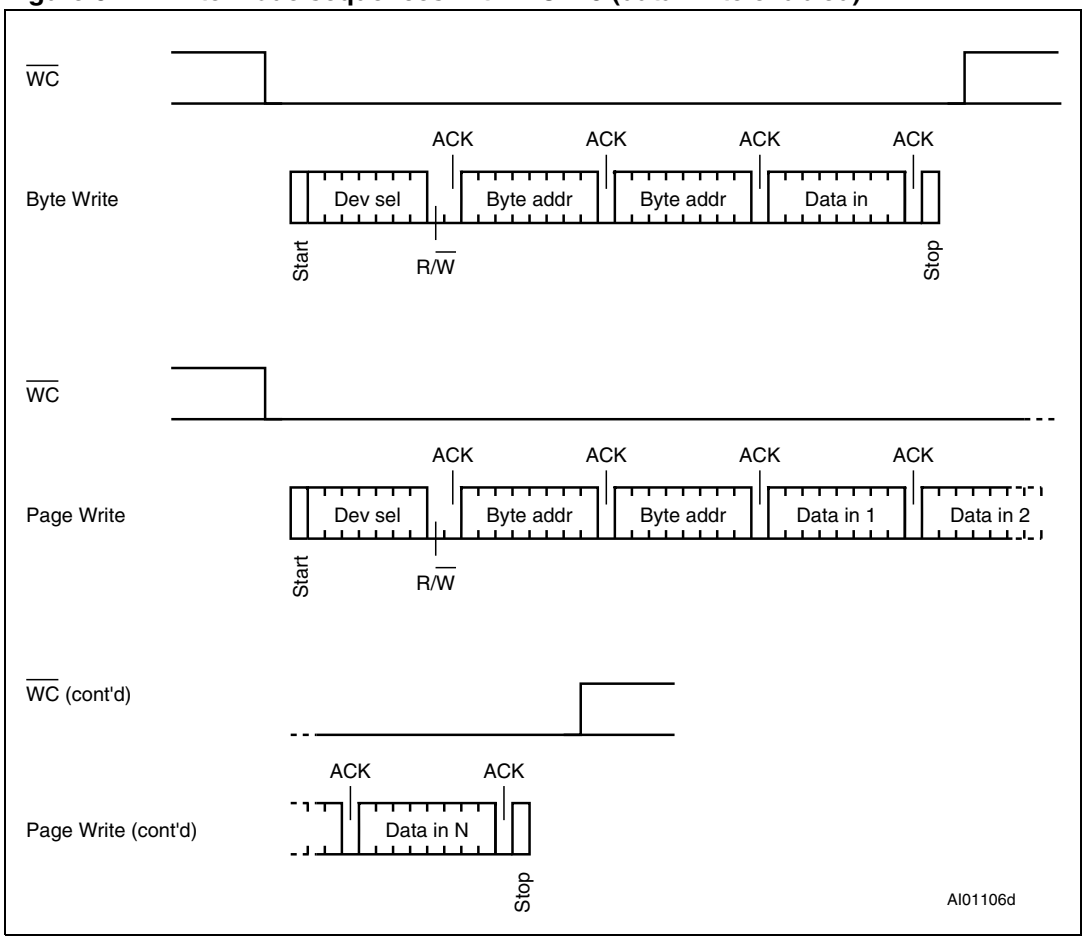
During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

If the Write Control input (WC) is driven High, the Write instruction is not executed and the accompanying data bytes are *not* acknowledged, as shown in *Figure 7*.

5.1.1 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 6*.

Figure 6. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)



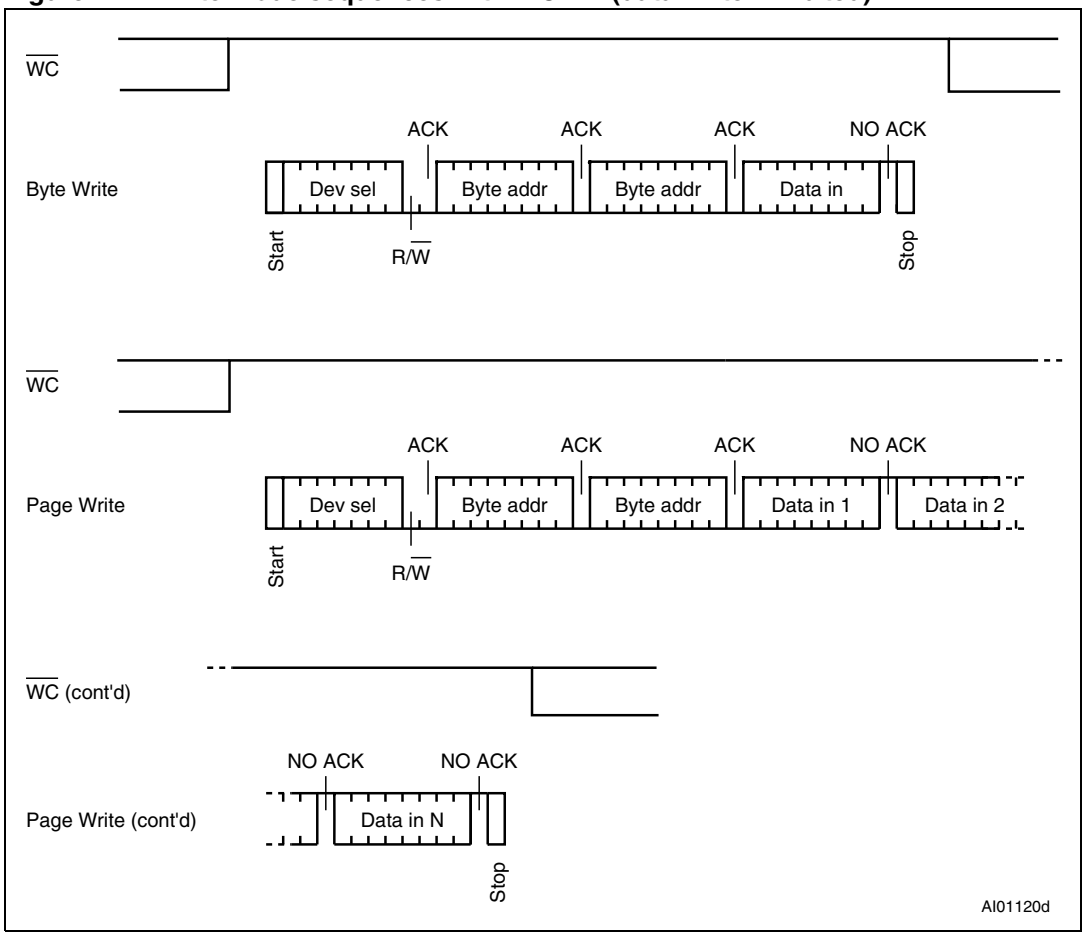
5.1.2 Page Write

The Page Write mode allows up to 32 bytes to be written in a single Write cycle, provided that they are all located in the same page in the memory: that is, the most significant memory address bits, b16-b5, are the same. If more bytes are sent than will fit up to the end of the page, a “roll-over” occurs, i.e. the bytes exceeding the page end are written on the same page, from location 0.

The bus master sends from 1 to 32 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is low. If Write Control ($\overline{WC}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck, as shown in *Figure 7*. After each transferred byte, the internal page address counter is incremented.

The transfer is terminated by the bus master generating a Stop condition.

Figure 7. Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)



5.1.3 Write Identification Page (M24C32-D only)

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences:

- Device type identifier = 1011b
- MSB address bits A15/ are don't care except for address bit A10 which must be ‘0’. LSB address bits A4/A0 define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

5.1.4 Lock Identification Page (M24C32-D only)

The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

- Device type identifier = 1011b
- Address bit A10 must be ‘1’; all other address bits are don't care
- The data byte must be equal to the binary value xxxx xx1x, where x is don't care

5.1.5 ECC (Error Correction Code) and Write cycling

The Error Correction Code (ECC) is an internal logic function which is transparent for the I^2C communication protocol.

The ECC logic is implemented on each group of four EEPROM bytes[a]. Inside a group, if a single bit out of the four bytes happens to be erroneous during a Read operation, the ECC detects this bit and replaces it with the correct value. The read reliability is therefore much improved.

Even if the ECC function is performed on groups of four bytes, a single byte can be written/cycled independently. In this case, the ECC function also writes/cycles the three other bytes located in the same group[a]. As a consequence, the maximum cycling budget is defined at group level and the cycling can be distributed over the 4 bytes of the group: the sum of the cycles seen by byte0, byte1, byte2 and byte3 of the same group must remain below the maximum value defined in *Table 12: Cycling performance by groups of four bytes*.

a. A group of four bytes is located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3], where N is an integer.

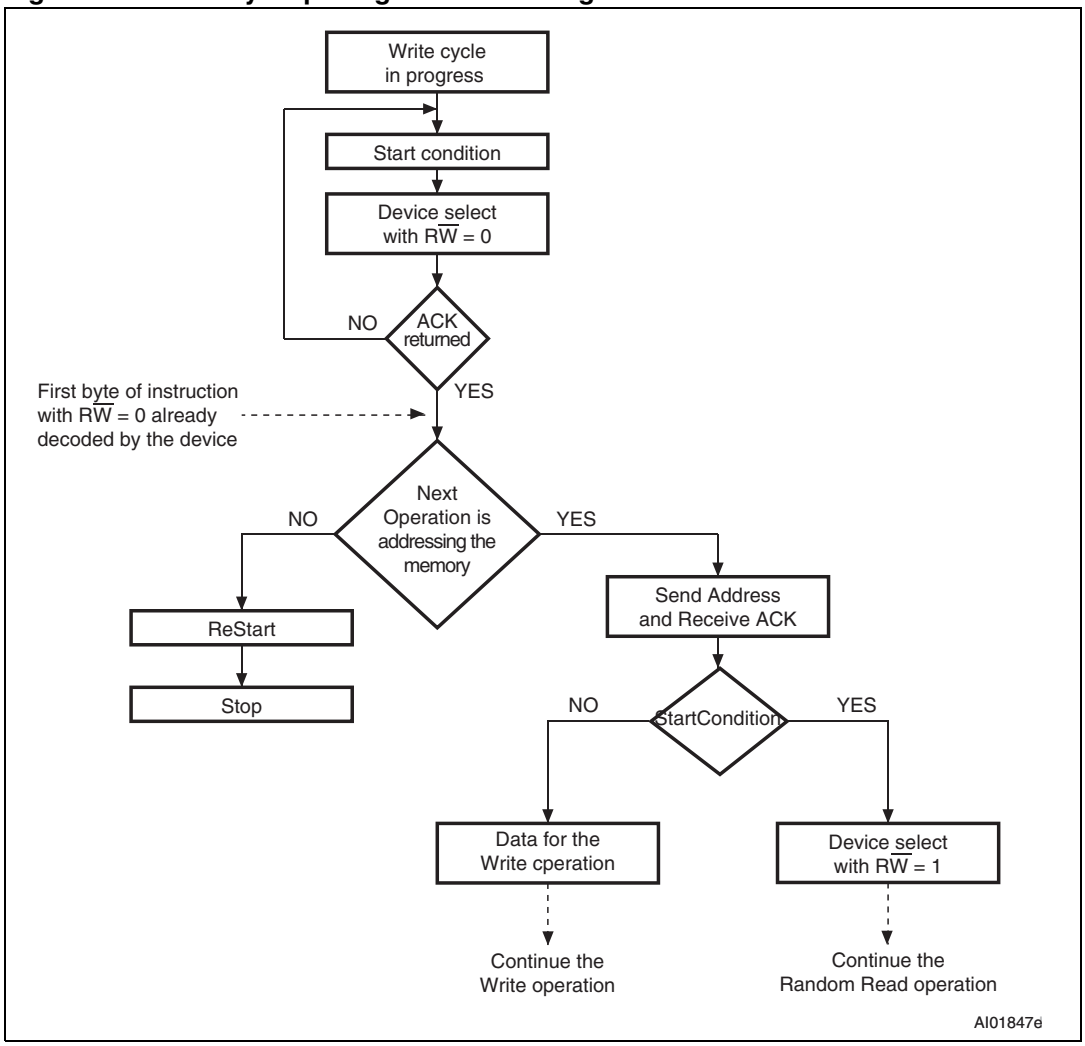
5.1.6 Minimizing Write delays by polling on ACK

The maximum Write time (t_w) is shown in AC characteristics tables in *Section 8: DC and AC parameters*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 8*, is:

- Initial condition: a Write cycle is in progress.
- Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).
- Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 8. Write cycle polling flowchart using ACK



1. The seven most significant bits of the Device Select code of a Random Read (bottom right box in the figure) must be identical to the seven most significant bits of the Device Select code of the Write (polling instruction in the figure).

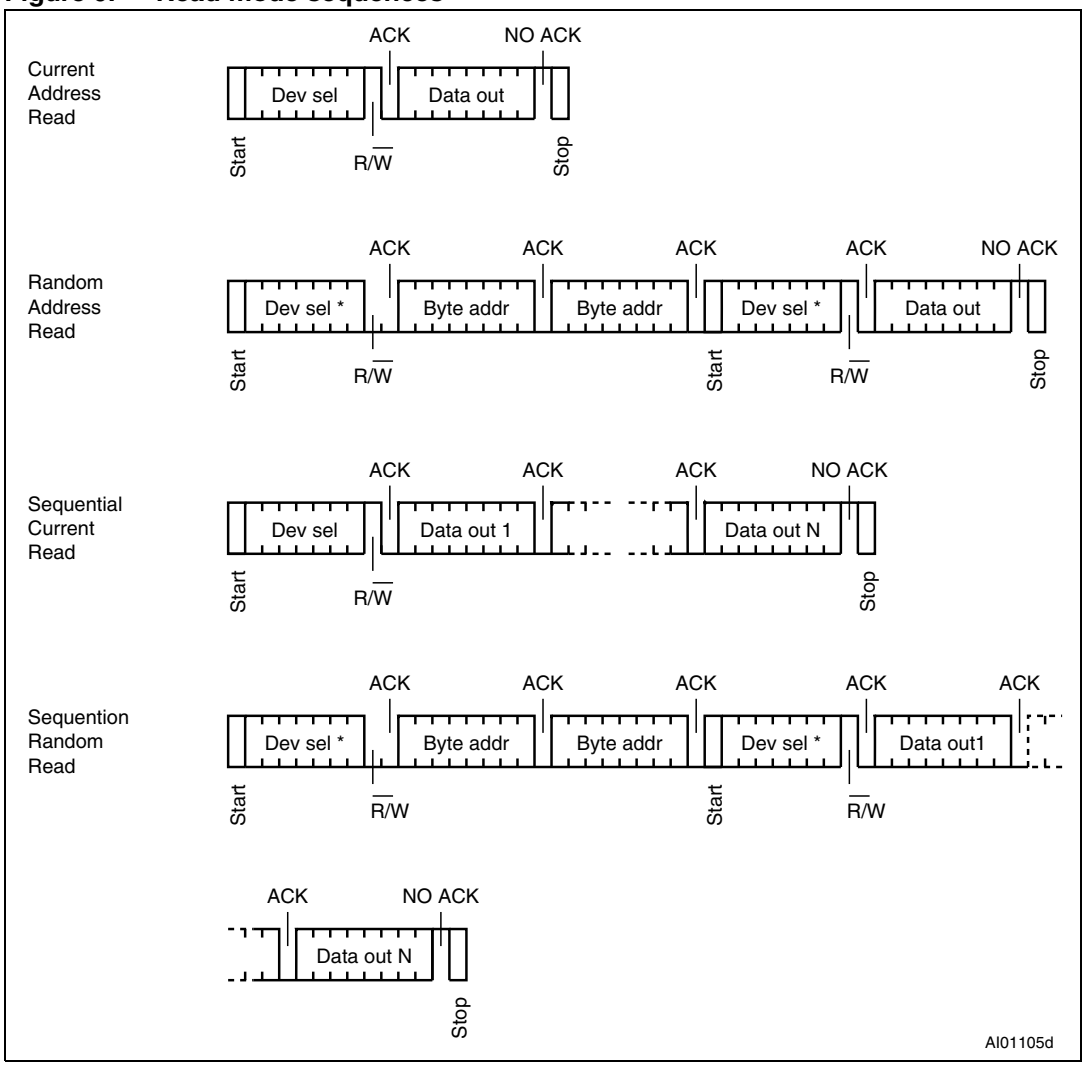
5.2 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device's internal address counter is incremented by one, to point to the next byte address.

For the Read instructions, after each byte read (data out), the device waits for an acknowledgment (data in) during the 9th bit time. If the bus master does not acknowledge during this 9th time, the device terminates the data transfer and switches to its Standby mode.

Figure 9. Read mode sequences



5.2.1 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 9*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the $\overline{RW}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

5.2.2 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 9*, *without* acknowledging the byte.

5.2.3 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 9*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter “rolls-over”, and the device continues to output data from memory address 00h.

5.3 Read Identification Page (M24C32-D only)

The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing an Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits A15/A5 are don't care, the LSB address bits A4/A0 define the byte address inside the Identification Page. The number of bytes to read in the ID page must not exceed the page boundary (e.g.: when reading the Identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes).

5.4 Read the lock status (M24C32-D only)

The locked/unlocked status of the Identification page can be checked by transmitting a specific truncated command [Identification Page Write instruction + one data byte] to the device. The device returns an acknowledge bit if the Identification page is unlocked, otherwise a NoAck bit if the Identification page is locked.

Right after this, it is recommended to transmit to the device a Start condition followed by a Stop condition, so that:

- Start: the truncated command is not executed because the Start condition resets the device internal logic,
- Stop: the device is then set back into Standby mode by the Stop condition.

6 Initial delivery state

The device is delivered with all bits set to 1 (both in the memory array and in the Identification page - that is, each byte contains FFh).

7 Maximum rating

Stressing the device outside the ratings listed in *Table 5* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note(1)		°C
	PDIP-specific lead temperature during soldering		260(2)	°C
V_{IO}	Input or output range	–0.50	6.5	V
I_{OL}	DC output current (SDA = 0)	-	5	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body model)(3)	-	4000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.
2. T_{LEAD} max must not be applied for more than 10 s.
3. Positive and negative pulses applied on different combinations of pin connections, according to AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω).

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 6. Operating conditions (voltage range W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1	MHz

Table 7. Operating conditions (voltage range R)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1	MHz

Table 8. Operating conditions (voltage range F)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.7	5.5	V
T_A	Ambient operating temperature	–40	85	°C
f_C	Operating clock frequency	-	1	MHz

Table 9. Operating conditions (voltage range X)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.6	5.5	V
T_A	Ambient operating temperature	–20	85	°C
f_C	Operating clock frequency	-	1	MHz

Table 10. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_{bus}	Load capacitance	100		pF
	SCL input rise/fall time, SDA input fall time		50	ns
	Input levels	0.2 V_{CC} to 0.8 V_{CC}		V
	Input and output timing reference levels	0.3 V_{CC} to 0.7 V_{CC}		V

Figure 10. AC measurement I/O waveform

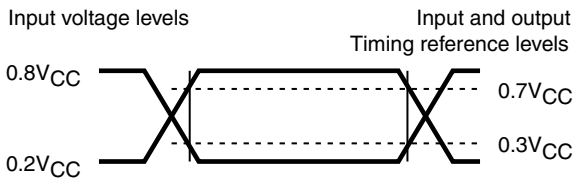


Table 11. Input parameters

Symbol	Parameter(1)	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)			8	pF
C_{IN}	Input capacitance (other pins)			6	pF
Z_L	Input impedance (E2, E1, E0, $\overline{WC}$)(2)	$V_{IN} < 0.3\ V_{CC}$	30		kΩ
Z_H		$V_{IN} > 0.7\ V_{CC}$	500		kΩ

1. Characterized only, not tested in production.
2. E2, E1, E0 input impedance when the memory is selected (after a Start condition).

Table 12. Cycling performance by groups of four bytes

Symbol	Parameter	Test condition(1)	Max.	Unit
Ncycle	Write cycle endurance(2)	TA ≤ 25 °C, V_{CC}(min) < V_{CC} < V_{CC}(max)	4,000,000	Write cycle(3)
		TA = 85 °C, V_{CC}(min) < V_{CC} < V_{CC}(max)	1,200,000	

1. Cycling performance for products identified by process letter K.
2. The Write cycle endurance is defined for groups of four data bytes located at addresses [4*N, 4*N+1, 4*N+2, 4*N+3] where N is an integer. The Write cycle endurance is defined by characterization and qualification.
3. A Write cycle is executed when either a Page Write, a Byte Write, a Write Identification Page or a Lock Identification Page instruction is decoded. When using the Byte Write, the Page Write or the Write Identification Page, refer also to *Section 5.1.5: ECC (Error Correction Code) and Write cycling*.

Table 13. Memory cell data retention

Parameter	Test condition	Min.	Unit
Data retention(1)	TA = 55 °C	200	Year

1. For products identified by process letter K. The data retention behavior is checked in production. The 200-year limit is defined from characterization and qualification results.

Table 14. DC characteristics (M24C32-W, device grade 6)

Symbol	Parameter	Test conditions (see *Table 6*)	Min.	Max.	Unit
I_{LI}	Input leakage current (SCL, SDA, E2, E1, E0)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	2.5 V < V_{CC} < 5.5 V, f_c = 400 kHz (rise/fall time < 50 ns)		2	mA
		2.5 V < V_{CC} < 5.5 V, f_c = 1 MHz(1) (rise/fall time < 50 ns)		2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 2.5 V < V_{CC} < 5.5 V		5(2)	mA
I_{CC1}	Standby supply current	Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		2	µA
		Device not selected(3), $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V		5(4)(5)	µA
V_{IL}	Input low voltage (SCL, SDA, WC)		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)		0.7 V_{CC}	6.5	V
	Input high voltage (WC, E2, E1, E0)		0.7 V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA, V_{CC} = 2.5 V or I_{OL} = 3 mA, V_{CC} = 5.5 V		0.4	V

1. Only for devices operating at f_C max = 1 MHz (see note(1) in *Table 19*)
2. Characterized value, not tested in production.
3. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).
4. The new M24C32-W devices (identified by the process letter K) offer I_{CC1} = 3µA (max)
5. 5 µA for previous devices identified by process letter A.

Table 15. DC characteristics (M24C32-R, device grade 6)

Symbol	Parameter	Test conditions[1] (in addition to those in *Table 7*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c= 400 kHz		0.8	mA
		f_c= 1 MHz[2]		2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 1.8 V		3[3]	mA
I_{CC1}	Standby supply current	Device not selected[4], $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		1	µA
V_{IL}	Input low voltage (SCL, SDA, WC)	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.8 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	6.5	V
	Input high voltage (WC, E2, E1, E0)	1.8 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.8 V		0.2	V

1. If the application uses the voltage range R device with 2.5 V < V_{cc} < 5.5 V and -40 °C < TA < +85 °C, please refer to *Table 14* instead of this table.
2. Only for devices operating at f_C max = 1 MHz (see see note[1] in *Table 19*).
3. Characterized value, not tested in production.
4. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 16. DC characteristics (M24C32-F, device grade 6)

Symbol	Parameter	Test conditions[1] (in addition to those in *Table 8*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.7 V, f_c= 400 kHz		0.8	mA
		f_c= 1 MHz[2]		2.5	mA
I_{CC0}	Supply current (Write)	During t_W 1.7 V < V_{CC} < 2.5 V		3[3]	mA
I_{CC1}	Standby supply current	Device not selected[4], $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.7 V		1	µA
V_{IL}	Input low voltage (SCL, SDA, WC)	1.7 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.7 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	6.5	V
	Input high voltage (WC, E2, E1, E0)	1.7 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.7 V		0.2	V

1. If the application uses the voltage range F device with 2.5 V < V_{CC} < 5.5 V and -40 °C < TA < +85 °C, please refer to *Table 14* instead of this table.
2. Only for devices operating at f_C max = 1 MHz (see note[1] in *Table 19*).
3. Characterized value, not tested in production.
4. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 17. DC characteristics (M24C32-X, device grade 5)

Symbol	Parameter	Test conditions[1] (in addition to those in *Table 9*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	SDA in Hi-Z, external voltage applied on SDA: V_{SS} or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.6 V, f_c= 400 kHz		0.8	mA
		f_c= 1 MHz[2]		2.5	
I_{CC0}	Supply current (Write)	During t_W, 1.6 V < V_{CC} < 2.5 V		3[3]	mA
I_{CC1}	Standby supply current	Device not selected[4], $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.6 V		1	µA
V_{IL}	Input low voltage (SCL, SDA, WC)	1.6 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
V_{IH}	Input high voltage (SCL, SDA)	1.6 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	6.5	V
	Input high voltage (WC, E2, E1, E0)	1.6 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+0.6	V
V_{OL}	Output low voltage	I_{OL} = 1 mA, V_{CC} = 1.6 V		0.2	V

1. If the application uses the device with 2.5 V < V_{CC} < 5.5 V and -20 °C < TA < +85 °C, please refer to *Table 14* instead of this table.
2. Only for devices operating at f_C max = 1 MHz (see note[1] in *Table 19*)
3. Characterized value, not tested in production.
4. The device is not selected after power-up, after a Read instruction (after the Stop condition), or after the completion of the internal write cycle t_W (t_W is triggered by the correct decoding of a Write instruction).

Table 18. 400 kHz AC characteristics

Symbol	Alt.	Parameter	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	-	400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300	-	ns
t_{QL1QL2}(1)	t_F	SDA (out) fall time	20(2)	300	ns
t_{XH1XH2}	t_R	Input signal rise time	(3)	(3)	ns
t_{XL1XL2}	t_F	Input signal fall time	(3)	(3)	ns
t_{DXCH}	$t_{SU:DAT}$	Data in set up time	100	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}(4)	t_{DH}	Data out hold time	100(5)	-	ns
t_{CLQV}(6)	t_{AA}	Clock low to next data valid (access time)	-	900	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	600	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300	-	ns
t_{WLDL}(7)(1)	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	µs
t_{DHWH}(8)(1)	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Internal Write cycle duration	-	5(9)	ms
t_{NS}(1)		Pulse width ignored (input filter on SCL and SDA) - single glitch	-	80(10)	ns

1. Characterized only, not tested in production.
2. With C_L = 10 pF.
3. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be more than 20 ns and less than 300 ns when f_C < 400 kHz.
4. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
5. The previous product identified by process letter P was specified with t_{CLQX} = 200 ns (min). Both values offer a safe margin compared to the I^2C specification recommendations.
6. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either $0.3V_{CC}$ or $0.7V_{CC}$, assuming that $R_{bus} \times C_{bus}$ time constant is within the values specified in *Figure 11*.
7. $\overline{WC}$=0 set up time condition to enable the execution of a WRITE command.
8. $\overline{WC}$=0 hold time condition to enable the execution of a WRITE command.
9. 10 ms for the M24C32-X, when V_{CC}< 1.7 V.
10. The previous M24C32 device (identified by process letter P) offers t_{NS} = 100 ns (max), while the current M24C32 device offers t_{NS} = 80 ns (max). Both products offer a safe margin compared to the 50 ns minimum value recommended by the I^2C specification.

Table 19. 1 MHz AC characteristics

Symbol	Alt.	Parameter[1]	Min.	Max.	Unit
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	260	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	500	-	ns
t_{XH1XH2}	t_R	Input signal rise time	(2)	(2)	ns
t_{XL1XL2}	t_F	Input signal fall time	(2)	(2)	ns
t_{QL1QL2}[3]	t_F	SDA (out) fall time	20[4]	120	ns
t_{DXCX}	$t_{SU:DAT}$	Data in setup time	50	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}[5]	t_{DH}	Data out hold time	100	-	ns
t_{CLQV}[6]	t_{AA}	Clock low to next data valid (access time)		450	ns
t_{CHDL}	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_{WLDL}[7][3]	$t_{SU:WC}$	$\overline{WC}$ set up time (before the Start condition)	0	-	µs
t_{DHWH}[8][3]	$t_{HD:WC}$	$\overline{WC}$ hold time (after the Stop condition)	1	-	µs
t_W	t_{WR}	Write time	-	5[9]	ms
t_{NS}[3]		Pulse width ignored (input filter on SCL and SDA)	-	80	ns

1. Only for M24C32 devices identified by the process letter K (devices qualified at 1 MHz).
2. There is no min. or max. values for the input signal rise and fall times. It is however recommended by the I²C specification that the input signal rise and fall times be less than 120 ns when f_C < 1 MHz.
3. Characterized only, not tested in production.
4. With C_L = 10 pF.
5. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.
6. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach either 0.3 V_{CC} or 0.7 V_{CC}, assuming that the Rbus × Cbus time constant is within the values specified in *Figure 12*.
7. $\overline{WC}$=0 set up time condition to enable the execution of a WRITE command.
8. $\overline{WC}$=0 hold time condition to enable the execution of a WRITE command.
9. 10 ms for the M24C32-X, when V_{CC}< 1.7 V.

Figure 11. Maximum R_{bus} value versus bus parasitic capacitance (C_{bus}) for an I^2C bus at maximum frequency f_C = 400 kHz

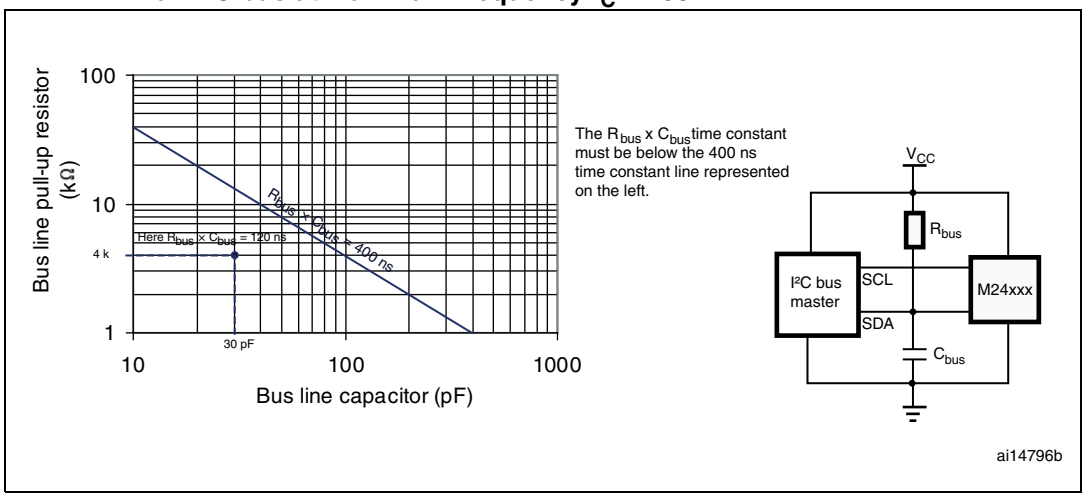


Figure 12. Maximum R_{bus} value versus bus parasitic capacitance C_{bus}) for an I^2C bus at maximum frequency f_C = 1MHz

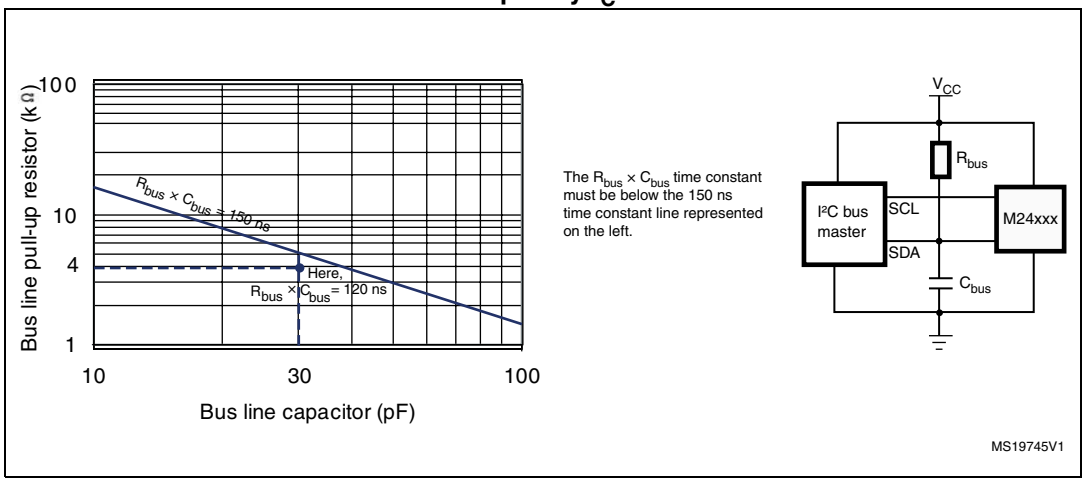
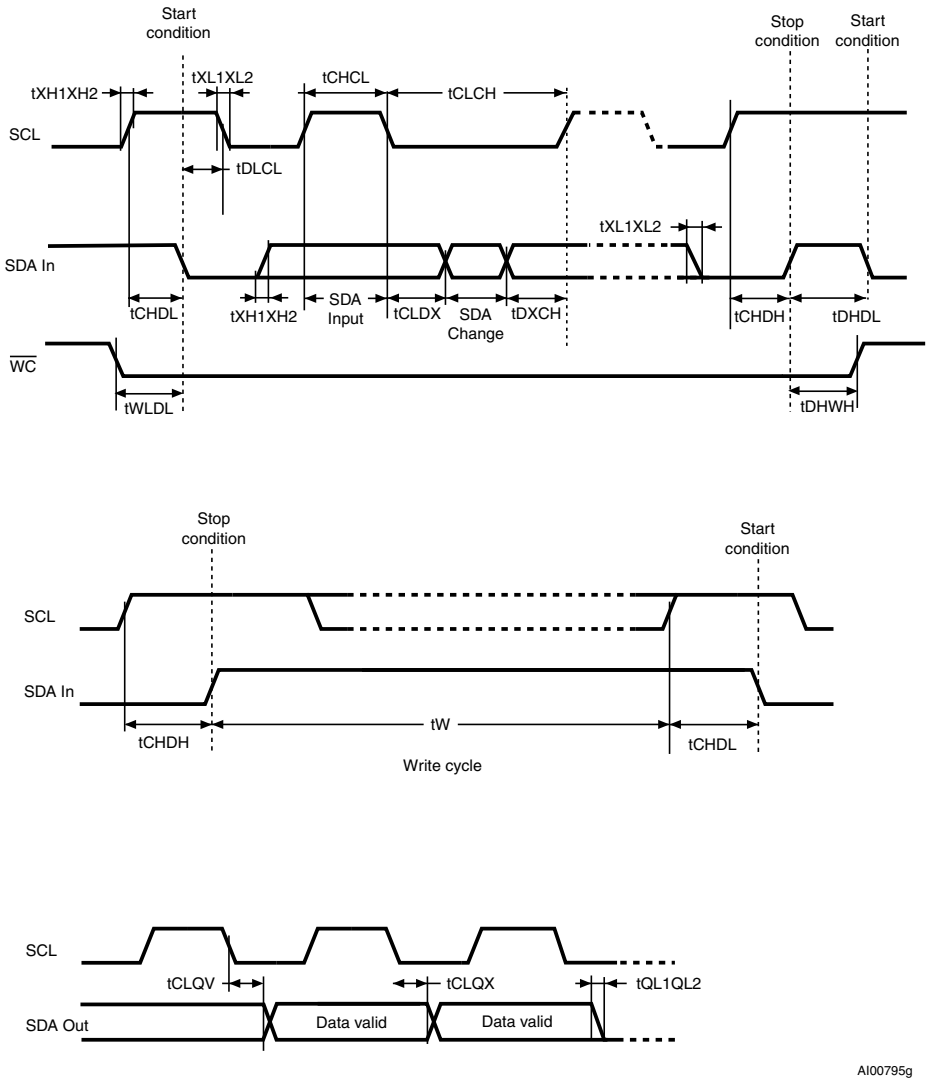


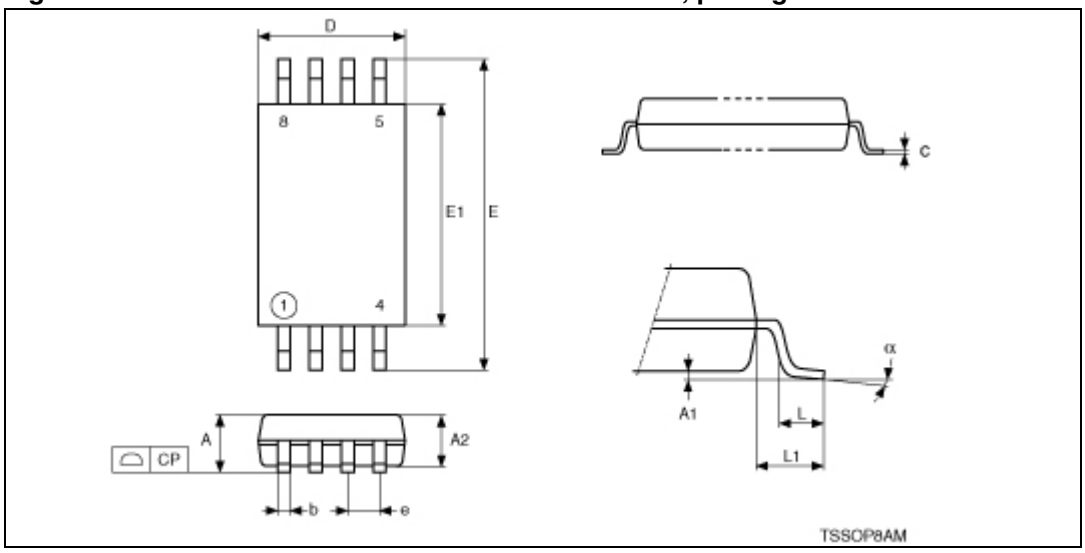
Figure 13. AC waveforms



9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 14. TSSOP8 – 8-lead thin shrink small outline, package outline



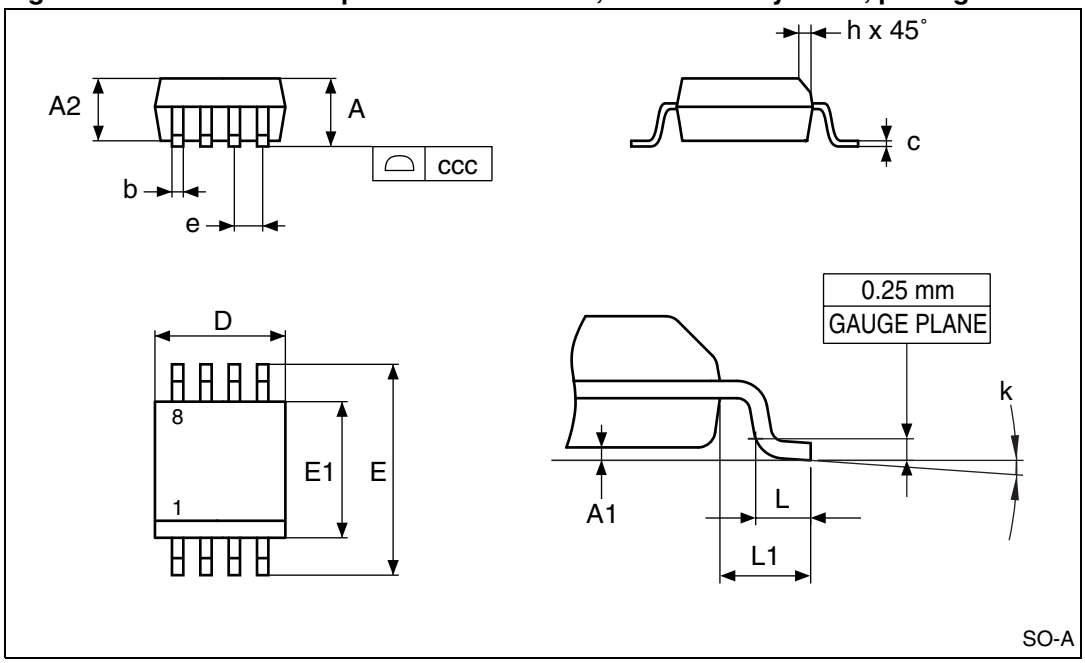
1. Drawing is not to scale.

Table 20. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches(1)		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 15. SO8N – 8 lead plastic small outline, 150 mils body width, package outline



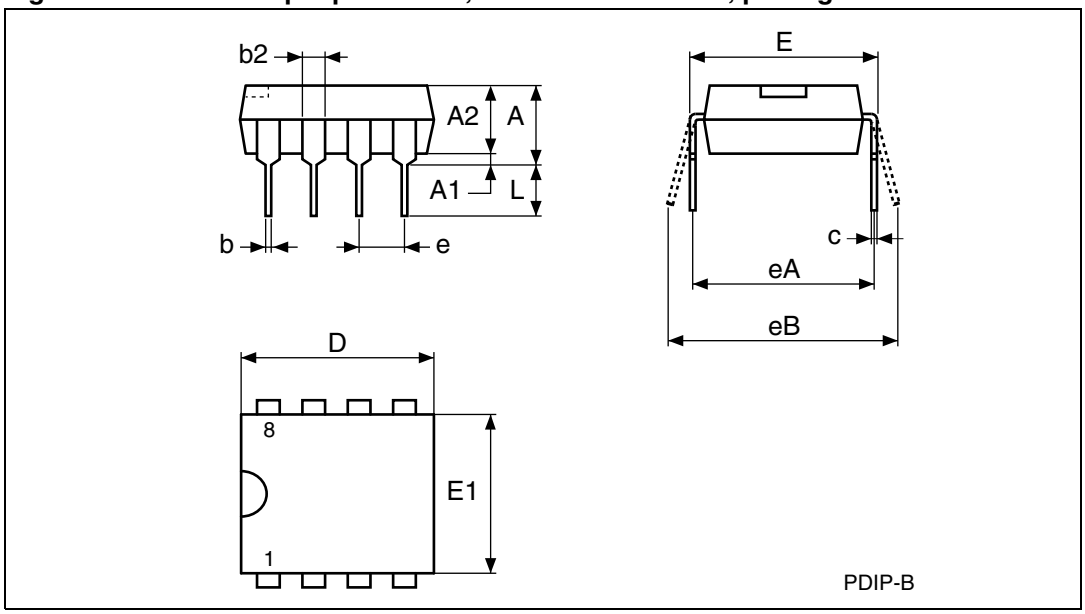
1. Drawing is not to scale.

Table 21. SO8N – 8 lead plastic small outline, 150 mils body width, package data

Symbol	millimeters			inches (1)		
	Typ	Min	Max	Typ	Min	Max
A			1.750			0.0689
A1		0.100	0.250		0.0039	0.0098
A2		1.250			0.0492	
b		0.280	0.480		0.0110	0.0189
c		0.170	0.230		0.0067	0.0091
ccc			0.100			0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270			0.0500		
h		0.250	0.500		0.0098	0.0197
k		0°	8°		0°	8°
L		0.400	1.270		0.0157	0.0500
L1	1.040			0.0409		

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 16. PDIP8 – 8 pin plastic DIP, 0.25 mm lead frame, package outline



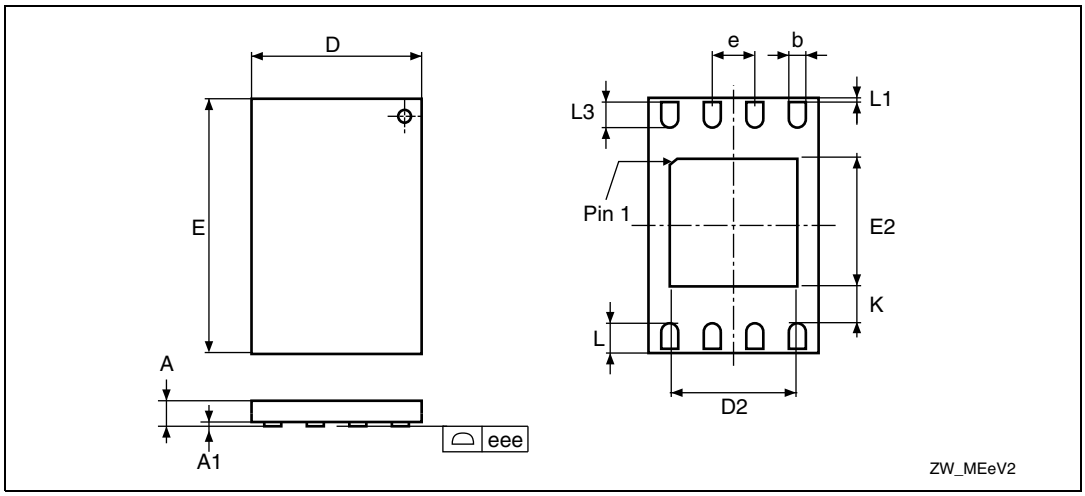
1. Drawing is not to scale.

Table 22. PDIP8 – 8 pin plastic DIP, 0.25 mm lead frame, package mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			5.33			0.2098
A1		0.38			0.0150	
A2	3.30	2.92	4.95	0.1299	0.1150	0.1949
b	0.46	0.36	0.56	0.0181	0.0142	0.0220
b2	1.52	1.14	1.78	0.0598	0.0449	0.0701
c	0.25	0.20	0.36	0.0098	0.0079	0.0142
D	9.27	9.02	10.16	0.3650	0.3551	0.4000
E	7.87	7.62	8.26	0.3098	0.3000	0.3252
E1	6.35	6.10	7.11	0.2500	0.2402	0.2799
e	2.54	–	–	0.1000	–	–
eA	7.62	–	–	0.3000	–	–
eB			10.92			0.4299
L	3.30	2.92	3.81	0.1299	0.1150	0.1500

1. Values in inches are converted from mm and rounded to four decimal digits.

Figure 17. UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package outline



1. Drawing is not to scale.
2. The central pad (area E2 by D2 in the above illustration) is internally pulled to V_{SS}. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 23. UFDFPN8 (MLP8) 8-lead ultra thin fine pitch dual flat package no lead 2 x 3 mm, data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.550	0.450	0.600	0.0217	0.0177	0.0236
A1	0.020	0.000	0.050	0.0008	0.0000	0.0020
b	0.250	0.200	0.300	0.0098	0.0079	0.0118
D	2.000	1.900	2.100	0.0787	0.0748	0.0827
D2 (rev MC)		1.200	1.600		0.0472	0.0630
E	3.000	2.900	3.100	0.1181	0.1142	0.1220
E2 (rev MC)		1.200	1.600		0.0472	0.0630
e	0.500			0.0197		
K (rev MC)		0.300			0.0118	
L		0.300	0.500		0.0118	0.0197
L1			0.150			0.0059
L3		0.300			0.0118	
eee[2]		0.080			0.0031	

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measuring.

10 Part numbering

Table 24. Ordering information scheme

Example: M24C32 - D W MN 6 T P /P

Device type

M24 = I^2C serial access EEPROM

Device function

C32 = 32 Kbit (4096 x 8)

Device family

Blank: Without Identification page

D: With additional Identification page

Operating voltage

W = V_{CC} = 2.5 V to 5.5 V

R = V_{CC} = 1.8 V to 5.5 V

F = V_{CC} = 1.7 V to 5.5 V

X = V_{CC} = 1.6 V to 5.5 V

Package

BN = PDIP8(1)

MN = SO8 (150 mil width)(2)

DW = TSSOP8 (169 mil width)(2)

MC = UFDFPN8 (MLP8)

Device grade

6 = Industrial: device tested with standard test flow over –40 to 85 °C

5 = Consumer: device tested with standard test flow over –20 to 85°C

Option

blank = standard packing

T = Tape and reel packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

Process(3)

/P or /K = Manufacturing technology code

1. RoHS-compliant (ECOPACK1®)
2. RoHS-compliant and halogen-free (ECOPACK2®)
3. The process letters appear on the device package (marking) and on the shipment box. Please contact your nearest ST Sales Office for further information.

11 Revision history

Table 25. Document revision history

Date	Revision	Changes
18-Mar-2011	18	Added: – M24C32-DF and all information concerning the Identification Page: sections *4.9*, *4.10*, *4.17*, *4.18* – ECC section *4.11* – AC table with clock frequency of 1 MHz (*Table 18*) – *Table 4: Device select code* Updated: – *Section 1: Description* – *Section 4.5: Memory addressing* – *Section 4.18: Read the lock status (M24C32-D)* – *Table 6: Absolute maximum ratings* – AC/DC tables *13*, *17* with values specific to the device identified with process letter K Deleted: – *Table 2: Device select code* – *Table 23: Available M24C32 products (package, voltage range, temperature grade)*
14-Sep-2011	19	Updated: – *Figure 4: I^2C Fast mode (f_C = 400 kHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})* – *Figure 5: I^2C Fast mode Plus (f_C = 1 MHz): maximum R_{bus} value versus bus parasitic capacitance (C_{bus})* Added t_{WLDL} and t_{DHWH} in: – *Table 17: 400 kHz AC characteristics* – *Table 18: 1 MHz AC characteristics* – *Figure 13: AC waveforms* Minor text changes.
21-May-2012	20	Datasheet split into: – M24C32-DF, M24C32-W, M24C32-R,M24C32-F (this datasheet) for standard products (range 6), – M24C32-125 datasheet for automotive products (range 3).
25-Jul-2012	21	Added reference M24C32-X. Updated: – *Features* – AC and DC tables in *Section 8: DC and AC parameters*. – *Section 10: Part numbering*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

Document Revision History

Date	Rev.	Description of the Revision
April 10, 2014	1.00	First draft creation

Source Documents & Reference Documents

Source document Title	**Rev.:**	**Date:**

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries(‘‘ST’’) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND / OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR ‘‘AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL’’ INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

RESTRICTIONS OF USE AND CONFIDENTIALITY OBLIGATIONS:

THIS DOCUMENT AND ITS ANNEXES CONTAIN ST PROPRIETARY AND CONFIDENTIAL INFORMATION. THE DISCLOSURE, DISTRIBUTION, PUBLICATION OF WHATSOEVER NATURE OR USE FOR ANY OTHER PURPOSE THAN PROVIDED IN THIS DOCUMENT OF ANY INFORMATION CONTAINED IN THIS DOCUMENT AND ITS ANNEXES IS SUBMITTED TO ST PRIOR EXPRESS AUTHORIZATION. ANY UNAUTHORIZED REVIEW, USE, DISCLOSURE OR DISTRIBUTION OF SUCH INFORMATION IS EXPRESSLY PROHIBITED.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com