

16-Mbit (1M x 16) Static RAM

Features

- Very high speed: 55 ns
- Wide voltage range: 1.65V–1.95V
- Ultra low active power
 - Typical active current: 1.5 mA @ f = 1 MHz
 - Typical active current: 15 mA @ f = f_{max}
- Ultra low standby power
- Easy memory expansion with \overline{CE}_1 , CE₂, and \overline{OE} features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 48-ball VFBGA package

Functional Description^[1]

The CY62167DV18 is a high performance CMOS static RAM organized as 1M words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 99% when addresses are not toggling. Placing the device into standby mode reduces power

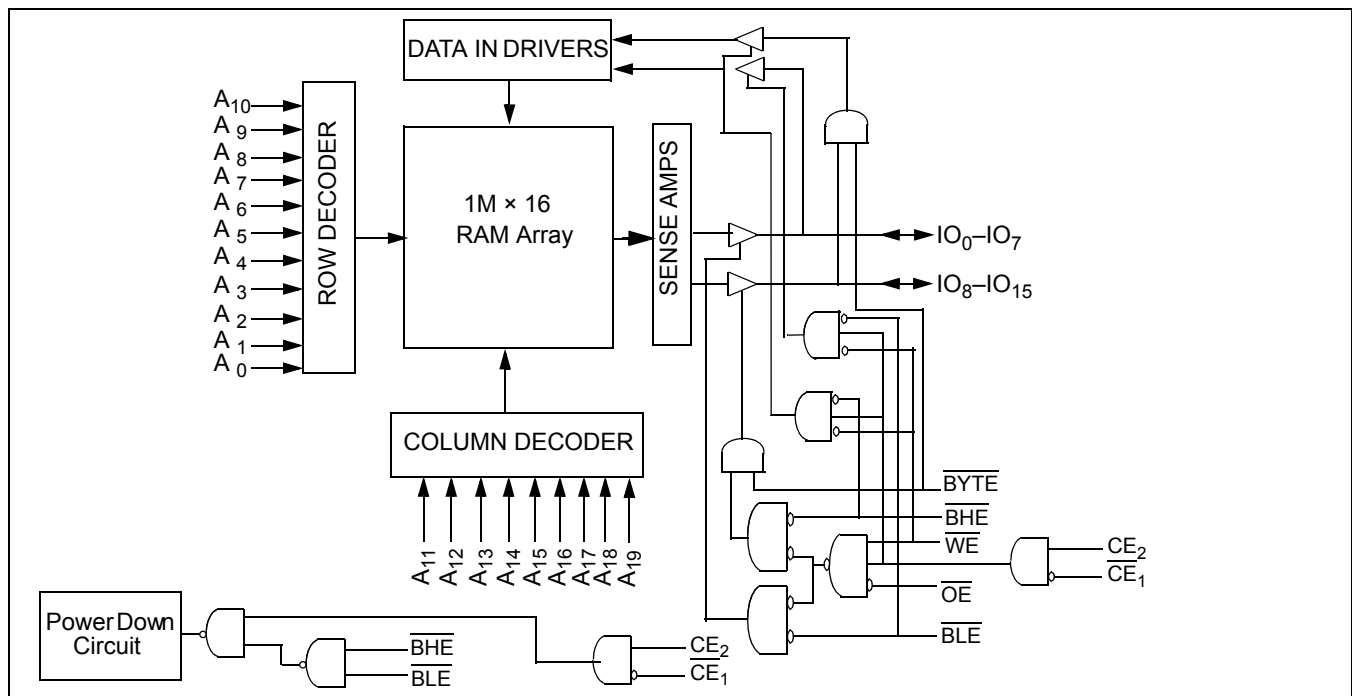
consumption by more than 99% when deselected (\overline{CE}_1 HIGH or CE₂ LOW or both \overline{BHE} and \overline{BLE} are HIGH). The input and output pins (IO₀ through IO₁₅) are placed in a high impedance state when:

- Deselected (\overline{CE}_1 HIGH or CE₂ LOW)
- Outputs are disabled (\overline{OE} HIGH)
- Both Byte High Enable (\overline{BHE}) and Byte Low Enable (\overline{BLE}) are disabled (\overline{BHE} , \overline{BLE} HIGH)
- Write operation is active (\overline{CE}_1 LOW, CE₂ HIGH and \overline{WE} LOW)

To write to the device, take Chip Enables (\overline{CE}_1 LOW and CE₂ HIGH) and Write Enable (\overline{WE}) input LOW. If \overline{BLE} is LOW, then data from IO pins (IO₀ through IO₇) is written into the location specified on the address pins (A₀ through A₁₉). If \overline{BHE} is LOW, then data from IO pins (IO₈ through IO₁₅) is written into the location specified on the address pins (A₀ through A₁₉).

To read from the device, take Chip Enables (\overline{CE}_1 LOW and CE₂ HIGH) and \overline{OE} LOW while forcing the \overline{WE} HIGH. If \overline{BLE} is LOW, then data from the memory location specified by the address pins appear on IO₀ to IO₇. If \overline{BHE} is LOW, then data from memory appears on IO₈ to IO₁₅. See the "Truth Table" on page 9 for a complete description of read and write modes.

Logic Block Diagram

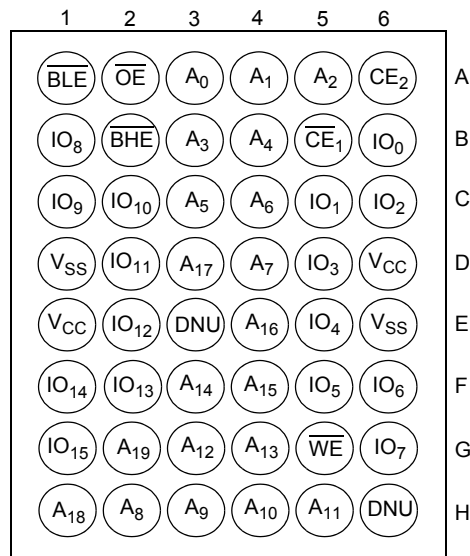


Note

1. For best practice recommendations, refer to the Cypress application note "System Design Guidelines" at <http://www.cypress.com>.

Product Portfolio

| Product | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---------------|---------------------------|--------------------|----------------------|------------|--------------------------------|-----|--------------------|-----|-------------------------------|-----|
| | | | | | Operating I _{CC} (mA) | | | | Standby I _{SB2} (μA) | |
| | f = 1MHz | | f = f _{max} | | | | | | | |
| | Min | Typ ^[2] | Max | | Typ ^[2] | Max | Typ ^[2] | Max | Typ ^[2] | Max |
| CY62167DV18LL | 1.65 | 1.8 | 1.95 | 55 | 1.5 | 5 | 15 | 30 | 2.5 | 20 |

Pin Configuration ^[3]
**48-Ball VFBGA
Top View**

Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25°C.
- DNU pins must be left floating or tied to V_{SS} to ensure proper operation.

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65°C to +150°C
 Ambient Temperature with Power Applied -55°C to +125°C
 Supply Voltage to Ground Potential . -0.2V to $V_{CCmax} + 0.2V$
 DC Voltage Applied to Outputs in High-Z State^[4, 5] -0.2V to $V_{CCmax} + 0.2V$

DC Input Voltage^[4, 5] -0.2V to $V_{CCmax} + 0.2V$
 Output Current into Outputs (LOW) 20 mA
 Static Discharge Voltage > 2001V (MIL-STD-883, Method 3015)
 Latch up Current > 200 mA

Operating Range

| Range | Ambient Temperature | V_{CC} ^[6] |
|------------|---------------------|-------------------------|
| Industrial | -40°C to +85°C | 1.65V to 1.95V |

DC Electrical Characteristics (Over the Operating Range)

| Parameter | Description | Test Conditions | 55 ns | | | Unit |
|-----------|---|--|---|--------------------|----------------|---------------|
| | | | Min | Typ ^[2] | Max | |
| V_{OH} | Output HIGH Voltage | $I_{OH} = -0.1 \text{ mA}$ | 1.4 | | | V |
| V_{OL} | Output LOW Voltage | $I_{OL} = 0.1 \text{ mA}$ | | | 0.2 | V |
| V_{IH} | Input HIGH Voltage | | 1.4 | | $V_{CC} + 0.2$ | V |
| V_{IL} | Input LOW Voltage | | -0.2 | | 0.4 | V |
| I_{IX} | Input Leakage Current | $GND \leq V_I \leq V_{CC}$ | -1 | | +1 | μA |
| I_{OZ} | Output Leakage Current | $GND \leq V_O \leq V_{CC}$, Output Disabled | -1 | | +1 | μA |
| I_{CC} | V_{CC} Operating Supply Current | $f = f_{MAX} = 1/t_{RC}$ $f = 1 \text{ MHz}$ | $V_{CC} = 1.95V$, $I_{OUT} = 0 \text{ mA}$, CMOS level | 15 | 30 | mA |
| | | | | 1.5 | 5 | |
| I_{SB1} | Automatic CE Power down Current – CMOS Inputs | $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$, $V_{IN} \leq 0.2V$, $f = f_{MAX}$ (Address and Data Only), $f = 0$ (\overline{OE} , \overline{WE} , \overline{BHE} and \overline{BLE}) | | 2.5 | 20 | μA |
| I_{SB2} | Automatic CE Power down Current – CMOS Inputs | $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0$, $V_{CC} = 1.95V$ | | 2.5 | 20 | μA |

Capacitance ^[7]

| Parameter | Description | Test Conditions | Max | Unit |
|-----------|--------------------|---|-----|------|
| C_{IN} | Input Capacitance | $T_A = 25^\circ\text{C}$, $f = 1 \text{ MHz}$, $V_{CC} = V_{CC(typ)}$ | 6 | pF |
| C_{OUT} | Output Capacitance | | 8 | pF |

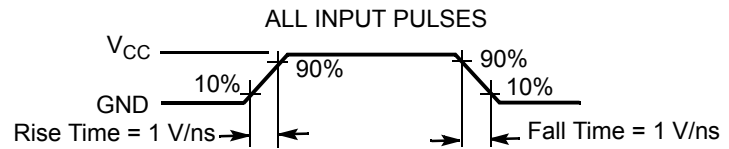
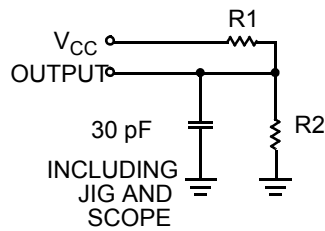
Notes

4. $V_{IL(min)}$ = -2.0V for pulse durations less than 20 ns.
5. $V_{IH(max)}$ = $V_{CC} + 0.75V$ for pulse durations less than 20 ns.
6. Full device AC operation requires linear V_{CC} ramp from 0 to $V_{CC(min)}$ and V_{CC} must be stable at $V_{CC(min)}$ for 500 μs .
7. Tested initially and after any design or process changes that may affect these parameters.

Thermal Resistance ^[7]

| Parameter | Description | Test Conditions | VFBGA | Unit |
|---------------|--|--|-------|------|
| Θ_{JA} | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 55 | °C/W |
| Θ_{JC} | Thermal Resistance (Junction to Case) | | 16 | °C/W |

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT

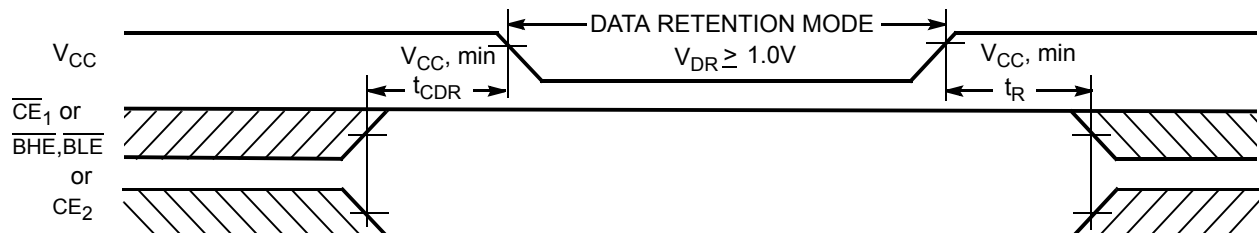


| Parameters | 1.8V | Unit |
|------------|-------|----------|
| R1 | 13500 | Ω |
| R2 | 10800 | Ω |
| R_{TH} | 6000 | Ω |
| V_{TH} | 0.80 | V |

Data Retention Characteristics (Over the Operating Range)

| Parameter | Description | Conditions | Min | Typ ^[2] | Max | Unit |
|-----------------|--------------------------------------|--|----------|--------------------|------|---------|
| V_{DR} | V_{CC} for Data Retention | | 1.0 | | 1.95 | V |
| I_{CCDR} | Data Retention Current | $V_{CC} = 1.0V$, $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | | | 10 | μA |
| $t_{CDR}^{[7]}$ | Chip Deselect to Data Retention Time | | 0 | | | ns |
| $t_R^{[8]}$ | Operation Recovery Time | | t_{RC} | | | ns |

Data Retention Waveform ^[9]



Notes

- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100 \mu s$ or stable at $V_{CC(min)} \geq 100 \mu s$.
- BHE.BLE is the AND of both BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling both BHE and BLE.

Switching Characteristics (Over the Operating Range)^[10]

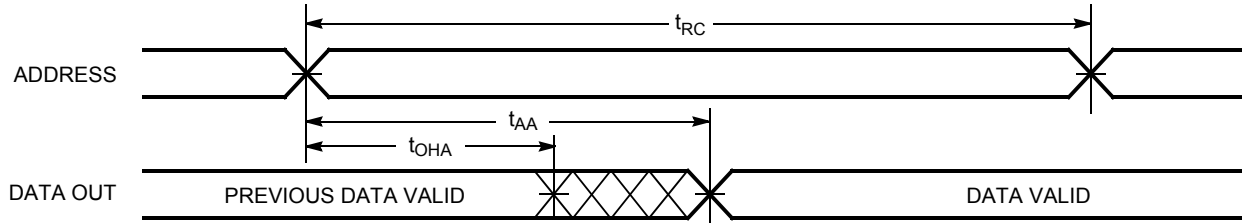
| Parameter | Description | 55 ns | | Unit |
|-----------------------------------|---|-------|-----|------|
| | | Min | Max | |
| Read Cycle | | | | |
| t_{RC} | Read Cycle Time | 55 | | ns |
| t_{AA} | Address to Data Valid | | 55 | ns |
| t_{OHA} | Data Hold from Address Change | 10 | | ns |
| t_{ACE} | \overline{CE}_1 LOW and CE_2 HIGH to Data Valid | | 55 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | | 25 | ns |
| t_{LZOE} | \overline{OE} LOW to LOW Z ^[11] | 5 | | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[11, 12] | | 20 | ns |
| t_{LZCE} | \overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[11] | 10 | | ns |
| t_{HZCE} | \overline{CE}_1 HIGH and CE_2 LOW to High Z ^[11, 12] | | 20 | ns |
| t_{PU} | \overline{CE}_1 LOW and CE_2 HIGH to Power up | 0 | | ns |
| t_{PD} | \overline{CE}_1 HIGH and CE_2 LOW to Power down | | 55 | ns |
| t_{DBE} | $\overline{BLE}/\overline{BHE}$ LOW to Data Valid | | 55 | ns |
| t_{LZBE} | $\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[11] | 5 | | ns |
| t_{HZBE} | $\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z ^[11, 12] | | 20 | ns |
| Write Cycle^[13] | | | | |
| t_{WC} | Write Cycle Time | 55 | | ns |
| t_{SCE} | \overline{CE}_1 LOW and CE_2 HIGH to Write End | 40 | | ns |
| t_{AW} | Address Setup to Write End | 40 | | ns |
| t_{HA} | Address Hold from Write End | 0 | | ns |
| t_{SA} | Address Setup to Write Start | 0 | | ns |
| t_{PWE} | \overline{WE} Pulse Width | 40 | | ns |
| t_{BW} | $\overline{BLE}/\overline{BHE}$ LOW to Write End | 45 | | ns |
| t_{SD} | Data Setup to Write End | 25 | | ns |
| t_{HD} | Data Hold from Write End | 0 | | ns |
| t_{HZWE} | \overline{WE} LOW to High- ^[11, 12] | | 20 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low-Z ^[11] | 10 | | ns |

Notes

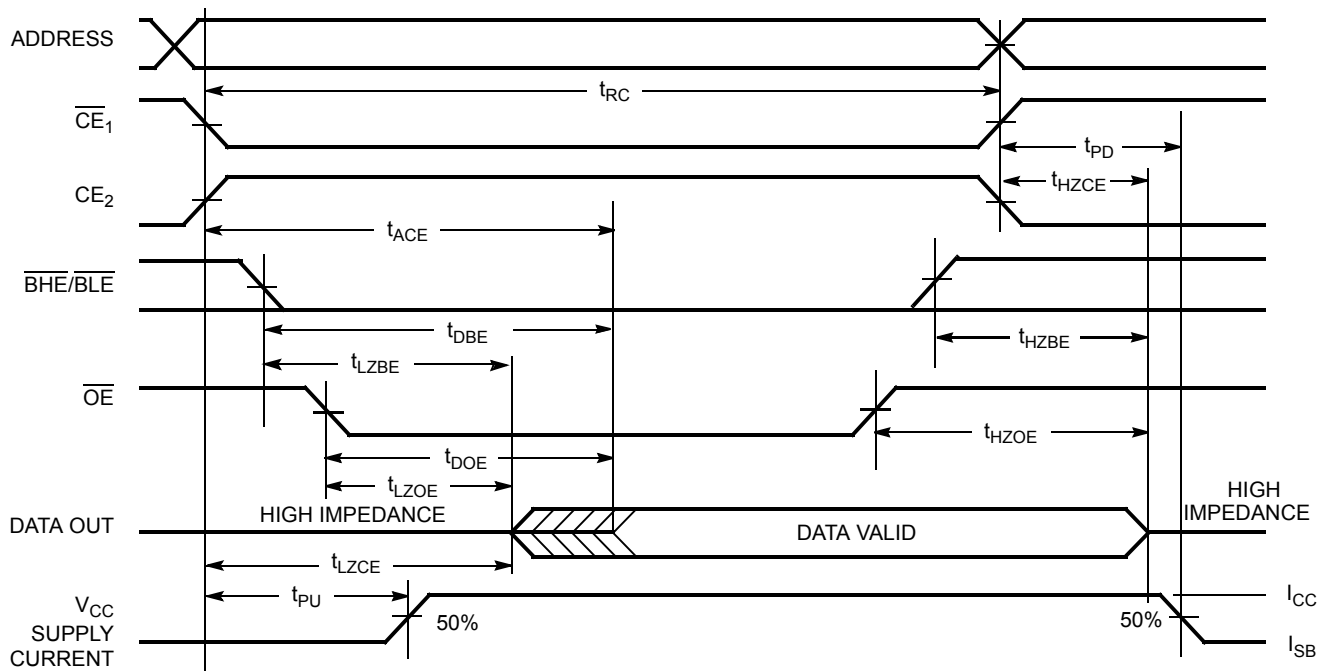
10. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 ns/V, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in "AC Test Loads and Waveforms" on page 4.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
13. The internal write time of the memory is defined by the overlap of \overline{WE} , $CE_1 = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)^[14, 15]



Read Cycle 2 ($\overline{\text{OE}}$ Controlled)^[15, 16]

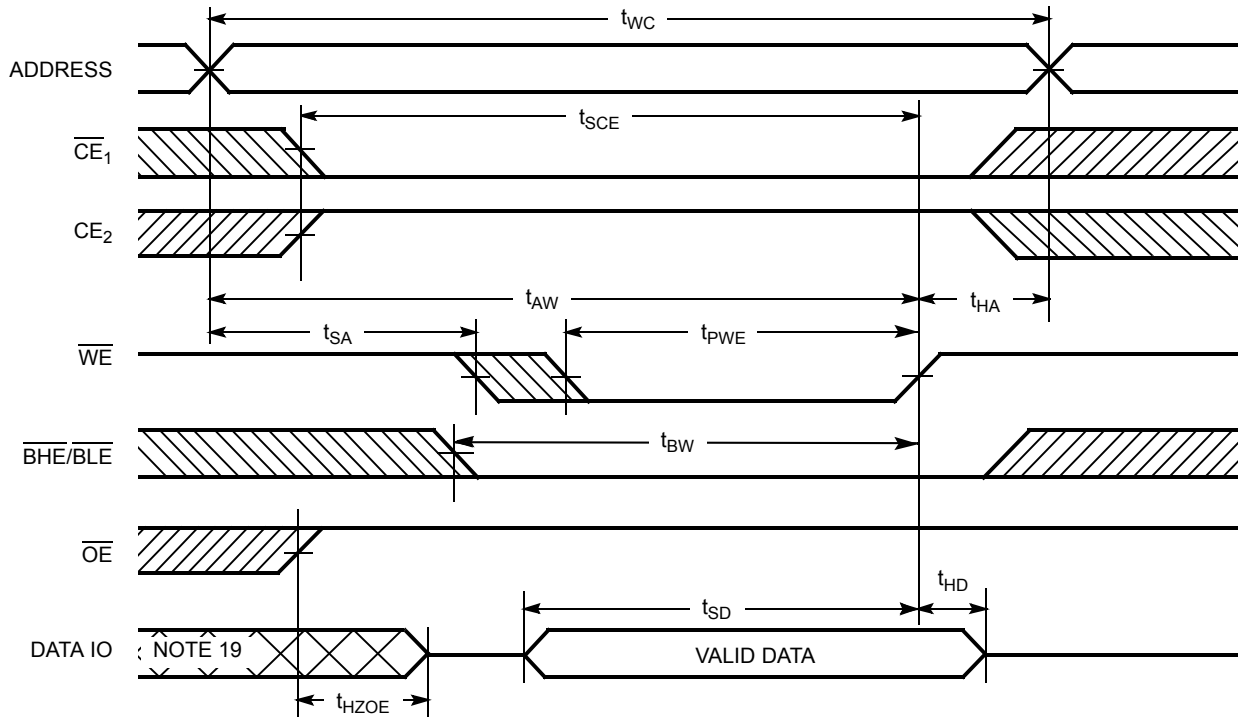


Notes

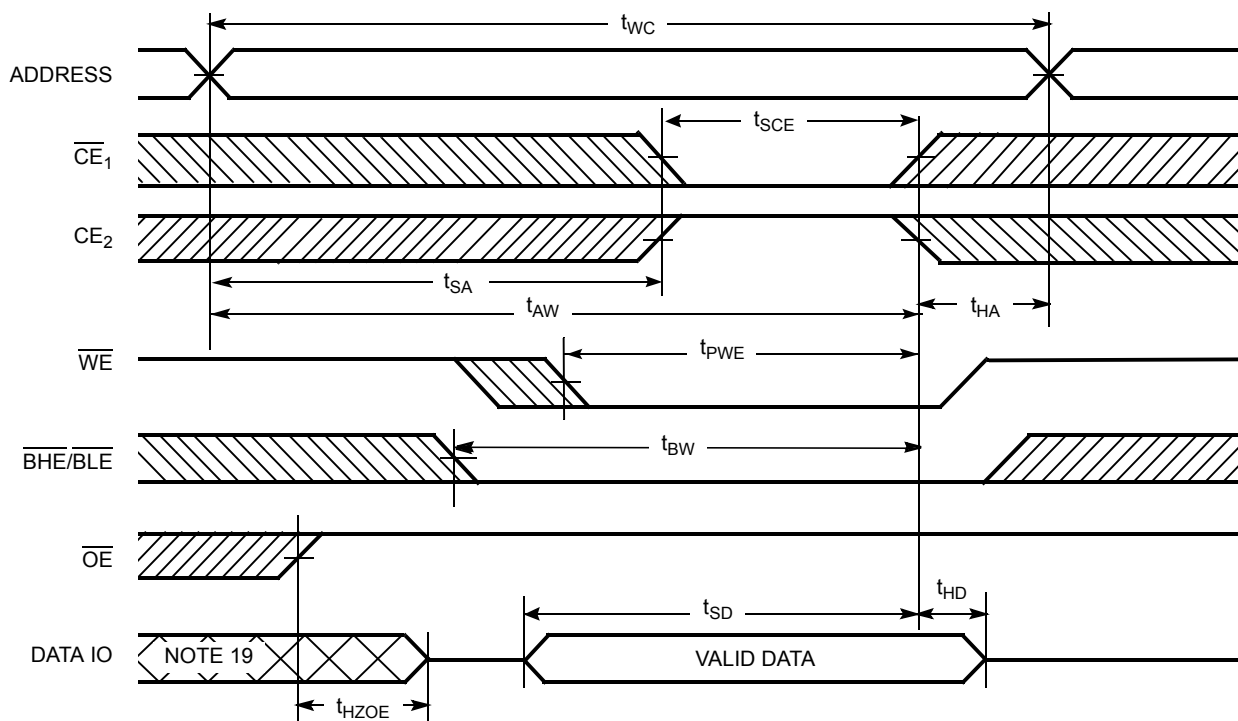
14. The device is continuously selected. $\overline{\text{OE}}$, $\overline{\text{CE}}_1 = V_{\text{IL}}$, $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IL}}$, and $\text{CE}_2 = V_{\text{IH}}$.
15. $\overline{\text{WE}}$ is HIGH for read cycle.
16. Address valid before or similar to $\overline{\text{CE}}_1$, $\overline{\text{BHE}}$, $\overline{\text{BLE}}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Write Cycle 1 (\overline{WE} Controlled)^[13, 17, 18]



Write Cycle 2 (\overline{CE}_1 or CE_2 Controlled)^[13, 17, 18]



Notes

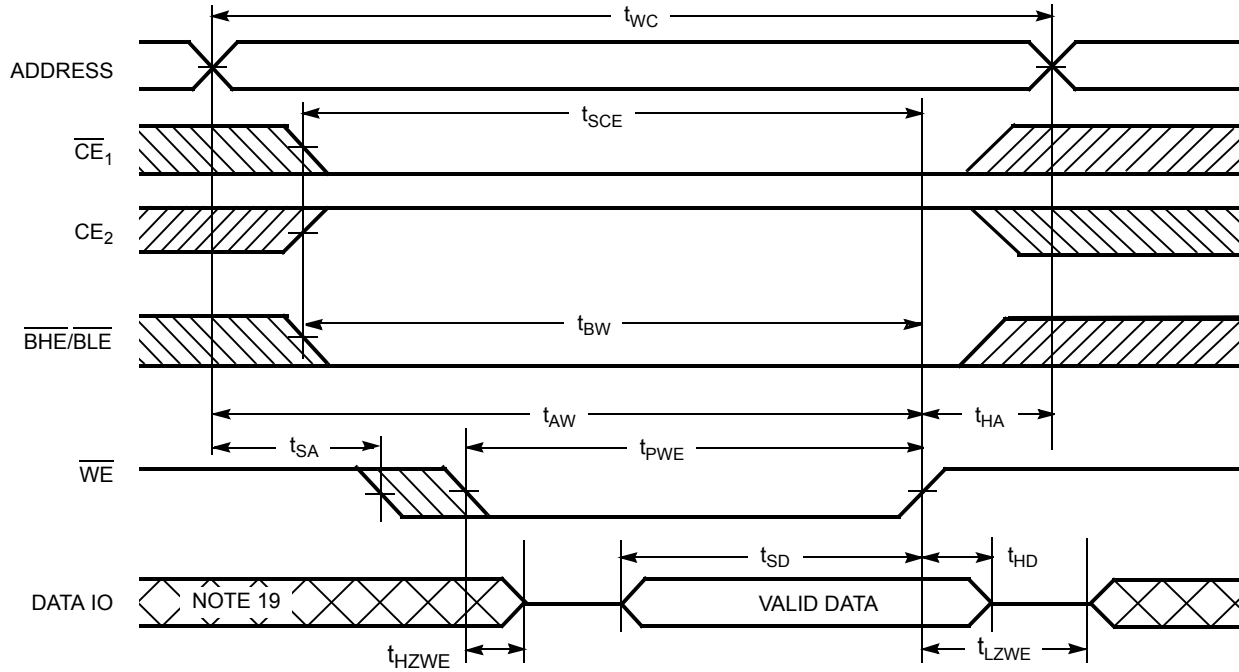
17. Data IO is high impedance if $\overline{OE} = V_{IH}$.

18. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.

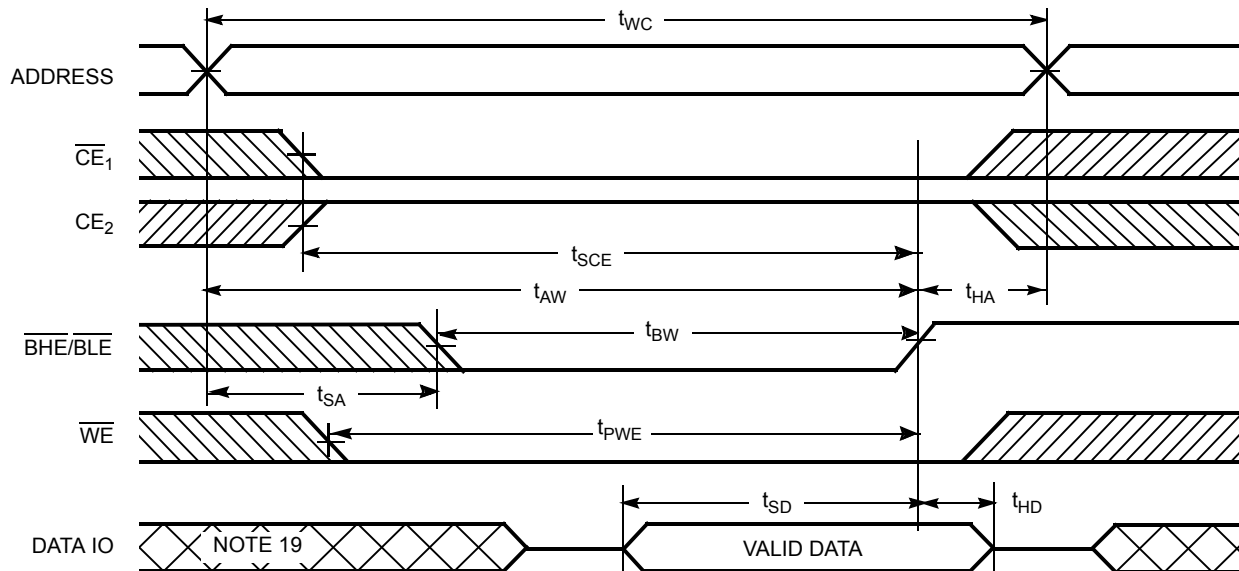
19. During this period, the IOs are in output state. Do not apply input signals.

Switching Waveforms (continued)

Write Cycle 3 (\overline{WE} Controlled, \overline{OE} LOW)^[18]



Write Cycle 4 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW)^[18]



Truth Table

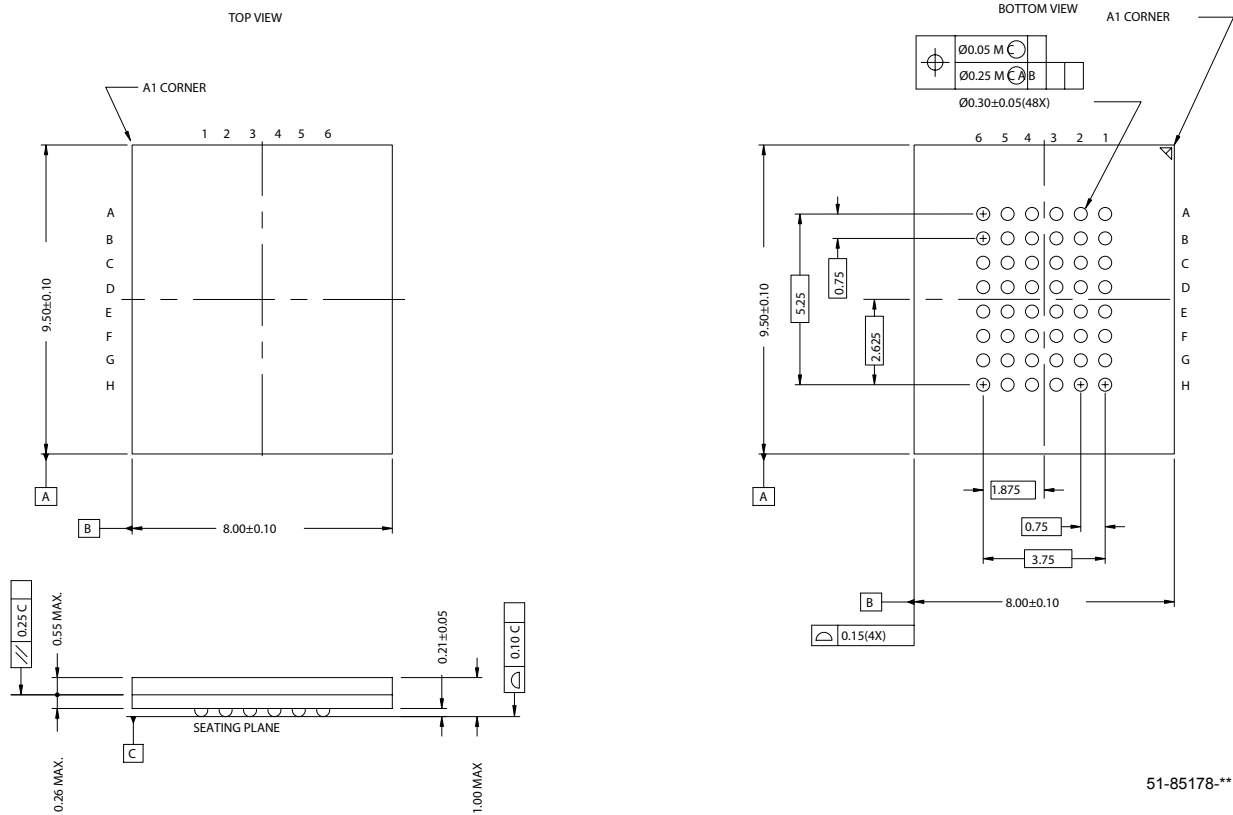
| \overline{CE}_1 | \overline{CE}_2 | \overline{WE} | \overline{OE} | \overline{BHE} | \overline{BLE} | Inputs/Outputs | Mode | Power |
|-------------------|-------------------|-----------------|-----------------|------------------|------------------|--|---------------------|----------------------|
| H | X | X | X | X | X | High Z | Deselect/Power Down | Standby (I_{SB}) |
| X | L | X | X | X | X | High Z | Deselect/Power Down | Standby (I_{SB}) |
| X | X | X | X | H | H | High Z | Deselect/Power Down | Standby (I_{SB}) |
| L | H | H | L | L | L | Data Out (IO_0 – IO_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | H | L | High Z (IO_8 – IO_{15}); Data Out (IO_0 – IO_7) | Read | Active (I_{CC}) |
| L | H | H | L | L | H | Data Out (IO_8 – IO_{15}); High Z (IO_0 – IO_7) | Read | Active (I_{CC}) |
| L | H | L | X | L | L | Data In (IO_0 – IO_{15}) | Write | Active (I_{CC}) |
| L | H | L | X | H | L | High Z (IO_8 – IO_{15}); Data In (IO_0 – IO_7) | Write | Active (I_{CC}) |
| L | H | L | X | L | H | Data In (IO_8 – IO_{15}); High Z (IO_0 – IO_7) | Write | Active (I_{CC}) |
| L | H | H | H | L | H | High Z | Output Disabled | Active (I_{CC}) |
| L | H | H | H | H | L | High Z | Output Disabled | Active (I_{CC}) |
| L | H | H | H | L | L | High Z | Output Disabled | Active (I_{CC}) |

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|----------------------|-----------------|---|-----------------|
| 55 | CY62167DV18LL-55BVXI | 51-85178 | 48-ball Fine Pitch BGA (8 x 9.5 x 1 mm) (Pb-free) | Industrial |

Package Diagrams

Figure 1. 48-Ball VFBGA (8 x 9.5 x 1 mm), 51-85178



51-85178-**

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Document History Page

| Document Title: CY62167DV18 MoBL [®] , 16-Mbit (1M x 16) Static RAM Document Number: 38-05326 | | | | |
|---|---------|------------|-----------------|--|
| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
| ** | 118406 | 09/30/02 | GUG | New Data Sheet |
| *A | 123690 | 02/11/03 | DPM | Changed Advance to Preliminary Added package diagram |
| *B | 126554 | 04/25/03 | DPM | Minor Change: Changed sunset owner from DPM to HRT |
| *C | 1015643 | See ECN | VKN | Converted from preliminary to final Removed "L" parts Removed 70 ns speed bin Updated footnote #3 Updated Ordering Information table |