

MOSFET – Dual, N-Channel, POWERTRENCH®

30 V, 9.5 mΩ and 20 mΩ

FDMC8200

General Description

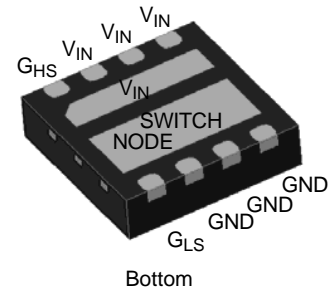
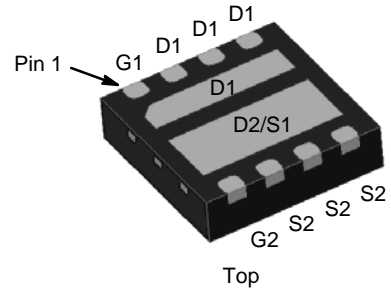
This device includes two specialized N-Channel MOSFETs in a dual Power33 (3 mm x 3 mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

Features

- Q1: N-Channel
 - ◆ Max $r_{DS(on)}$ = 20 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 6\text{ A}$
 - ◆ Max $r_{DS(on)}$ = 32 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 5\text{ A}$
- Q2: N-Channel
 - ◆ Max $r_{DS(on)}$ = 9.5 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 9\text{ A}$
 - ◆ Max $r_{DS(on)}$ = 13.5 mΩ at $V_{GS} = 4.5\text{ V}$, $I_D = 7\text{ A}$
- This Device is Pb-Free, Halide Free and is RoHS Compliant

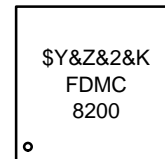
Applications

- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load



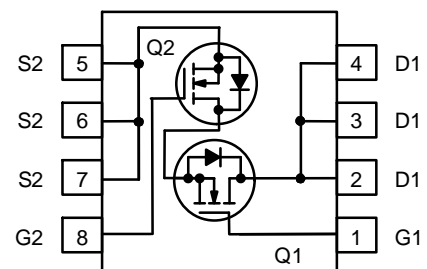
WDFN8 3x3, 0.65P
(Power 33)
CASE 511DE

MARKING DIAGRAM



- \$Y = Logo
- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code
- &K = 2-Digits Lot Run Traceability Code
- FDMC8200 = Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

FDMC8200

MOSFET MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter		Q1	Q2	Unit
V _{DS}	Drain to Source Voltage		30	30	V
V _{GS}	Gate to Source Voltage	(Note 3)	±20	±20	V
I _D	Drain Current – Continuous (Package Limited)	T _C = 25°C	18	18	A
	– Continuous (Silicon Limited)	T _C = 25°C	23	45	
	– Continuous	T _A = 25°C	8 (Note 1a)	12 (Note 1b)	
	– Pulsed		40	40	
P _D	Power Dissipation	T _A = 25°C	1.9 (Note 1a)	2.2 (Note 1b)	W
	Power Dissipation	T _A = 25°C	0.7 (Note 1c)	0.9 (Note 1d)	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		–55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter		Q1	Q2	Unit
R _{θJA}	Thermal Resistance, Junction to Ambient		65 (Note 1a)	55 (Note 1b)	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient		180 (Note 1c)	145 (Note 1d)	
R _{θJC}	Thermal Resistance, Junction to Case		7.5	4	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	Q1	30	–	–	V
		I _D = 250 μA, V _{GS} = 0 V	Q2	30	–	–	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	Q1	–	14	–	mV/°C
		I _D = 250 μA, referenced to 25°C	Q2	–	14	–	
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	Q1	–	–	1	μA
		V _{DS} = 24 V, V _{GS} = 0 V	Q2	–	–	1	
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V	Q1	–	–	100	nA
			Q2	–	–	100	

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	Q1	1.0	2.3	3.0	V
		V _{GS} = V _{DS} , I _D = 250 μA	Q2	1.0	2.3	3.0	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C	Q1	–	–5	–	mV/°C
		I _D = 250 μA, referenced to 25°C	Q2	–	–6	–	
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 6 A V _{GS} = 4.5 V, I _D = 5 A	Q1	–	16	20	mΩ
				–	24	32	
		V _{GS} = 10 V, I _D = 6 A, T _J = 125°C	Q2	–	7.3	9.5	
				–	9.5	13.5	
V _{GS} = 10 V, I _D = 9 A V _{GS} = 4.5 V, I _D = 7 A V _{GS} = 10 V, I _D = 9 A, T _J = 125°C	Q2	–	10	13			
		–	10	13			
g _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 6 A V _{DD} = 5 V, I _D = 9 A	Q1	–	29	–	S
			Q2	–	56	–	

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	Q1	–	495	660	pF
			Q2	–	1180	1570	
C _{oss}	Output Capacitance		Q1	–	145	195	pF
			Q2	–	330	440	
C _{rss}	Reverse Transfer Capacitance		Q1	–	20	30	pF
			Q2	–	30	45	

FDMC8200

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
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DYNAMIC CHARACTERISTICS

R _g	Gate Resistance	f = 1 MHz	Q1	–	1.4	–	Ω
			Q2	–	1.4	–	

SWITCHING CHARACTERISTICS

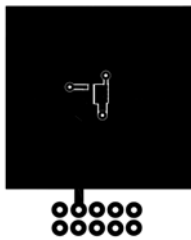
t _{d(on)}	Turn-On Delay Time	Q1 V _{DD} = 15 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω Q2 V _{DD} = 15 V, I _D = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω	Q1	–	11	20	ns
t _r	Rise Time		Q1	–	3.1	10	
t _{d(off)}	Turn-Off Delay Time		Q2	–	4	10	
t _f	Fall Time		Q1	–	35	56	
			Q2	–	38	60	
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 10 V Q1: V _{DD} = 15 V, I _D = 6 A Q2: V _{DD} = 15 V, I _D = 9 A	Q1	–	7.3	10	nC
			Q2	–	16	22	
Q _{g(TOT)}	Total Gate Charge	V _{GS} = 0 V to 4.5 V Q1: V _{DD} = 15 V, I _D = 6 A Q2: V _{DD} = 15 V, I _D = 9 A	Q1	–	3.1	4.3	nC
			Q2	–	7	10	
Q _{gs}	Gate to Source Charge	Q1: V _{DD} = 15 V, I _D = 6 A	Q1	–	1.8	–	nC
			Q2	–	4.1	–	
Q _{gd}	Gate to Drain "Miller" Charge	Q2: V _{DD} = 15 V, I _D = 9 A	Q1	–	1	–	nC
			Q2	–	1.5	–	

DRAIN-SOURCE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 6 A (Note 2) V _{GS} = 0 V, I _S = 9 A (Note 2)	Q1	–	0.8	1.2	V
			Q2	–	0.8	1.2	
t _{rr}	Reverse Recovery Time	Q1 I _F = 6 A, di/dt = 100 A/μS	Q1	–	13	24	ns
			Q2	–	21	34	
Q _{rr}	Reverse Recovery Charge	Q2 I _F = 9 A, di/dt = 100 A/μS	Q1	–	2.3	10	nC
			Q2	–	5.6	12	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

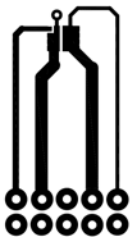
- R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



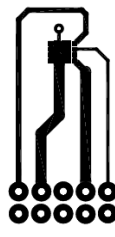
- 65°C/W when mounted on a 1 in² pad of 2 oz copper



- 55°C/W when mounted on a 1 in² pad of 2 oz copper



- 180°C/W when mounted on a minimum pad of 2 oz copper



- 145°C/W when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- As an N-ch device, the negative V_{gs} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted)

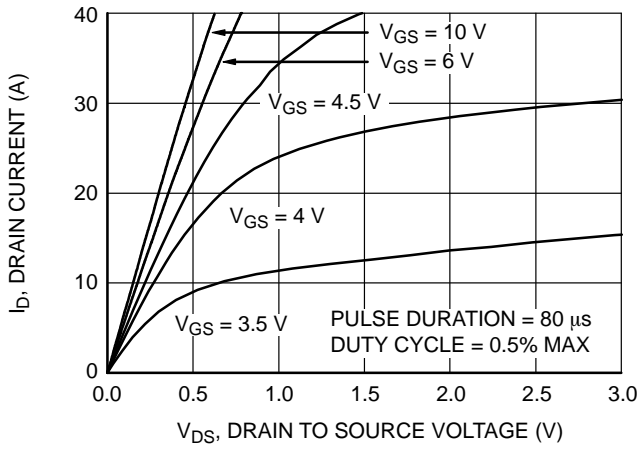


Figure 1. On Region Characteristics

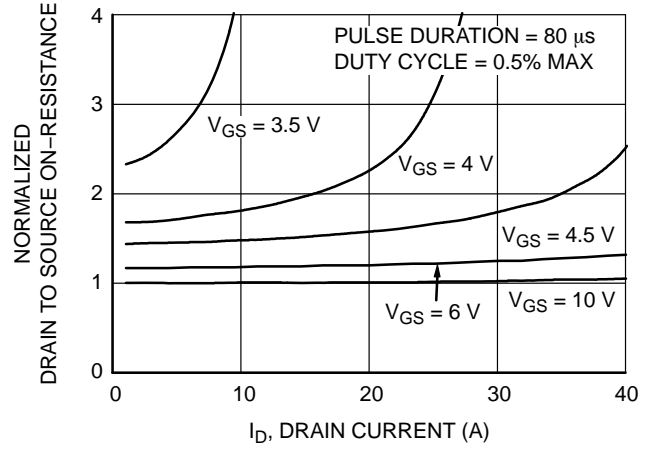


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

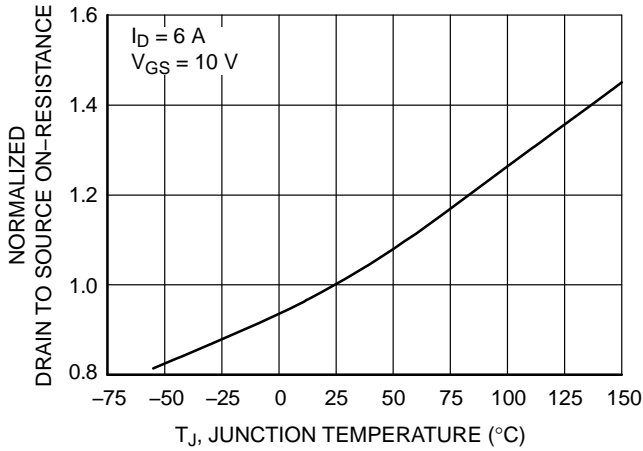


Figure 3. Normalized On Resistance vs. Junction Temperature

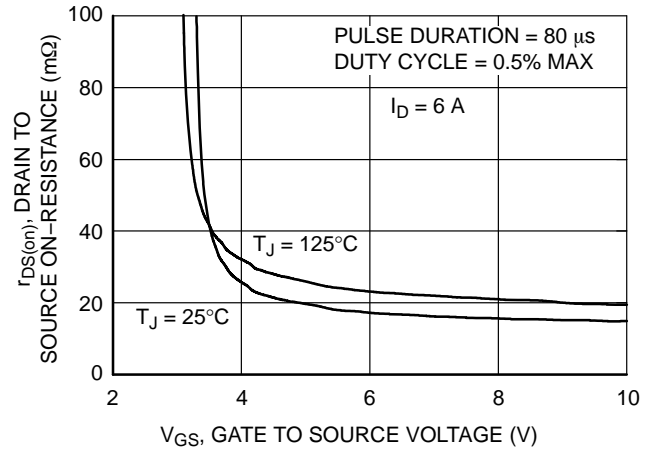


Figure 4. On-Resistance vs. Gate to Source Voltage

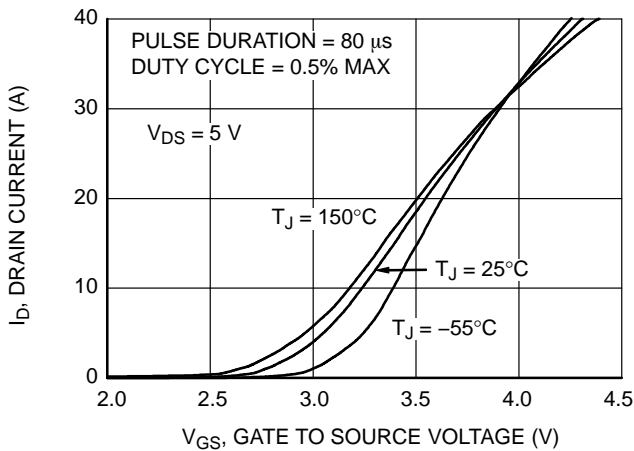


Figure 5. Transfer Characteristics

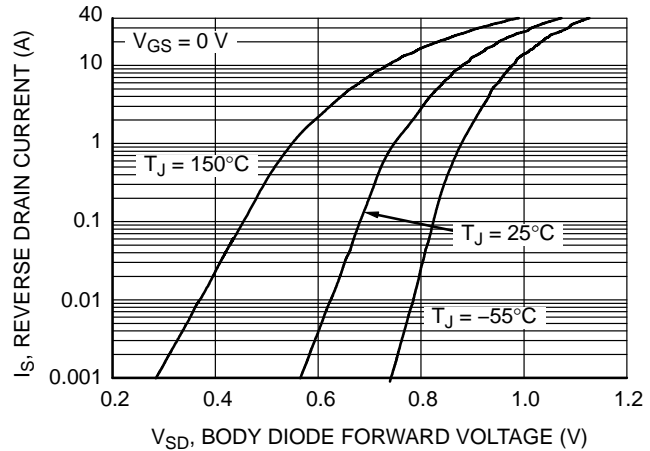


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

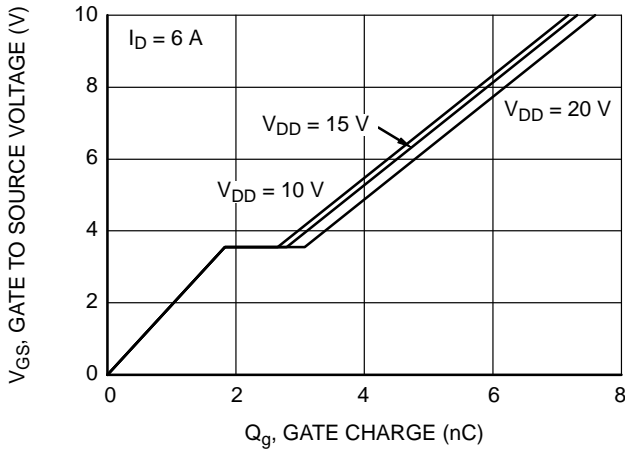


Figure 7. Gate Charge Characteristics

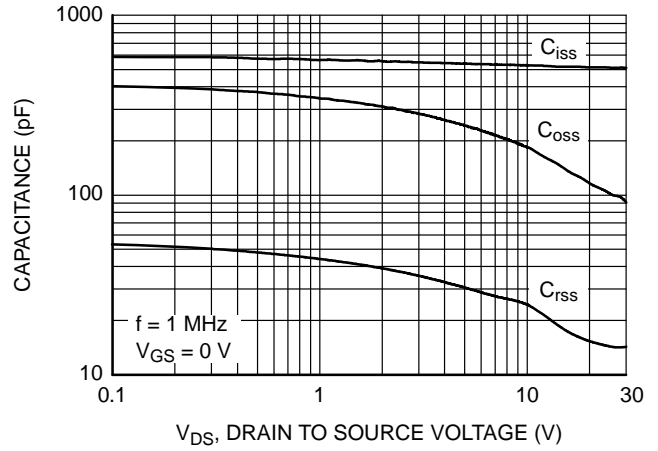


Figure 8. Capacitance vs. Drain to Source Voltage

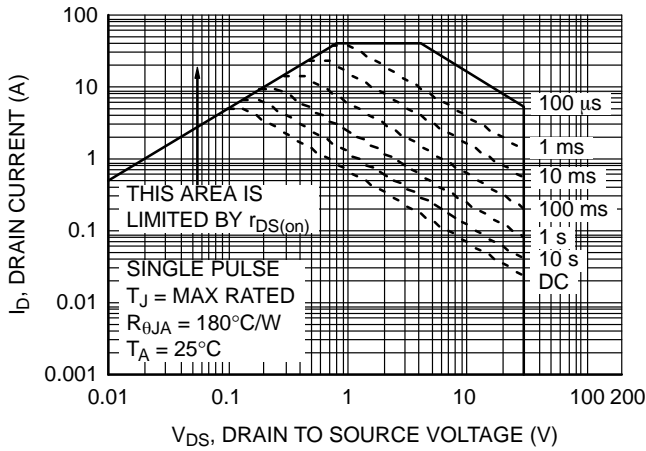


Figure 9. Forward Bias Safe Operating Area

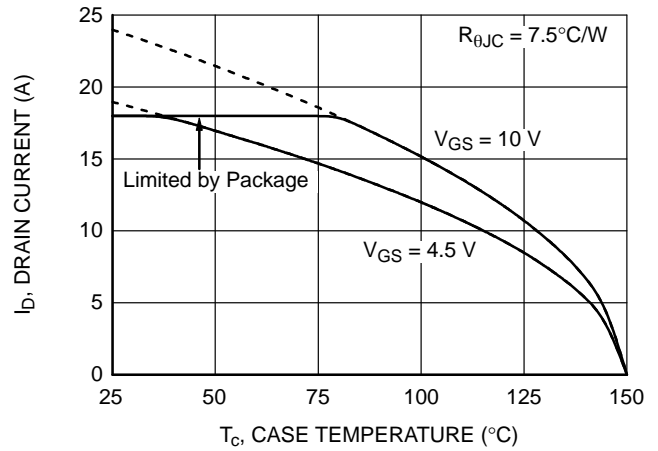


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

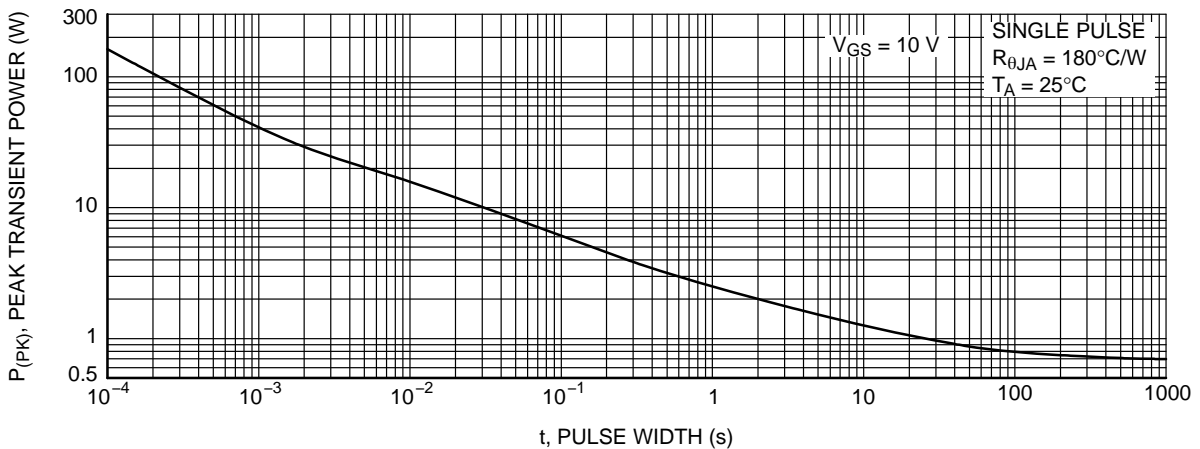


Figure 11. Single Pulse Maximum Power Dissipation

FDMC8200

TYPICAL CHARACTERISTICS (Q1 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

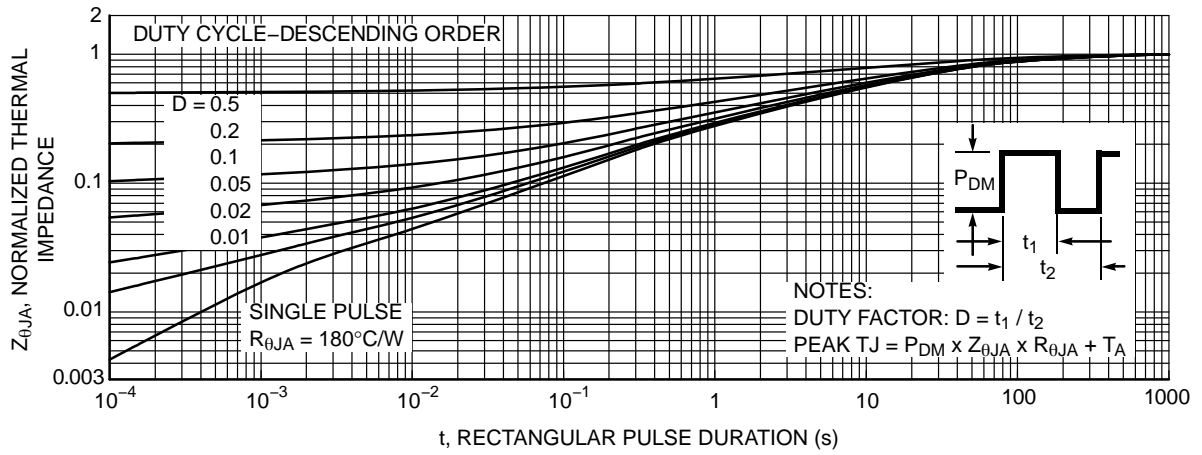


Figure 12. Junction-to-Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted)

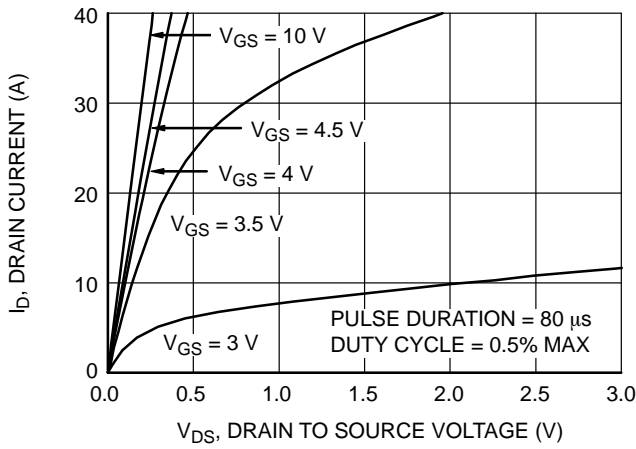


Figure 13. On-Region Characteristics

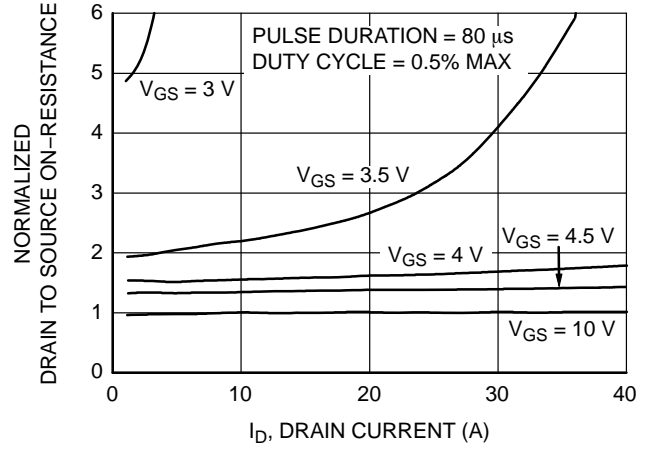


Figure 14. Normalized On-Resistance vs. Drain Current and Gate Voltage

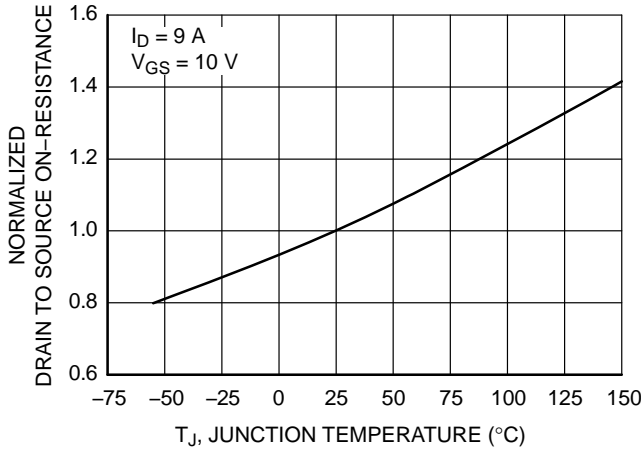


Figure 15. Normalized On Resistance vs. Junction Temperature

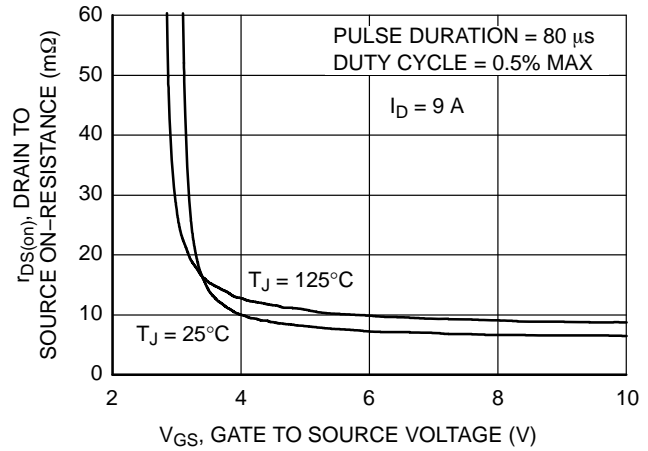


Figure 16. On-Resistance vs. Gate to Source Voltage

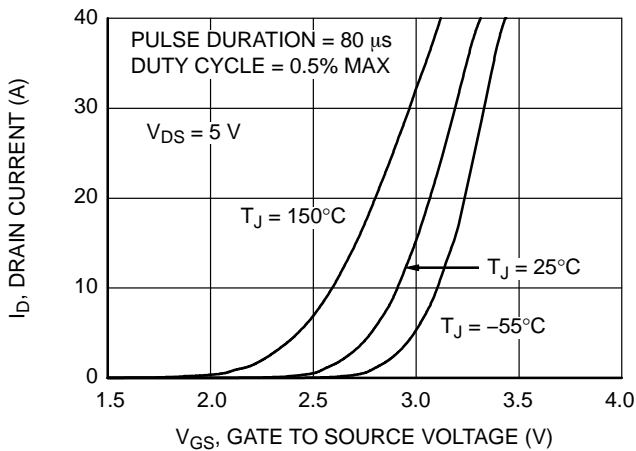


Figure 17. Transfer Characteristics

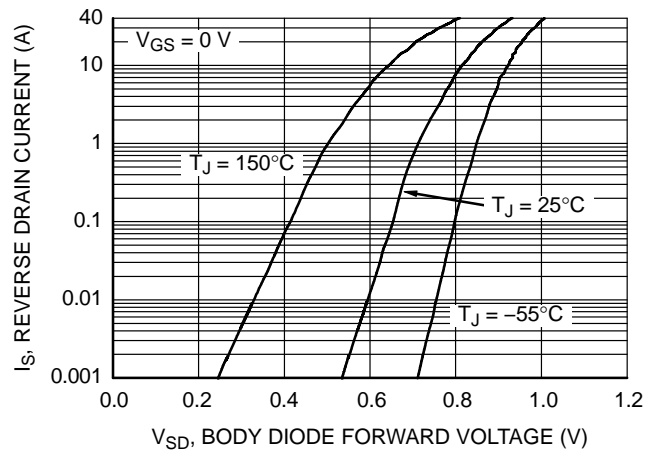


Figure 18. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

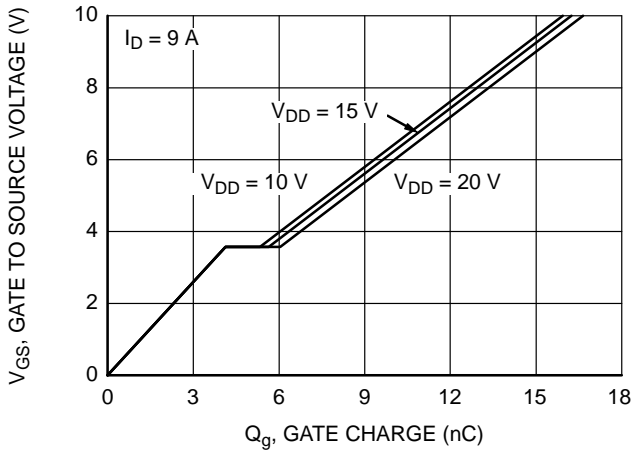


Figure 19. Gate Charge Characteristics

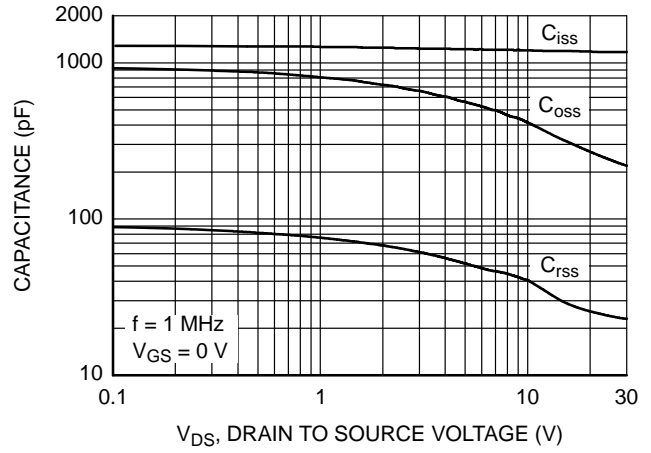


Figure 20. Capacitance vs. Drain to Source Voltage

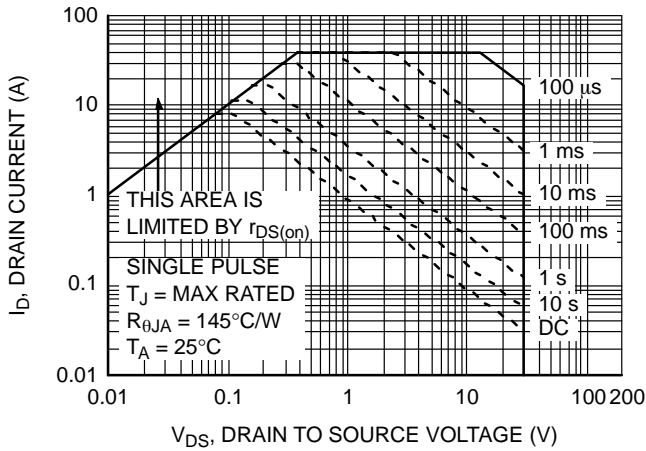


Figure 21. Forward Bias Safe Operating Area

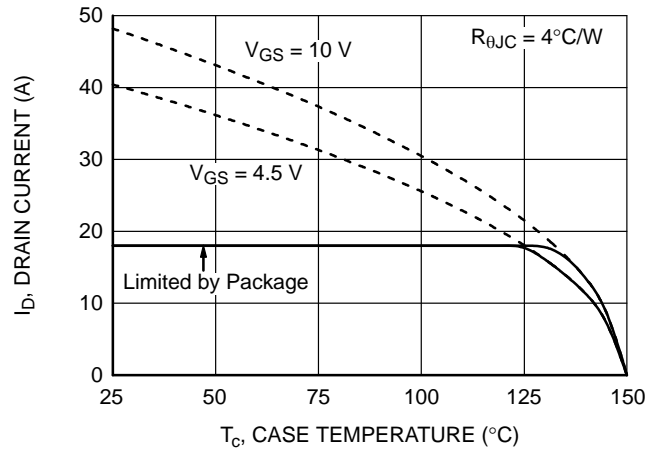


Figure 22. Maximum Continuous Drain Current vs. Case Temperature

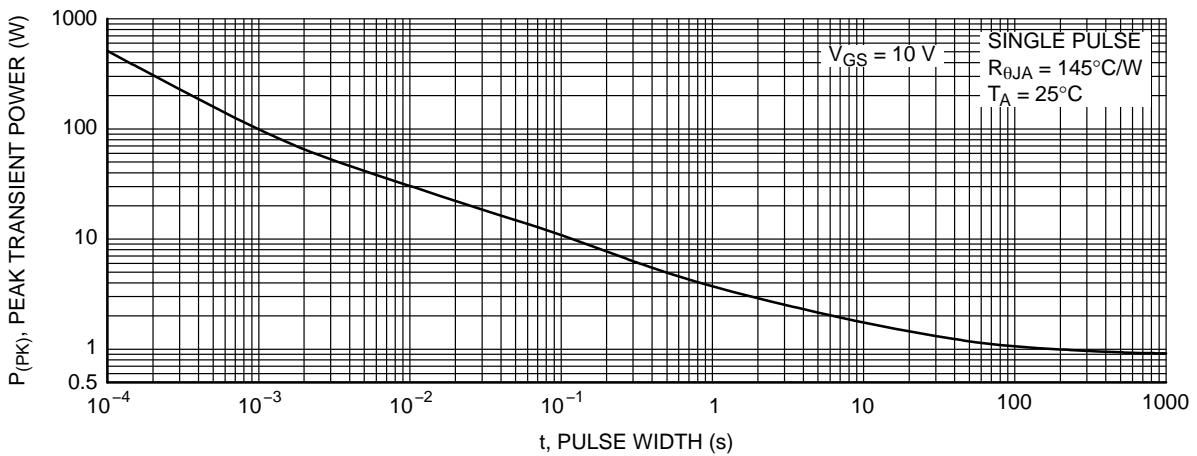


Figure 23. Single Pulse Maximum Power Dissipation

FDMC8200

TYPICAL CHARACTERISTICS (Q2 N-CHANNEL) ($T_J = 25^\circ\text{C}$, unless otherwise noted) (continued)

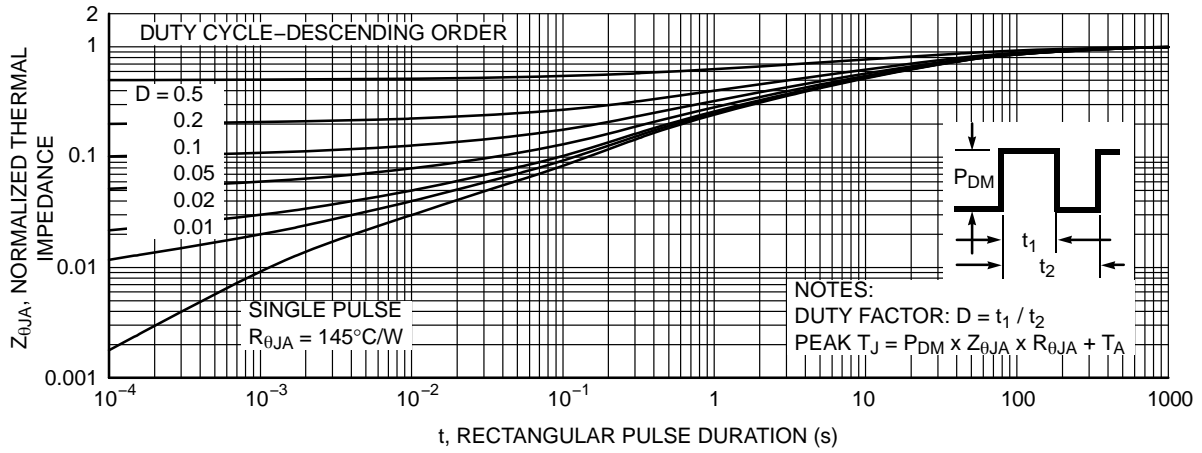


Figure 24. Junction-to-Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

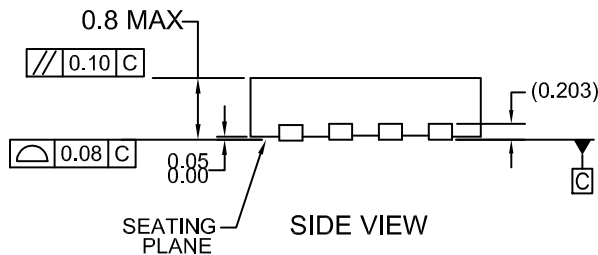
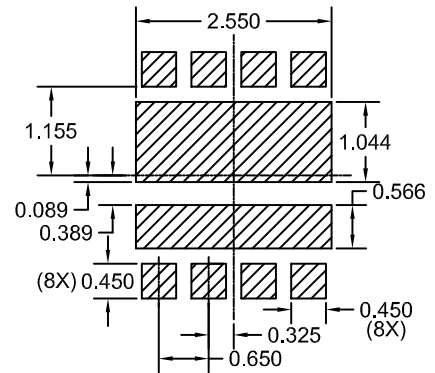
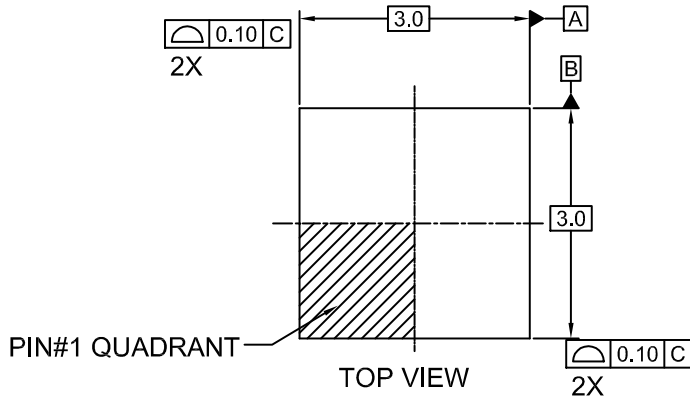
Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDMC8200	FDMC8200	WDFN8 3x3, 0.65P (Power 33) (Pb-Free, Halide Free)	13"	12 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

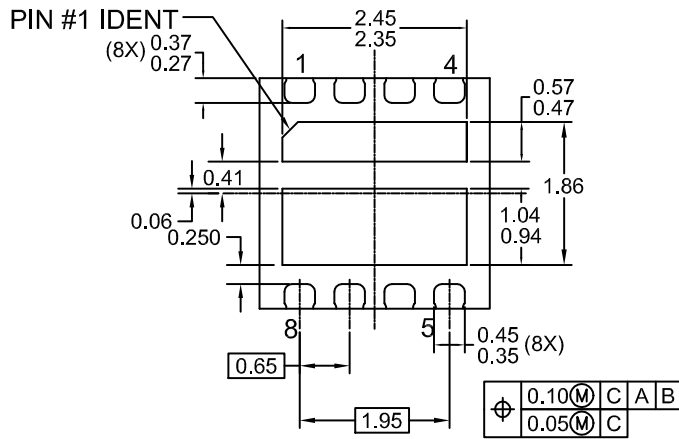
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

WDFN8 3x3, 0.65P
CASE 511DE
ISSUE O

DATE 31 AUG 2016



RECOMMENDED LAND PATTERN



BOTTOM VIEW

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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DESCRIPTION:	WDFN8 3X3, 0.65P	PAGE 1 OF 1

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