

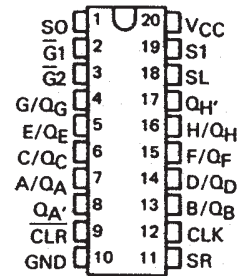
SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

SDLS156 – MARCH 1974 – REVISED MARCH 1988

- Multiplexed Inputs/Outputs Provide Improved Bit Density
- Four Modes of Operations:

Hold (Store)	Shift Left
Shift Right	Load Data
- Operates with Outputs Enabled or at High Z
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- SN54LS323 and SN74LS323 Are Similar But Have Synchronous Clear

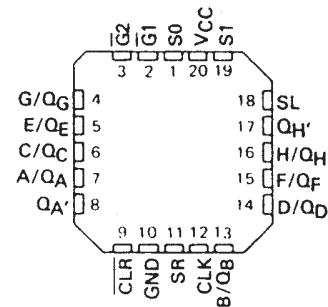
SN54LS299, SN54S299 . . . J OR W PACKAGE
SN74LS299, SN74S299 . . . DW OR N PACKAGE
(TOP VIEW)



- Applications:
 - Stacked or Push-Down Registers
 - Buffer Storage, and Accumulator Registers

TYPE	GUARANTEED	TYPICAL
	SHIFT (CLOCK) FREQUENCY	POWER DISSIPATION
'LS299	25 MHz	175 mW
'S299	50 MHz	700 mW

SN54LS299, SN54S299 . . . FK PACKAGE
(TOP VIEW)



description

These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

FUNCTION TABLE

MODE	INPUTS						INPUTS/OUTPUTS								OUTPUTS			
	CLR	FUNCTION SELECT		OUTPUT CONTROL		CLK	SERIAL		A/QA	B/QB	C/QC	D/QD	E/QE	F/QF	G/QG	H/QH	QA'	QH'
		S1	S0	G1†	G2†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Hold	H	L	L	L	L	X	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
	H	X	X	L	L	L	X	X	QA0	QB0	QC0	QD0	QE0	QF0	QG0	QH0	QA0	QH0
Shift Right	H	L	H	L	L	†	X	H	H	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	H	QH _n
	H	L	H	L	L	†	X	L	L	QA _n	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	L	QH _n
Shift Left	H	H	L	L	L	†	H	X	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	H	QB _n	H
	H	H	L	L	L	†	L	X	QB _n	QC _n	QD _n	QE _n	QF _n	QG _n	QH _n	L	QB _n	L
Load	H	H	H	X	X	†	X	X	a	b	c	d	e	f	g	h	a	h

† When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



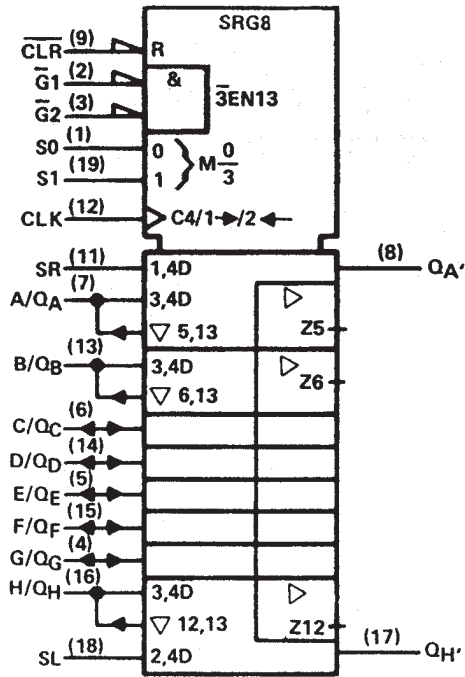
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SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

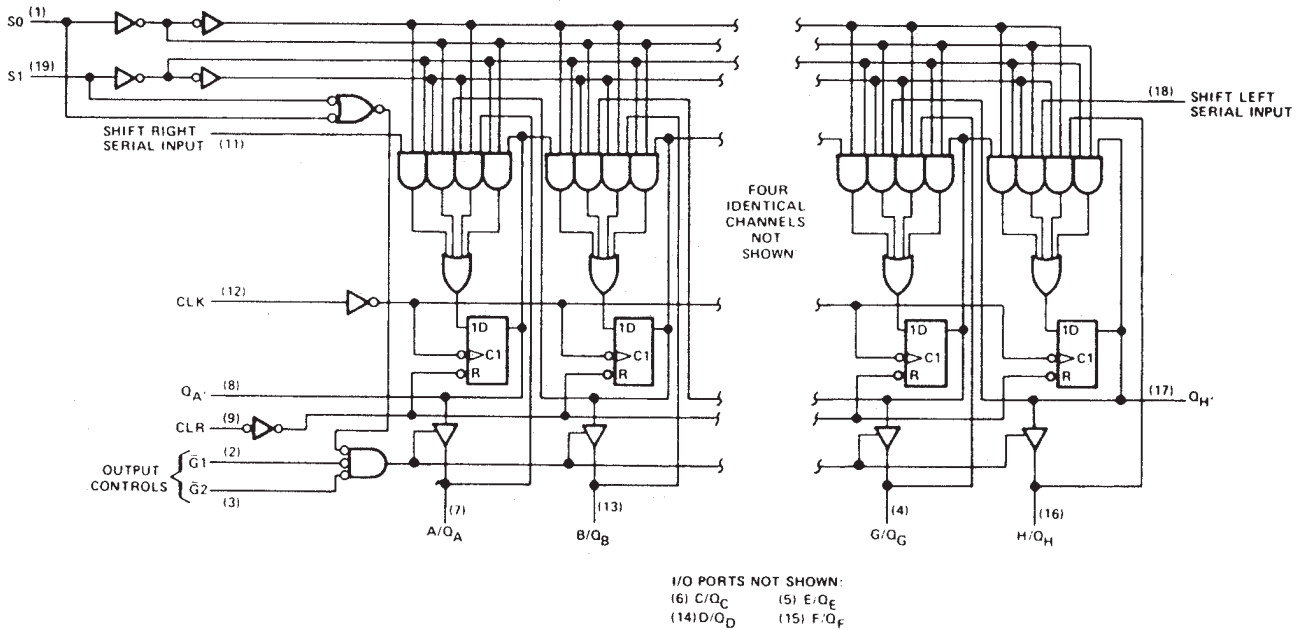
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

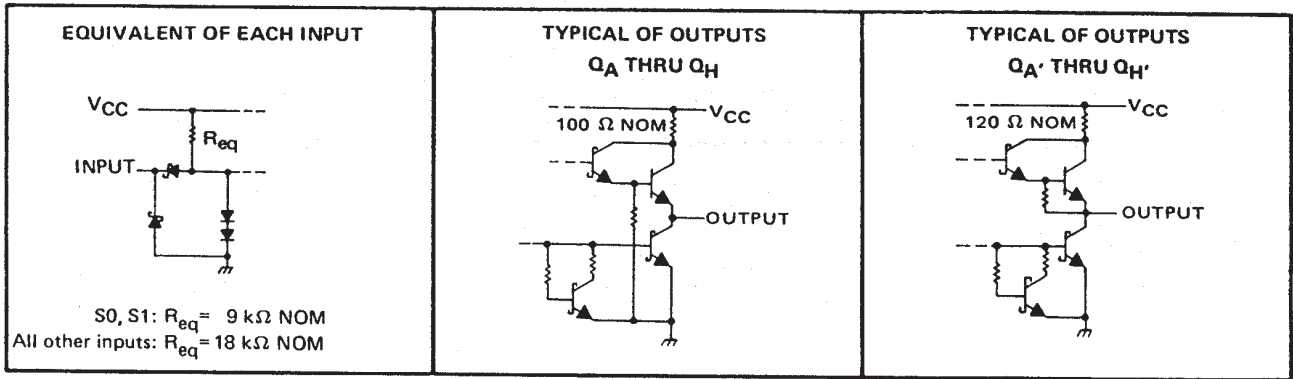


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SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS299	-55°C to 125°C
SN74LS299	0°C to 70°C
Storage temperature	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS299			SN74LS299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			-1			-2.6	mA
	Q_A' or Q_H'			-0.4			-0.4	
Low-level output current, I_{OL}	Q_A thru Q_H			12			24	mA
	Q_A' or Q_H'			4			8	
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock pulse, $t_w(\text{clock})$	Clock high	30			30			ns
	Clock low	18			10			
Width of clear pulse, $t_w(\text{clear})$	Clear low	25			20			ns
	Clear high							
Setup time, t_{su}	Select	35 [†]			35 [†]			ns
	High-level data [†]	20 [†]			20 [†]			
	Low-level data [†]	20 [†]			20 [†]			
	Clear inactive-state	24 [†]			20 [†]			
Hold time, t_h	Select	10 [†]			10 [†]			ns
	Data [†]	3 [†]			0 [†]			
Operating free-air temperature, T_A		-55		125	0		70	$^{\circ}\text{C}$

[†] Data includes the two serial inputs and the eight input/output data lines.

SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS299		SN74LS299		UNIT			
			MIN	TYP‡	MAX	MIN		TYP‡	MAX	
V _{IH}	High-level input voltage		2		2		V			
V _{IL}	Low-level input voltage				0.7	0.8	V			
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.5	-1.5	V			
V _{OH}	High-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V,		2.4	3.2	2.4	3.1	V	
		Q _A ' or Q _H '	V _{IL} = V _{ILmax} , I _{OH} = MAX		2.5	3.4	2.7	3.4		
V _{OL}	Low-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{ILmax}	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V	
				I _{OL} = 24 mA			0.35	0.5		
		Q _A ' or Q _H '		I _{OL} = 4 mA	0.25	0.4	0.25	0.4		
				I _{OL} = 8 mA			0.35	0.5		
I _{OZH}	Off-state output current, high-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _O = 2.7 V, V _{IH} = 2 V,		40		40	μA		
I _{OZL}	Off-state output current, low-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _O = 0.4 V, V _{IH} = 2 V,		-400		-400	μA		
I _I	Input current at maximum input voltage	S0, S1	V _{CC} = MAX	V _I = 7 V		200		200	μA	
		A thru H		V _I = 5.5 V		100		100		
		Any other		V _I = 7 V		100		100		
I _{IH}	High-level input current	A thru H, S0, S1	V _{CC} = MAX, V _I = 2.7 V			40		40	μA	
		Any other				20		20		
I _{IL}	Low-level input current	S0, S1	V _{CC} = MAX, V _I = 0.4 V			-0.8		-0.8	mA	
		Any other				-0.4		-0.4		
I _{OS}	Short-circuit output current§	Q _A thru Q _H	V _{CC} = MAX		-30	-130	-30	-130	mA	
		Q _A ' or Q _H '			-20	-100	-20	-100		
I _{CC}	Supply current		V _{CC} = MAX		33	53		33	53	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			See Note 2	20	35		MHz
t _{PLH}	CLK	Q _A ' or Q _H '	R _L = 2 kΩ, C _L = 15 pF		22	33	ns
t _{PHL}					26	39	
t _{PHL}		CLR		Q _A ' or Q _H '		27	40
t _{PLH}	CLK	Q _A thru Q _H	R _L = 665 Ω, C _L = 45 pF		17	25	ns
t _{PHL}					26	39	
t _{PHL}				CLR	Q _A thru Q _H		26
t _{PZH}	G1, G2	Q _A thru Q _H			13	21	ns
t _{PZL}					19	30	
t _{PHZ}	G1, G2	Q _A thru Q _H	R _L = 665 Ω, C _L = 5 pF		10	20	ns
t _{PLZ}					10	15	

¶ f_{max} ≡ maximum clock frequency

t_{PLH} ≡ propagation delay time, low-to-high-level output.

t_{PHL} ≡ propagation delay time, high-to-low-level output

t_{PZH} ≡ output enable time to high level

t_{PZL} ≡ output enable time to low level

t_{PHZ} ≡ output disable time from high level

t_{PLZ} ≡ output disable time from low level

NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.

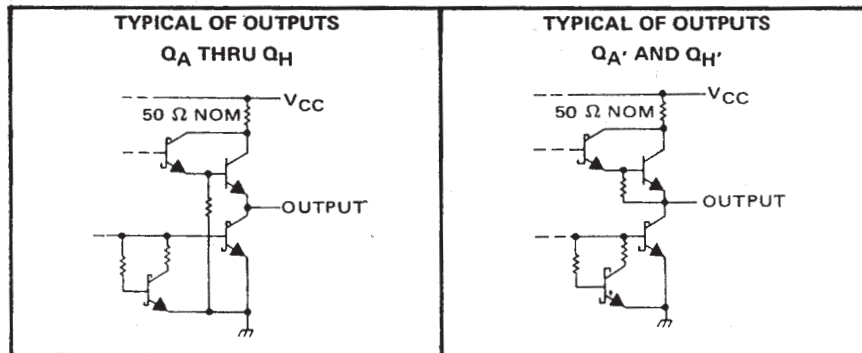
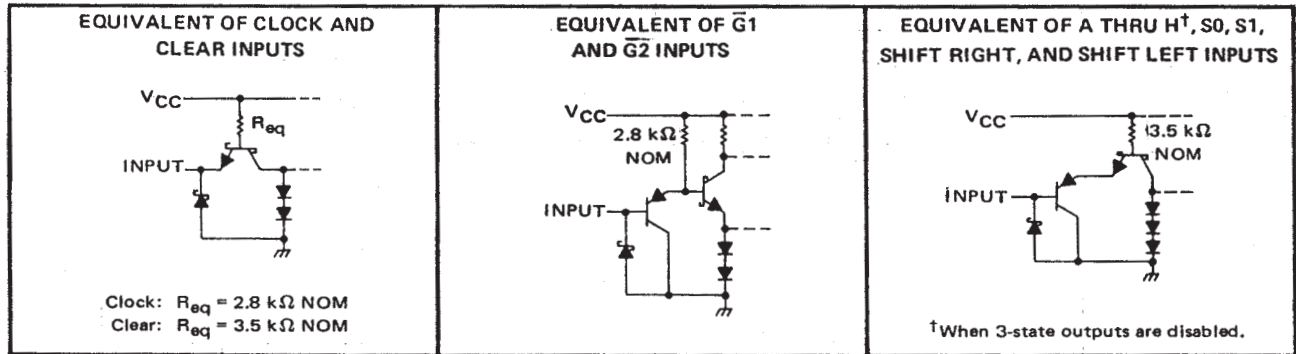


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SN54LS299, SN54S299, SN74LS299, SN74S299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS

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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54S299 (See Note 1)	-55 °C to 125 °C
SN74S299	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S299			SN74S299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Q_A thru Q_H			-2			-6.5	mA
	$Q_{A'}$ or $Q_{H'}$			-0.5			-0.5	
Low-level output current, I_{OL}	Q_A thru Q_H			20			20	mA
	$Q_{A'}$ or $Q_{H'}$			6			6	
Clock frequency, f_{clock}		0		50	0		50	MHz
Width of clock pulse, $t_{w(clock)}$	Clock high	10			10			ns
	Clock low	10			10			
Width of clear pulse, $t_{w(clear)}$	Clear low	10			10			ns
Setup time, t_{su}	Select	15 †			15 †			ns
	High-level data †	7 †			7 †			
	Low-level data †	5 †			5 †			
	Clear inactive-state	10 †			10 †			
Hold time, t_h	Select	5 †			5 †			ns
	Data †	5 †			5 †			
Operating free-air temperature, T_A		-55		125	0		70	°C

† Data includes the two serial inputs and the eight input/output data lines.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V _{IH}	High-level input voltage		2			V
V _{IL}	Low-level input voltage				0.8	V
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = -18 mA			-1.2	V
V _{OH}	High-level output voltage	Q _A thru Q _H	V _{CC} = MIN, V _{IH} = 2 V,	2.4	3.2	V
		Q _A ' or Q _H '	V _{IL} = 0.8 V, I _{OH} = MAX	2.7	3.4	
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = MAX			0.5	V
I _{OZH}	Off-state output current, high-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 2.4 V		100	μA
I _{OZL}	Off-state output current, low-level voltage applied	Q _A thru Q _H	V _{CC} = MAX, V _{IH} = 2 V, V _O = 0.5 V		-250	μA
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH}	High-level input current	A thru H, S ₀ , S ₁	V _{CC} = MAX, V _I = 2.7 V		100	μA
		Any other			50	
I _{IL}	Low-level input current	CLK or CLR	V _{CC} = MAX, V _I = 0.5 V		-2	mA
		S ₀ , S ₁			-500	μA
		Any other			-250	μA
I _{OS}	Short-circuit output current §	Q _A thru Q _H	V _{CC} = MAX		-40	mA
		Q _A ' or Q _H '			-20	
I _{CC}	Supply current	V _{CC} = MAX		140	225	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f _{max}			See Note 2	50	70		MHz
t _{PLH}	CLK	Q _A ' or Q _H '	R _L = 1 kΩ, C _L = 15 pF		12	20	ns
t _{PHL}					13	20	
t _{PHL}	CLR	Q _A ' or Q _H '			14	21	ns
t _{PLH}	CLK	Q _A thru Q _H	R _L = 280 Ω, C _L = 45 pF		15	21	ns
t _{PHL}					15	21	
t _{PHL}	CLR	Q _A thru Q _H	R _L = 280 Ω, C _L = 45 pF		16	24	ns
t _{PZH}					10	18	
t _{PZL}	G ₁ , G ₂	Q _A thru Q _H	R _L = 280 Ω, C _L = 5 pF		12	18	ns
t _{PHZ}					7	12	
t _{PLZ}	G ₁ , G ₂	Q _A thru Q _H	R _L = 280 Ω, C _L = 5 pF		7	12	ns

¶ f_{max} = maximum clock frequency

t_{PLH} = Propagation delay time, low-to-high-level output

t_{PHL} = Propagation delay time, high-to-low-level output

t_{PZH} = output enable time to high level

t_{PZL} = output enable time to low level

t_{PHZ} = output disable time from high level

t_{PLZ} = output disable time from low level

NOTE 2: For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

Load circuits and voltage waveforms are shown in Section 1.



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
78024012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK	Samples
7802401RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J	Samples
7802401RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J	Samples
7802401SA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W	Samples
7802401SA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W	Samples
SN54LS299J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS299J	Samples
SN54LS299J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS299J	Samples
SN74LS299DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS299	Samples
SN74LS299DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS299	Samples
SN74LS299N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS299N	Samples
SN74LS299N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS299N	Samples
SNJ54LS299FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK	Samples
SNJ54LS299FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	78024012A SNJ54LS 299FK	Samples
SNJ54LS299J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J	Samples
SNJ54LS299J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802401RA SNJ54LS299J	Samples
SNJ54LS299W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS299W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7802401SA SNJ54LS299W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS299, SN74LS299 :

- Catalog : [SN74LS299](#)
- Military : [SN54LS299](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
78024012A	FK	LCCC	20	1	506.98	12.06	2030	NA
7802401SA	W	CFP	20	1	506.98	26.16	6220	NA
SN74LS299DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74LS299N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54LS299FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54LS299W	W	CFP	20	1	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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