Freescale Semiconductor
Product Brief

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MPC8360E PowerQUICC II™ Pro Processor Product Brief

This document provides an overview of the MPC8360E PowerQUICC II™ Pro processor features. The MPC8360E is a cost-effective, highly integrated communications processor that addresses the requirements of several networking applications, including next generation DSLAMs, network interface cards for 3G base stations (Node Bs), routers, media gateways, and high-end integrated access devices (IADs). The MPC8360E extends current PowerQUICC II offerings, adding higher CPU performance, additional functionality, faster interfaces and interworking between various communication protocols, while addressing the requirements related to time-to-market, price, power consumption, and board real estate.

Contents

1 Overview

The MPC8360E incorporates the e300 (MPC603e-based) core which includes 32 Kbytes of L1 instruction and data caches, along with a double-precision floating-point unit and on-chip memory management units. The MPC8360E also includes a 32-bit PCI bridge, four DMA channels, USB support, and dual 32-bit DDR memory controllers.

A new communications complex—the QUICC Engine™—forms the heart of the networking capability of

the MPC8360E. The QUICC Engine contains several peripheral controllers and integrates two 32-bit RISC controllers. Each RISC controller can control multiple peripherals and they work together to provide increased aggregated system bandwidth for higher throughput applications. Protocol support is provided by the main workhorses of the device—the unified communication controllers (UCCs) and multi-channel communication controller (MCC). A block diagram of the MPC8360E is shown in Figure 1.

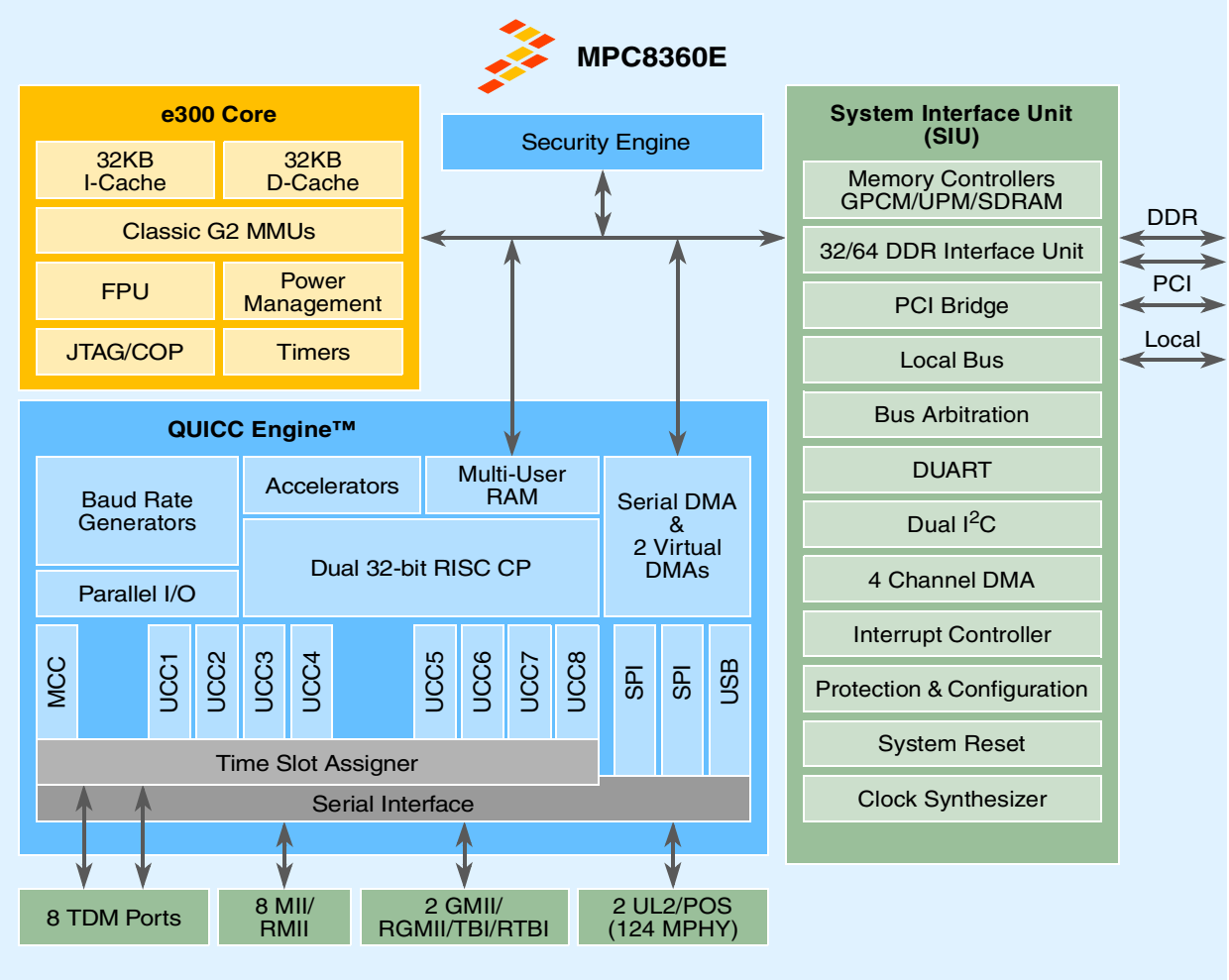

Figure 1. MPC8360E Block Diagram

Each of the eight UCCs can support a variety of communication protocols: 10/100/1000 Mbps Ethernet GMII/RGMII/TBI/RTBI, ATM/POS PHY support up to OC-12 speeds, serial ATM, multi-PHY ATM, HDLC, UART, and BISYNC. The MCC is capable of supporting up to 256 TDM channels in either transparent or HDLC modes, and multi-link/class PPP. Inverse multiplexing over ATM is supported and allows ATM traffic to be distributed across multiple E1/T1 circuits.

In addition, the QUICC Engine can also support two UTOPIA level 2 or two POS interfaces, each interface capable of supporting 124 multi-PHY, or up to two, 128 multi-PHY interfaces using extended address mode. The QUICC Engine also features an integrated 8-port, L2 Ethernet switch which can provide four priority levels on each port, VLAN functionality, IGMP snooping, network auto-negotiation functions, store-and-forward switching and packet-error filtering. Enhanced interworking features within the QUICC

Engine helps offload the main CPU. The QUICC Engine provides support for ATM (AAL2/AAL5) to Ethernet interworking, with L3 / L4 support and PPP interworking.

The MPC8360E's security engine allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. The security-processing accelerator provides hardware acceleration for the DES, 3DES, AES, SHA-1, MD-5, and ARC-4 algorithms. It includes a public key accelerator and an on-chip random number generator.

In summary, the MPC8360E provides users with a highly integrated, fully programmable communications processor. This helps ensure that a low-cost system solution can be quickly developed and will offer flexibility to accommodate new standards and evolving system requirements.

2 Application Examples

The internal features of the MPC8360E make it suitable for a wide variety of network communication applications as described in this section.

2.1 DSLAM Line Card

The diagram in Figure 2 illustrates how an intelligent DSLAM line-card can be readily implemented.

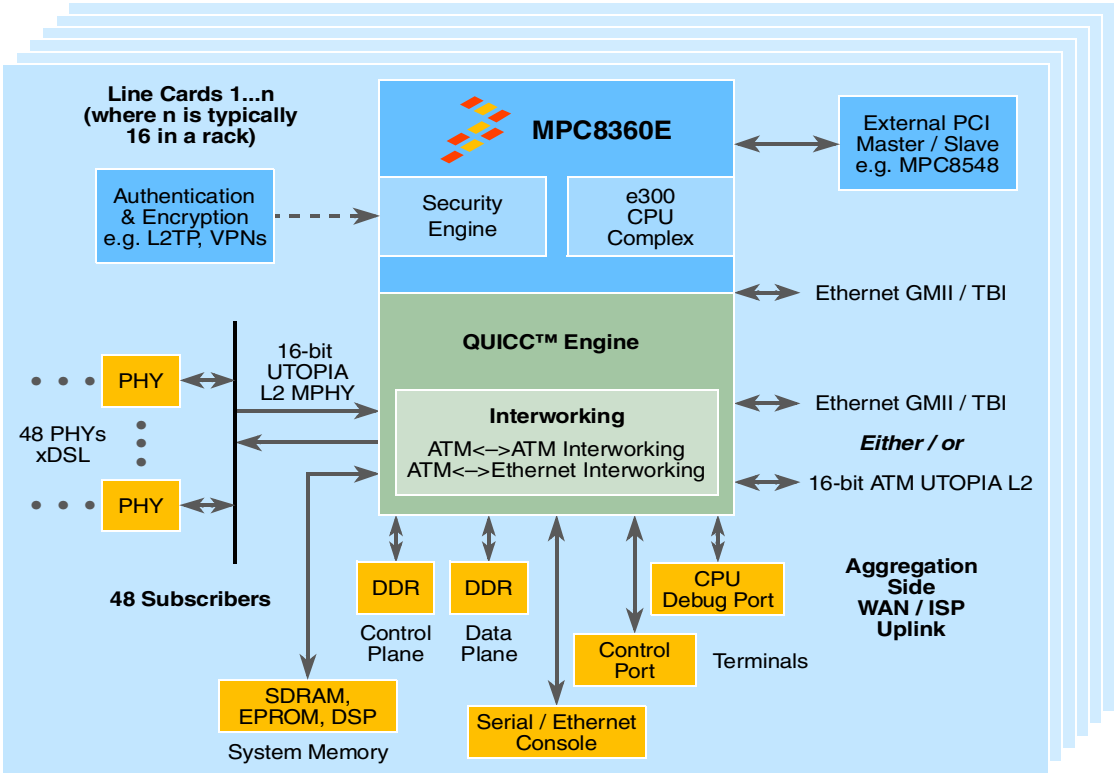

Figure 2. MPC8360E Line Card Implementation

In this example, the versatility of the UCCs handle the convergence of both packet and circuit switched networks because both ATM and gigabit Ethernet functions can be supported. As shown on the left-hand

side of the figure, subscribers are connected to the DSLAM line-card via the DSL PHYs and the integrated UTOPIA interface on the MPC8360E.

In this type of application, the MPC8360E makes use of its internal interworking features to offload the e300 CPU. Here, ATM-ATM interworking would be used to transfer data from the ATM based DSL subscriber inputs, through the cores within the QUICC Engine and out through the other ATM UTOPIA on the uplink port. In the event that the uplink switch fabric is Ethernet-based then ATM-Ethernet interworking would also be provided by the MPC8360E QUICC Engine. Subscribers could also connect directly to the DSLAM line-card using E1/T1 lines. In this scenario, the built-in IMA microcode could be used to bundle multiple E1/T1 lines together into a higher bit stream ATM connection for the uplink.

2.2 Node B Network Interface Card

Figure 3 illustrates how easily a typical Node B network interface card application can be created with the MPC8360E.

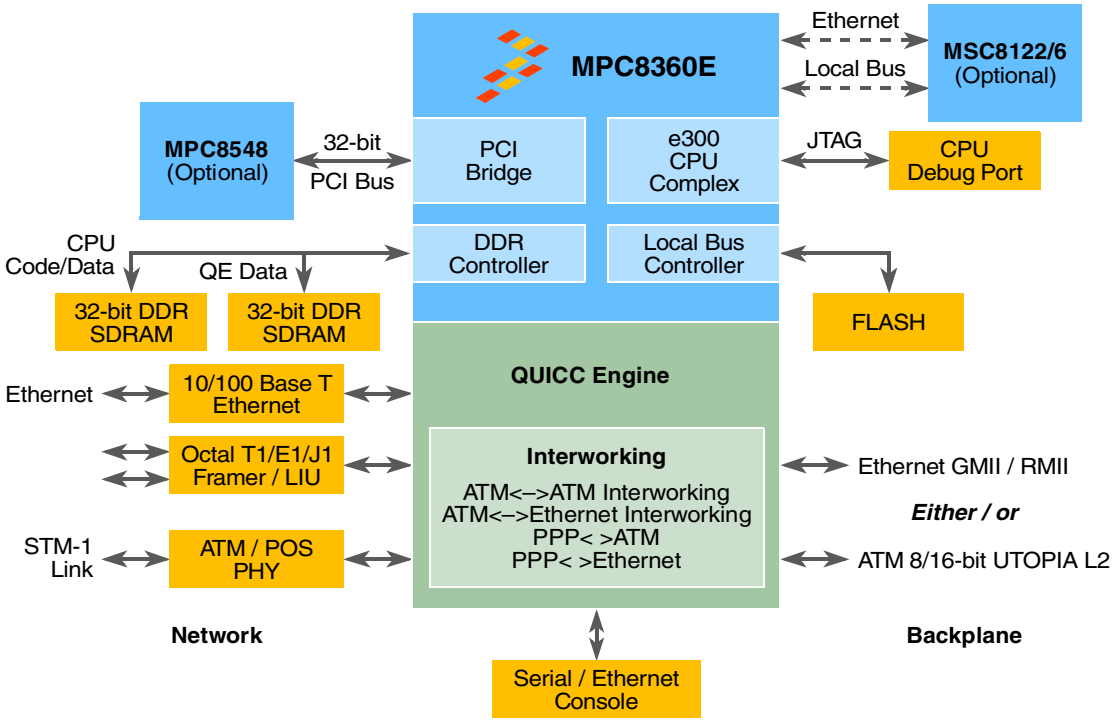

Figure 3. Node B Network Interface Card Using the MPC8360E

In this application, the MPC8360E provides all of the processing, protocol, and interworking functions required to implement the Node B network interface card. The QUICC Engine is used to carry voice, data, and video using ATM or IP over eight T1/E1 TDM links bundled with IMA or MLPPP-terminated protocols between the Node Bs and the RNC. In addition, one of the UCCs in the QUICC Engine could be used to support either a gigabit Ethernet (GMII) or ATM (UTOPIA 8/16-bit) interface to a backplane in the Node B. Another UCC could be used to implement an STM-1 / OC-3 (AAL5 and AAL2) link to the network (RNC). The unused UCCs can be configured as serial (UART) or Ethernet (MII) for debug and control.

2.3 SME Router

Figure 4 illustrates how a typical small/medium enterprise (SME) router application can be realized with the MPC8360E.

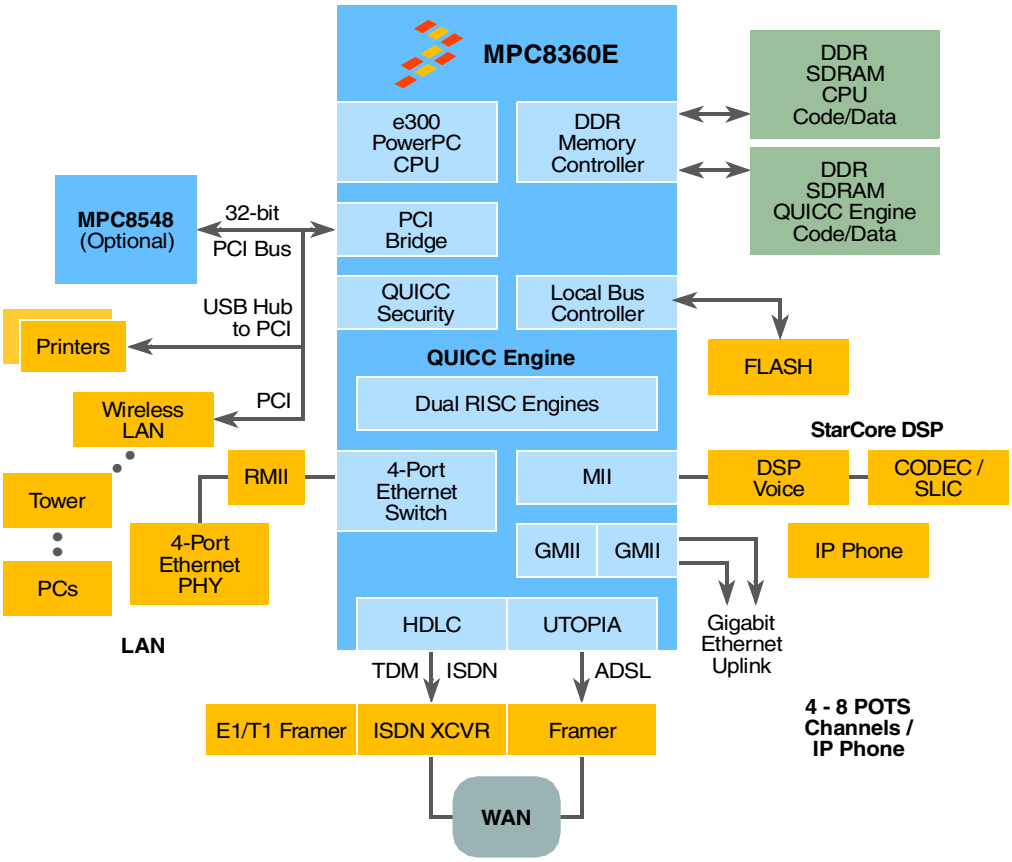

Figure 4. SME Router Using MPC8360E

In this application the MPC8360E provides all of the processing, protocol, and interworking functions required to implement the SME router. Specifically, the QUICC Engine is used to carry voice, data and video using IP over the LAN and WAN interfaces. On the LAN side, four UCCs are used to provide 10/100 fast Ethernet switching capabilities. Two gigabit Ethernet interfaces are used for uplink. One of the TDM interfaces is used to support HDLC, which provides a leased line E1/T1 connection or an ISDN connection. One UCC is used as an ATM interface supporting AAL5 cell Saring for dial-up ADSL connection, while the last UCC can be configured as serial (UART) or Ethernet (MII) for debug and control.

Alternatively, the remaining UCC of the MPC8360E could be used to support an Ethernet connection to a low cost digital signal processor (DSP) such as the family of DSPs based on the StarCore technology supporting 4 to 8 voice ports, which can be for plain old telephone system (POTS) telephones or for IP-based telephones using a combination of premium voice algorithms such as G729a/b, G723.1 or G71.1. For very high-density voice ports, the MSC8122 DSP can be used via an Ethernet interface.

Other interfaces connected to the PCI bus can include a four-port universal serial bus (USB) hub for connecting equipment such as printers, copiers, scanners, and system back up disks. In addition, a wireless

LAN interface can be connected to the PCI bus supporting 802.11-a/b/g/n connectivity within the office environment.

Finally, the security engine provides acceleration for encryption, authentication, and standards based tunnelling as required by IP-Sec.

3 Architecture Overview

The PowerQUICC II Pro MPC8360E is a high performance, highly integrated communication processor solution.

3.1 MPC8360E Features

- High-performance, low power, and cost-effective communications processor
- The MPC8360E QUICC Engine offers a future-proof solution for next generation designs by supporting programmable protocol termination, network interface termination, and interworking features to meet evolving protocol standards
- Single platform architecture supports the convergence of IP packet networks and ATM networks, including interworking between these networks
- Simplified network interface card design with a cost-effective single chip data plane/control plane solution for ATM or IP packet processing (or both). This reduces component count, board power consumption, and board real estate.
- Universal network interface card design for multiple applications, which lowers costs and reduces time-to-market
- Built-in proprietary hardware accelerators that accelerate data plane traffic, such as interworking, and control plane packet snooping, such as IGMP, VLAN tagging, DHCP, and so on
- DDR memory controller—one 64-bit or 2x32-bit interfaces that split data and control plane traffic at up to 333 MHz
- e300 PowerPC core (enhanced version of MPC603e core with 32 Kbytes of level 1 instruction and 32 Kbytes of level 1 data caches)
- 32-bit PCI interface
- 32-bit local bus interface
- USB
- Integrated 8-port L2 Ethernet switch
  - 8 connection ports of 10/100 Mbps MII/RMII & one CPU internal port
  - Each port supports four priority levels
  - Priority levels used with VLAN tags or IP TOS field to implement QoS
  - QoS types of traffic, such as voice, video, and data
- Security engine provides termination or encrypted plane traffic
- High degree of software compatibility with previous-generation PowerQUICC™ processor-based designs for backward compatibility and easier software migration

- Seamless connection to PowerQUICC III family devices for increased control (CPU) application processing requirements

3.1.1 Protocols

- ATM SAR up to 622 Mbps (OC-12) full duplex, with ATM traffic shaping (ATF TM4.1) for up to 64K ATM connections
- Support for ATM AAL1 structured and unstructured circuit emulation service (CES 2.0)
- Support for IMA and ATM transmission convergence sub-layer
- ATM OAM handling features compatible with ITU-T I.610
- PPP, multi-link (ML-PPP), multi-class (MC-PPP) and PPP multiplexing in accordance with the following RFCs: 1661, 1662, 1990, 2686 and 3153
- IP termination support for IPv4 and IPv6 packets including TOS, TTL, and header checksum processing
- L2 Ethernet switching using MAC address or IEEE 802.1P/Q VLAN tags
- Support for ATM (AAL2/AAL5) to Ethernet (IP) interworking
- Extensive support for ATM statistics and Ethernet RMON/MIB statistics.
- Support for 256 channels or HDLC/transparent or 128 channels of SS#7

3.1.2 Serial Interfaces

- Support for two UL2 / POS-PHY interfaces with 124 multi-PHY addresses each.
- Support for two 1000Mbps Ethernet interfaces using GMII or RGMII, TBI, RTBI.
- Support for up to eight 10/100Mbps Ethernet interfaces using MII or RMII
- Support for up to eight T1/E1/J1/E3 or DS-3 serial interfaces
- Support for dual UART, I^2C and SPI interfaces.

System scalability is also made available through the number of UCCs and MCCs. The initial implementation offers eight UCCs and one MCC; however as a result of the system-on-a-chip design methodology used for the QUICC Engine, these numbers can be scaled to support an optimized mix of communications channels. The flexible architecture of the QUICC Engine allows customers to customize their own application protocol and filtering requirements, allowing Freescale to add more RISC engines and/or UCCs on future family derivatives.

3.2 QUICC Engine

The QUICC Engine is a versatile communications complex that integrates several communications peripheral controllers. It provides on-chip system design for a variety of applications, particularly in communications and networking systems. The QUICC Engine has the following features:

- Two 32-bit RISC controllers for flexible support of the communications peripherals
- Serial DMA channel for receive and transmit on all serial channels

- Eight universal communication controllers (UCCs) supporting the following protocols and interfaces (not all of them simultaneously):
  - 10/100 Mbps Ethernet/IEEE 802.3
  - 1000 Mbps Ethernet/IEEE 802.3
  - IP support for IPv4 and IPv6 packets including TOS, TTL and header checksum processing
  - L2 Ethernet switching using MAC address or IEEE 802.1 P/Q VLAN tags
  - PPP, Multi-Link (ML-PPP), Multi-Class (MC-PPP), and PPP mux support
  - ATM protocol through UTOPIA interface
  - HDLC /transparent up to 70-Mbps full-duplex
  - HDLC BUS up to 10 Mbps
  - Asynchronous HDLC
  - UART
  - BISYNC up to 2 Mbps
  - QUICC Multichannel Controller (QMC) for 128 TDM channels
- One multichannel communication controller (MCC) supporting the following:
  - 256 HDLC or transparent channels
  - 128 SS#7 channels
- Two UTOPIA/POS interfaces supporting 124 multiphys each (optional 2×128 multiphys with extended address)
- Two serial peripheral interfaces (SPI). SPI2 is dedicated to Ethernet PHY management.
- 8 TDM interfaces
- Sixteen independent baud rate generators and 30 input clock pins for supplying clocks to UCC and MCC serial channels
- Four independent 16-bit timers that can be interconnected as two 32-bit timers
- Interworking functionality:
  - L2 10/100-Base T Ethernet switch
  - ATM-to-ATM switching (AAL0, 2, 5)
  - Ethernet-to-ATM switching with L3/L4 support

The QUICC Engine has a high level of compatibility with the peripherals in the MPC8260. It contains:

- Eight universal communication controllers (UCC)
- Two UTOPIA-packet over SONET (POS) controllers (UPC)
- Two serial peripheral controllers (SPI)
- One multi-channel controller (MCC)
- One universal serial bus (USB)

The UCCs are similar to the PowerQUICC II peripherals: SCC (BISYNC, UART, and HDLC bus), and FCC (fast Ethernet, HDLC, transparent, and ATM). In addition, 2×124 UTOPIA PHYs are supported in ATM mode. The QUICC Engine presents enhanced flexibility by allowing the user to configure the UCCs to support a Layer-2 Ethernet switch.

3.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, 802.11i, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs). The execution units are:

- Public key execution unit (PKEU)
- Data encryption standard execution unit (DEU)
- Advanced encryption standard unit (AESU)
- ARC four execution unit (AFEU)
- Message digest execution unit (MDEU)
- Random number generator (RNG)
- Four crypto-channels, each supporting multi-command descriptor chains

3.4 Dual DDR Memory Controllers

The MPC8360E DDR memory controllers include the following features:

- Programmable timing supporting DDR-1 SDRAM
- Configurable as two 32-bit buses or one 64-bit bus
- Support for up to 333 MHz data rate
- Support for up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
- Support for unbuffered and registered DIMMs
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 2.5-V SSTL2 compatible I/O

3.5 PCI Controller

The MPC8360E PCI controller includes the following features:

- PCI specification Revision 2.2 compatible
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Host and agent modes support.
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

3.6 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for general-purpose interrupt control. The PIC programming model is compatible with the MPC8260 interrupt controller, and it supports 8 external and 35 internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

3.7 DMA Controller, I^2C, DUART, Local Bus Controller, and Timers

The MPC8360E provides an integrated four-channel DMA controller, which:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local and remote masters).
- Supports misaligned transfers.

There are two I^2C controllers. These synchronous, multimaster buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The MPC8360E local bus controller (LBC) port allows connections with a wide variety of external memories, DSPs, and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user programmable machine (UPM) can be programmed to interface to synchronous devices or custom ASIC interfaces. The SDRAM controller provides access to standard SDRAM. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM, UPM, or SDRAM controller. All may exist in the same system.

The MPC8360E system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

4 Development Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Freescale Alliance Program, including third party protocol and signaling stack suppliers, real time operating systems support, and a variety of applications software support. All of this builds upon the existing industry standard PowerQUICC family support program.

To simplify and accelerate the development process, Freescale will provide a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator, and debugger for the e300 PowerPC core.

Freescale also provides an MDS board as a reference platform and programming development environment for the MPC8360E with a complete Linux board support package. The MDS board will support on-board DDR SDRAM memory, a PCI interface, and a debug port and can be configured with optional daughter cards supporting protocols such as OC-3 or OC-12 ATM, 8xT1/E1 and Ethernet (10/100/1000Base T).

The QUICC Engine will also be supported by a complete set of configurable device API drivers and initialization software. Figure 5 shows the wealth of communication protocols supported by the QUICC Engine with the e300 core.

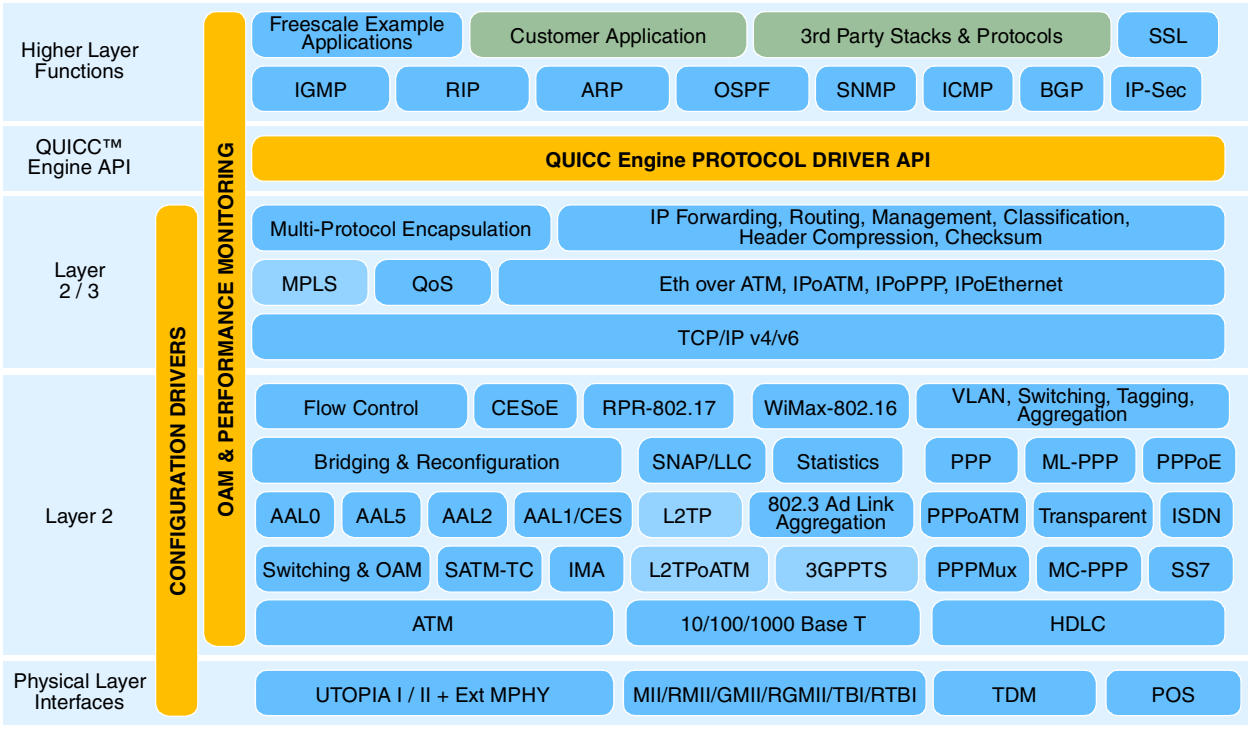

Figure 5. Software Protocol Support for the QUICC Engine

5 Document Revision History

Table 1 provides a revision history for this product brief.

Table 1. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release.

How to Reach Us:

Home Page:
www.freescale.com

email:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
(800) 521-6274
480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064, Japan
0120 191014
+81 2666 8080
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
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Literature Distribution Center
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@hibbertgroup.com

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