AMD8513/X

USB-to-10/100 Mbps Ethernet LAN Controller

Communications

Never stop thinking.

Edition 2005-12-05

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Revision History: 2005-12-05, Rev. 1.21

Previous Version:

Page/Date	Subjects (major changes since last revision)
2001-12	Rev. 0.1: Preliminary
2002-01	Rev. 1.0: Rearrange
2002-06	Rev. 1.1: 1.VAARef I/O is power pin, not input pin in P.7 2.GNDRef I/O is power pin, not input pin in P.7 3.Modify Pin Assignment Diagram P.5 4.Make small correction on P1, P2, P5, P10, P13, P17, P19, P35, P37, P38
2002-06	Rev 1.2: 1.Remove power consumption @ mode 1 in P.2 2.Change power consumption in P.33 3.Add layout guide in Appendix A
2005-09-13	Rev 1.21: when changed to the new Infineon format
2005-12-05	Minor change. Included Green package information

Trademarks

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1 Product Overview

1.1 Package Information

Product Name	Product Type	Package	Ordering Number
ADM8513	ADM8513-AD-T-1	P-LQFP-48-5	Q67801H 62A101 [1]
ADM8513X	ADM8513X-AD-T-1	PG-LQFP-48-5	Q67801H 98A101

1) “x” stands as key to Infineon packing variants, such as “Tape&reel, drypacked” as well as for the environmentally “green” package version.

1.2 Features

Main features:

- **Industrial Standard**
  - IEEE 802.3/802.3u 10Base-T/100Base-Tx compliant.
  - Supports IEEE 802.3x flow control
  - Supports Auto-Negotiation for 10BASE-T and 100BASE-TX
  - USB specification 1.0 and 1.1 compliant
- **USB Interface**
  - USB specification 1.0 and 1.1 compliant
  - Full-Speed USB Device
  - Supports 1 USB configuration and 1 interface
  - Supports all USB standard commands
  - Supports two vendor specific commands
  - Supports USB Suspend/Resume detection logic
  - Supports 4 endpoints: 1 control endpoint with maximum 8-byte packet, 1 bulk IN endpoint with maximum 64-byte packet, 1 bulk OUT endpoint with maximum 64-byte packet and 1 interrupt IN endpoint with maximum 8-byte packet
- **MAC/PHY**
  - Integrates the PHY by using address 1
  - Supports configurable threshold for PAUSE frame.
  - Supports Auto-Negotiation
  - Provides transmit wave-shaper, receive filter, and adapter equalizer.
  - Provides MLT-3 transceiver with DC restoration for Base-Line wander.
  - Supports external transmit/receive transformer with turn ration 1:1.
- **EEPROM Interface**
  - Provides serial interface to access 93C46 EEPROM
  - Automatically load device ID, vendor ID from EEPROM after power-on reset
- **FIFO**
  - Synchronous SRAM.
  - Internal 2K-byte two port asynchronous SRAM.
- **LED Interface**
  - 2 LED operation modes
  - LED0: speed indication for 10Mbps or 100Mbps.
  - LED1: link indication.
  - LED2: full duplex indication.
- **Support Power Save Function @ USB suspend mode**

  - Mode 0: Resume by remote wakeup or host when OS goes into standby
  - Mode 1: Resume by host when OS goes into standby.
- **Miscellaneous**
  - Supports 6 GPIO pins
  - Provides 48-pin LQFP package
  - 3.3 V power supply with 5 V/3.3 V I/O tolerance
- **Support Driver**
  - Win98/ME/2000/XP
  - Linux driver, WinCE 3.0&4.0 driver
  - Manufacturing test utilities:
  - EEPROM Burn-in program
  - MFG testing program

2 Interface Description

2.1 Pin Assignment Diagram

Pin Diagram ADM8513/X.

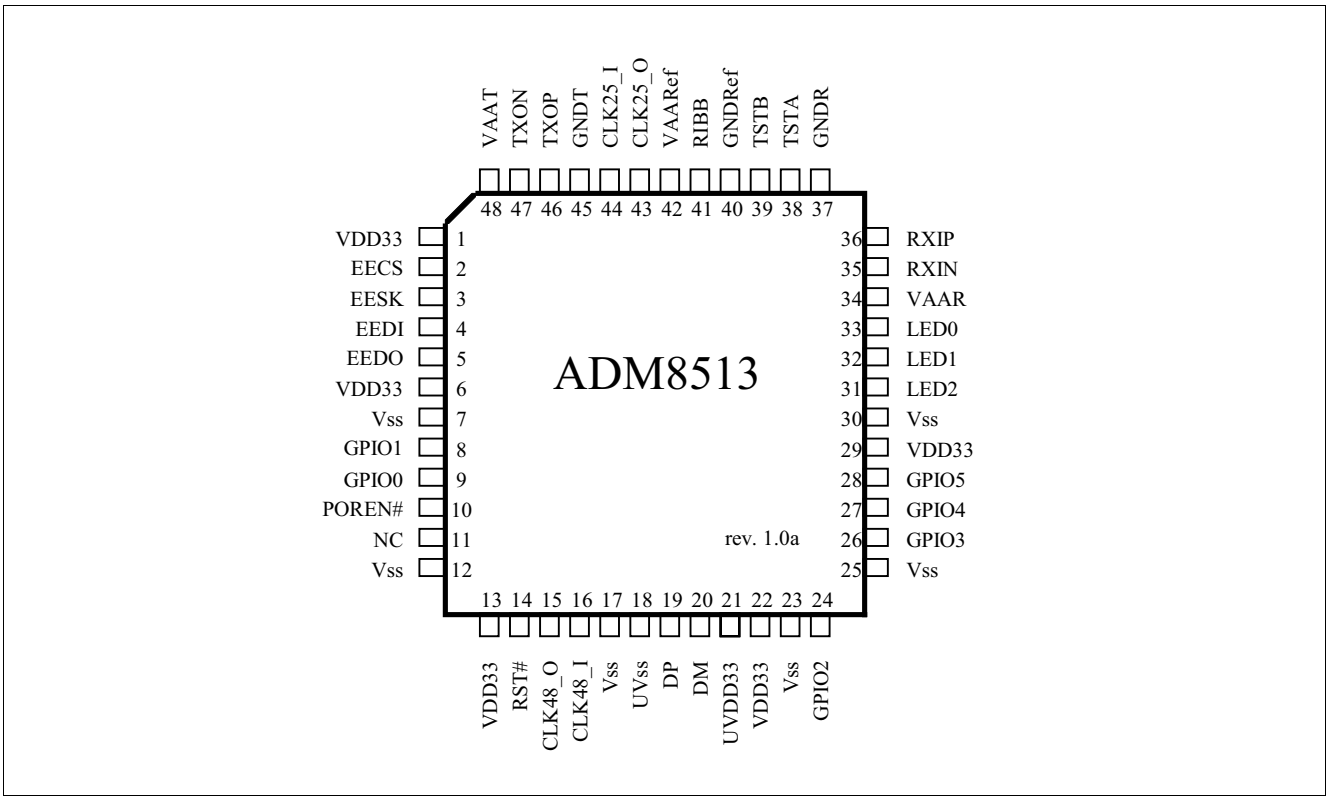


Figure 1 Pin Diagram

2.2 Pin Description by Function

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)

Table 1 Abbreviations for Pin Type (cont'd)

Abbreviations	Description
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 kΩ
PD1	Pull down, 10 kΩ
PD2	Pull down, 20 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.2.1 Host Interface

Table 3 Host Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
16	CLK48_I	I		**Input Clock** 48 MHz clock input from crystal or oscillator.
15	CLK48_O	O		**Output for Crystal**
14	RST#	I		**External Hardware Reset Input** Schmitt-trigger, internal pull high.
20	DM	I/O		**USB Data Minus pin**
19	DP	I/O		**USB Data Plus Pin**

2.2.2 Physical Interface

Table 4 Physical Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
86, 35	RXIP, RXIN	I		**RX Input**
46, 47	TXOP, TXON	O		**TX Output**
44	CLK25_I	I		**Crystal Input** 25MHz
43	CLK25_O	O		**Crystal Output** 25MHz
41	RIBB	I		**Reference Bias Resistor, tied to external 10K(1%) resistor to ground**
38, 39	TSTA, TSTB	O		**Test Output Pin**

2.2.3 LED Interface

Table 5 LED Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
33	LED0	O		**LED display for 100M b/s or 10M b/s speed.** Active low indicates 100Base-TX, active high indicates 10 BaseT.
32	LED1	O		**LED display for link and activity status.** Active low when link is established.
31	LED2	O		**LED display for Full Duplex or Collision status.** Active low indicates full duplex, high indicates collision in half duplex.

Note: The LED interface is EEPROM-programmable, 2 bit EEPROM control bit, Address 0B[7:6] at EEPROM, is used to select LED mode, the default setting are:

1. *LED0: 100Mbps(on, drive '0') or 10Mbps(off, drive '1')*
2. *LED1: link (keeps on when link ok) or activity (blinks with 10Hz when Pegasus II is receiving or transmitting but not colliding*
3. *LED2: full duplex (keeps on when in full duplex mode) or collision (blinks with 20Hz when colliding)*
4. *All LED pins will be tri-state when using external PHY (offset 81h with bit[4:2] = 001_B)*

Mapping between LED action and EEPROM 0B[7:6] setting

Table 6 Mapping between LED action and EEPROM 0B[7:6] setting

EEPROM 0B[7:6]	LED	Action
0,0	LED0	10 / 100 (OFF/ON)
	LED1	LINK / ACTIVITY (ON/FLASH)
	LED2	FULL DUP / COL (ON/FLASH)
0,1	LED0	ACTIVITY when LINK (FLASH)
	LED1	LINK 10(ON)
	LED2	LINK 100(ON)

2.2.4 EEPROM Interface

Table 7 EEPROM Interface

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
2	EECS	O		**EEPROM Chip Select** This pin enables the EEPROM during loading of the Ethernet configuration data. CMOS I/O with 5 V tolerant, 2mA
4	EEDI	O		**EEPROM Data In** The MAC will use this pin to serially write opcodes, addresses and data into the serial EEPROM. CMOS I/O with 5 V tolerant, 2mA
5	EEDO	I		**EEPROM Data Out, internal pull low** The MAC will read the contents of the EEPROM serially through this pin. Input, pull down, 5 V tolerant
3	EESK	O		**EEPROM Clock** After reset, the MAC if configured, will read the contents of the EEPROM using EESK, EEDO, and EEDI. This pin provides the clock for the EEPROM. CMOS I/O with 5 V tolerant, 2mA

2.2.5 Miscellaneous

Table 8 Miscellaneous

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
9	GPIO5	I/O		**General Purpose Input/Output Pins** These pins are used as general purpose Input/Output pins and offset 0A[1] = 0 in EEPROM. Default is internal pull-low
8	GPIO4			
24	GPIO3			
26	GPIO2			
27	GPIO1			
28	GPIO0			
10	POREN#	I		**Test Pins**
11	NC	X		**Test Pins**

2.2.6 POWER USB

Table 9 Power USB

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
21	UVDD 33	PWR		**3.3V power supply for USB transceiver**
18	UVSS	PWR		**Ground for USB transceiver**

2.2.7 POWER

Table 10 Power

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
1, 6, 13, 22, 29	VDD 33	PWR		**3.3V Power Supply.**
7, 12, 23, 17, 25, 30	VSS	PWR		**Ground**
42	VAARef	PWR		**+3.3V Power Supply for PHY.**
40	GNDRed	PWR		**+3.3V Power Ground for PHY**
48	VAAT	PWR		**+3.3V for Transmitter**
45	GNDT	PWR		**GND for Transmitter**
34	VAAR	PWR		**+3.3V for Receiver**
37	GNDR	PWR		**GND for Receiver**

2.3 Block Diagram

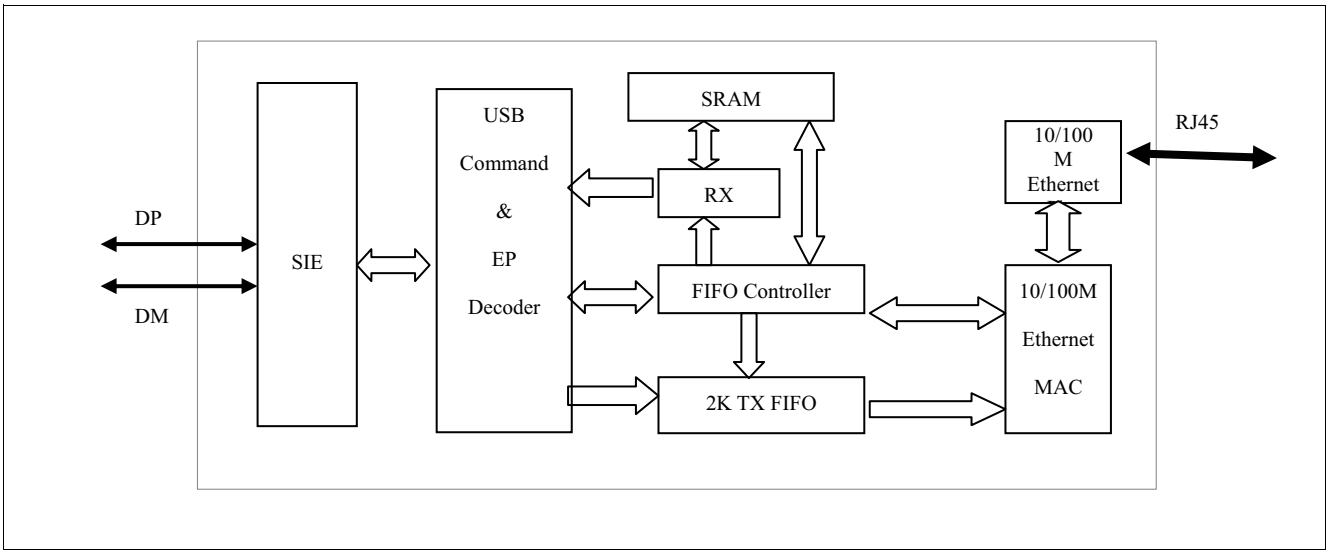


Figure 2 Block Diagram

3 Function Description

3.1 USB Interface

USB is a likely solution any time you want to use a computer to communication with devices outside the computer. The interface is suitable for one-of-kind and small-scale designs as well as mass-produced, standard peripheral. The benefits to USB are easy to use, fast and reliable data transfers, flexibility, low cost and power conservation.

3.1.1 SIE

SIE (Serial Interface Engine) is to control USB communications and check USB protocol, then transfer protocol to EP decoder. The SIE and USB transceivers, which provide the hardware interface to the USB cable, together comprise the USB engine.

3.1.2 USB Command & EP Decoder

The detail description is in “USB Command”.

3.2 FIFO Controller

FIFO Controller in receive path is in charge of:

- Stores received Ethernet packets to SRAM and multiple packets can be stored to SRAM. If more than maximum packet counts are received or total packet size is more than the size of SRAM, the subsequent coming Ethernet packet will be discarded.
- FIFO controller will load data from SRAM to internal RX FIFO then inform EP Decoder that 64-byte data or a packet is ready in RX FIFO. Before FIFO controller informs about this, any USB access to bulk IN endpoint will return NAK. This is to maintain the data transfer on the USB bus via bulk IN transfer which is continuous, thus a 64-byte internal RX FIFO is needed.
- If an Ethernet packet is being received and loading into SRAM while FIFO Controller is moving data from SRAM to internal RX FIFO, writing the Ethernet packet to SRAM will get the higher priority.

3.3 TX FIFO and RX FIFO

RX FIFO is a one-port 64-byte FIFO and TX FIFO is a two-port 2K-byte FIFO.

3.4 10/100M Ethernet PHY

The Ethernet PHY is compliant to IEEE 802.3u 100BASE-TX and IEEE802.3 10BASE-T. It provides the whole physical layer functions for both 10M and 100M Ethernet speed.

4 USB Device Endpoint Operation

4.1 Endpoint 0

Endpoint 0 is in charge of response to standard USB commands and vendor specific commands. Internal register settings are also via this endpoint. The response to each command is described in section 6.

4.2 Endpoint 1 Bulk IN

Endpoint 1 is in charge of sending the received Ethernet packet to USB host. An Ethernet packet will be split to multiple 64 bytes USB packets on USB. The end of the Ethernet packet is indicated by less then 64-byte or 0 length data transfer in this pipe. The Ethernet received status is optionally reported at the end of the packet.

While accessing to this endpoint, if RXFIFO is either full or any packet is inside, the data in RXFIFO is returned in USB data stage. If ACK is received from USB host, data in RXFIFO is flushed. If no response or NAK is received from USB host, the content in RXFIFO will be re-transmitted. If RXFIFO isn't ready for transmission, NAK is returned to USB host.

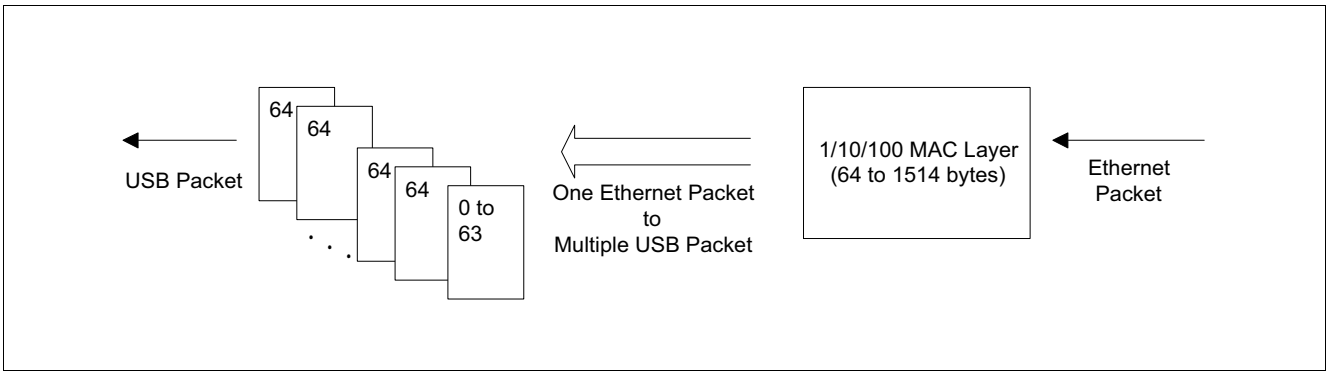


Figure 3 Packet Form when Receive

The Received Status is Reported as Follows:

Table 11 USB Received Status

Offset	Bit	Field	Description
Offset0	7-0	rx_bytecnt_lo	The received byte count[7:0].
Offset1	3-0	rx_bytecnt_hi	The received byte count[11:8].
	7-4	reserved	
Offset2	0	multicast_frame	Indicates received a multicast frame.
	1	long_pkt	Indicates received packet length > 1518 bytes.
	2	runt_pkt	Indicates received packet length < 64 bytes.
	3	crc_err	Indicates CRC check error.
	4	dribble_bit	Indicates packet length is not integer multiple of 8-bit.
	7-5	reserved	
Offset3	7-0	reserved	

4.2.1 Endpoint 2 Bulk OUT

Endpoint 2 is in charge of sending the USB packet to Ethernet. An Ethernet packet is concatenated by multiple 64 bytes USB packets on USB. The first two bytes in every first concatenated USB packet indicate the length of the Ethernet packet. The end of the Ethernet packet is indicated by less then 64-byte or 0 length data transfer in this pipe. The Ethernet transmit status is reported in transmit status register.

When accessing to this endpoint, data in USB data stage is transferred to TXFIFO, if TXFIFO is free and ACK is returned. If TXFIFO isn’t free, NAK is returned.

Table 12 USB Packet Format

Field	1st Byte in 1st USB Packet	2nd Byte in 1st USB Packet	The Following Packets
Content	len[7:0]: Low byte Ethernet packet length	{reserved[4:0], len[10:8]}	Ethernet packet

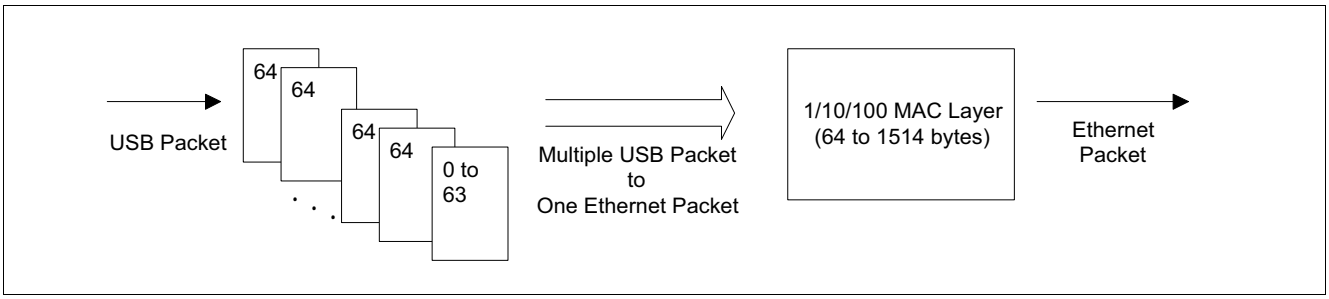


Figure 4 Packet Form when Transmit

4.2.2 Endpoint 3 Interrupt IN

Endpoint 3 is in charge of returning the current Ethernet transfer status every polling interval. When accessing to this endpoint, 8 bytes data is returned to USB host. The 8-byte packet contains

Table 13 Interrupt Packet Form

Offset0	Offset1	Offset2	Offset3	Offset4
tx_status(Reg2B$_H$)	tx_status(Reg2C$_H$)	rx_status(Reg2D$_H$)	rx_lostpkt(Reg2E$_H$)	rx_lostpkt(Reg2F$_H$)

Table 14 Interrupt Packet Form

Offset5	Offset6(1B)	Offset7(1B)
wakeup_status(Reg7A$_H$)	Packet number in RX FIFO (Reg82$_H$)	7'b00, length error

5 USB Commands

5.1 USB Command

5.1.1 Get Register (Vendor Specific) Single/Burst Read

Table 15 Setup Stage

bmReq	bReq	wValue(2B)	wIndexLow(1B)	wIndexHigh(1B)	wLength L(1B)	wLength H(1B)
C0	F0	0	RegIndex[7:0]	00	Length Low	Length High

Table 16 Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)
{RegIndex}	{RegIndex+1)	{RegIndex+2)

The returned total number of registers depends on the length field.

5.1.2 Set Register (Vendor Specific) Burst Write

Table 17 Setup Stage

bmReq	bReq	wValue(2B)	wIndexLow(1B)	wIndexHigh(1B)	wLength L(1B)	wLength H(1B)
40	F1	0	RegIndex[7:0]	00	Length Low	Length High

Table 18 Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)
{RegIndex}	{RegIndex+1}	{RegIndex+2}	{RegIndex+3}

Ex. Write 44 to RegIndex = 05_H, the transfer will be

Table 19 Setup Stage

bmReq	bReq	wValue L(1B)	wValue H(1B)	wIndexLow (1B)	wIndexHigh (1B)	wLength L(1B)	wLength H(1B)
40	F1	44	00	05	00	01	00

If wLength > 1, more than 1 register is accessed (burst write) and mask is not supported => DataStage for 8-byte OUT transfer appears

Ex. Burst write 20 registers from RegIndex = 07_H and data from 01_D to 20_D

- Setup Stage

Table 20 Setup Stage

bmReq	bReq	wValue(2B)	wIndexLow(1B)	wIndexHigh(1B)	wLength L(1B)	wLength H(1B)
40	F1	0000	07	00	14	00

- Data Stage

Table 21 1st OUT Transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
01	02	03	04	05	06	07	08

Table 22 2nd OUT Transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
09	0A	0B	0C	0D	0E	0F	10

Table 23 3rd OUT Transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)
11	12	13

5.1.3 Get Status (Device)

Table 24 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
80	0	0	0	2	0

Table 25 Data Stage

D[15:2]	D[1]: Remote Wakeup	D[0]:Self Powered
0	Register of remote_wakeup	1

5.1.4 Get Status (Interface)

Table 26 Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
81	0	0	0	2	0

Table 27 Data Stage

D[15:0]
0

5.1.5 Get Status (EP0)

Table 28 Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	wLength H(1B)
82	0	0	80 or 00	00	2	0

Table 29 Data Stage

D[15:1]	D[0]: Halt
0	Register of ep0_halt

5.1.6 Get Status (EP1) Bulk In

Table 30 Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	wLength H(1B)
82	0	0	81	00	2	0

Table 31 Data Stage

D[15:1]	D[0]: Halt
0	Register of ep1_halt

5.1.7 Get Status (EP2) Bulk OUT

Table 32 Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	WLength H(1B)
82	0	0	02	00	2	0

Table 33 Data Stage

D[15:1]	D[0]: Halt
0	register of ep2_halt

5.1.8 Get Status (EP3) Interrupt IN

Table 34 Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	wLength H(1B)
82	0	0	83	00	2	0

Table 35 Data Stage

D[15:1]	D[0]: Halt
0	register of ep3_halt

5.1.9 Get Descriptor (Device) Total 18-byte

Table 36 Setup Stage

bmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
80	6	01	00	0	Length low	Length high

Table 37 Data Stage: wLength Field Specifies the Total byte Count to Return 1

Offset 0	Offset 1 (type)	Offset 2 (USB release no. L)	Offset 3 (USB release no. H)	Offset 4 (Class code)	Offset 5 (Sub Class Code)	Offset 6 (Protocol)	Offset 7 (EP0 MaxPktSize)
$12(1_B)$	$01(1_B)$	$10(1_B)$	$01(1_B)$	$FF(1_B)$	$00(1_B)$	$ff(1_B)$	$8(1_B)$

Table 38 Data Stage: wLength Field Specifies the Total byte Count to Return 2

Offset 8 (vendor ID) Low	Offset 9(vendor ID) High	Offset 10 (productID) Low	Offset 11 (productID) High	Offset 12 (releaseID Low)
(1_B)	(1_B)	(1_B)	(1_B)	$01(1_B)$

Table 39 Data Stage: wLength Field Specifies the Total byte Count to Return 3

Offset 13 (releaseID High)	Offset 14 (manufacture)	Offset 15 (Product)	Offset 16 (serial no.)	Offset 17 (no. of config)
$01(1_B)$	$01(1_B)$	$02(1_B)$	$03(1_B)$	$01(1_B)$

5.1.10 Get Descriptor (Configuration) Total 39-byte

Table 40 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
80	6	02	00	0	Length low	Length high

- Data Stage

Table 41 Configuration Descriptor 1

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (TotalLength) Low	Offset 3 (TotalLength) High	Offset 4 (NumInterface)
$09(1_B)$	$02(1_B)$	$27(1_B)$	$00(1_B)$	$01(1_B)$

Table 42 Configuration Descriptor 2

Offset 5 (ConfgValue)	Offset 6 (StringIndex)	Offset 7 (Attribute)	Offset 8(MaxPower)
$00(1_B)$	$00(1_B)$	$E0(1_B)$	$max\_pwr(1_B)$

Table 43 Interface 0 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (Interface Num)	Offset 3 (AltInterface)	Offset 4 (NumEP)	Offset 5 (IntfClass)	Offset 6 (IntfSubClass)	Offset 7 (IntfProtocol)	Offset 8 (StringIndex)
$09(1_B)$	$04(1_B)$	$00(1_B)$	$00(1_B)$	$03(1_B)$	$FF(1_B)$	$E0(1_B)$	$FF(1_B)$	$00(1_B)$

Table 44 EP1 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (EPAddr)	Offset 3 (Attribute)	Offset 4 (MaxPktSize) Low	Offset 5 (MaxPktSize) High	Offset 6 (Interval)
$07(1_B)$	$05(1_B)$	$81(1_B)$	$02(1_B)$ bulk	$64(1_B)$	$00(1_B)$	$00(1_B)$

Table 45 EP2 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (EPAddr)	Offset 3 (Attribute)	Offset 4 (MaxPktSize) Low	Offset 4 (MaxPktSize) High	Offset 6 (Interval)
$07(1_B)$	$05(1_B)$	$02(1_B)$	$02(1_B)$ bulk	$64(1_B)$	$00(1_B)$	$00(1_B)$

Table 46 EP3 Descriptor

Offset 0 (Length)	Offset 1 (DscrType)	Offset 2 (EPAddr)	Offset 3 (Attribute)	Offset 4 (MaxPktSize) Low	Offset 5 (MaxPktSize) High	Offset 6 (Interval)
$07(1_B)$	$05(1_B)$	$83(1_B)$	$03(1_B)$ interrupt	$08(1_B)$	$00(1_B)$	ep3_interval(1_B)

5.1.11 Get Descriptor (String) Index 0, LanguageID Code

Table 47 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength Low(1B)	wLength High(1B)
80	06	00	03	0000	Length Low	Length High

Table 48 Data Stage

Offset0 (Length)	Offset1 (DscrType)	Offset2 (LanguageID) L	Offset3 (LanguageID) H
$04(1_B)$	$03(1_B)$	$09(1_B)$	$04(1_B)$

5.1.12 Get Descriptor (String) Index 1, Manufacture

Table 49 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex (2B)	wLength Low(1B)	wLength High(1B)
80	06	01	03	0904	Length Low	Length High

Table 50 Data Stage

Offset0 (Length)	Offset1 (DscrType)	
length(1B)	03(1B)	String

5.1.13 Get Descriptor (String) Index 2, Product

Table 51 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex (2B)	wLength Low(1B)	wLength High(1B)
80	06	02	03	0904	Length Low	Length High

Table 52 Data Stage

Offset 0 (Length)	Offset 1 (DscrType)	
length(1_B)	03(1_B)	String

5.1.14 Get Descriptor (String) Index 3, Serial No.

Table 53 Setup Stage

BmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex (2B)	wLength Low(1B)	wLength High(1B)
80	06	03	03	0904	Length Low	Length High

Table 54 Data Stage

Offset 0 (Length)	Offset 1 (DscrType)	
Length(1_B)	03(1_B)	String

5.1.15 Get Configuration

Table 55 Setup Stage

BmReq	bReq	wValue(2B)	wIndex(2B)	wLength Low(1B)	wLength High(1B)
80	08	0	0	1	0

Table 56 Data Stage

Offset 0 (ConfgValue)(1B)

5.1.16 Get Interface

Table 57 Setup Stage

BmReq	bReq	wValue(2B)	wIndex(2B)	wLength Low(1B)	wLength High(1B)
81	10	0	0	1	0

Table 58 Data Stage

Offset0 (AltIntf) (1B)
00

5.1.17 Clear Feature (Device) Remote Wakeup

Table 59 Setup Stage

BmReq	bReq	wValue L(1B)	WValue H(1B)	wIndex(2B)	wLength(2B)
00	01	01	00	0	0

5.1.18 Set Feature (Device) Remote Wakeup

Table 60 Setup Stage

BmReq	bReq	wValue L(1B)	WValue H(1B)	wIndex(2B)	wLength(2B)
00	03	01	00	0	0

5.1.19 Clear Feature (EP 0, 1, 2, 3) Halt

Table 61 Setup Stage

BmReq	bReq	wValue(2B)	WIndex L(1B)	wIndex L(2B)	WLength(2B)
02	03	0000	EP no	00	0

5.1.20 Set Feature (EP 0, 1, 2, 3) Halt

Table 62 Setup Stage

BmReq	bReq	wValue(2B)	WIndex H(1B)	wIndex H(2B)	WLength(2B)
02	03	0000	EP no	00	0

6 Registers Description

6.1 System Registers

Table 63 Registers Address Space

Module	Base Address	End Address	Note
System Registers	0000 0000_H	0000 0081_H	

Table 64 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
Res30_Res155	Reserved 30~Reserved 155	82~FF_H	34
EC0	Ethernet Control 0	00_H	30
EC1	Ethernet Control 1	01_H	31
EC2	Ethernet Control 2	02_H	32
Res0	Reserved 0	03_H	33
Res1	Reserved 1	04_H	33
Res2	Reserved 2	05_H	33
Res3	Reserved 3	06_H	33
Res4	Reserved 4	07_H	33
MA0	Multicast Address 0	08_H	34
MA1	Multicast Address 1	09_H	34
MA2	Multicast Address 2	$0A_H$	35
MA3	Multicast Address 3	$0B_H$	35
MA4	Multicast Address 4	$0C_H$	36
MA5	Multicast Address 5	$0D_H$	36
MA6	Multicast Address 6	$0E_H$	37
MA7	Multicast Address 7	$0F_H$	37
EID0	Ethernet ID 0	10_H	38
EID1	Ethernet ID 1	11_H	38
EID2	Ethernet ID 2	12_H	39
EID3	Ethernet ID 3	13_H	39
EID4	Ethernet ID 4	14_H	40
EID5	Ethernet ID 5	15_H	40
Res5	Reserved 5	16_H	33
Res6	Reserved 6	17_H	33
PT	Pause Timer	18_H	41
RPNBFC	Receive Packet Number Based Flow Control	$1A_H$	41
ORFBFC	Occupied Receive FIFO Based Flow Control	$1B_H$	42
EP1C	EP1 Control	$1C_H$	42
Res7	Reserved 7	$1C_H$	33

Table 64 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
Res8	Reserved 8	$1D_H$	33
Res9	Reserved 9	$1E_H$	33
Res10	Reserved 10	$1F_H$	33
EEPROMO	EEPROM Offset	20_H	43
EEPROMDL	EEPROM Data Low	21_H	43
EEPROMDH	EEPROM Data High	22_H	43
EEPROMAC	EEPROM Access Control	23_H	45
Res11	Reserved 11	24_H	33
PHYA	PHY Address	25_H	45
PHYDL	PHY Data Low	26_H	46
PHYDH	PHY Data High	27_H	46
PHYAC	PHY Access Control	28_H	47
Res12	Reserved 12	29_H	33
USBBS	USB Bus Status	$2A_H$	47
TS1	Transmit Status 1	$2B_H$	47
TS2	Transmit Status 2	$2C_H$	49
RS	Receive Status	$2D_H$	49
RLPCH	Receive Lost Packet Count High	$2E_H$	50
RLPCL	Receive Lost Packet Count Low	$2F_H$	50
WUF0M_0	Wakeup Frame 0 Mask	30_H	50
WUF0M_1	Wakeup Frame 0 Mask 1	31_H	51
WUF0M_2	Wakeup Frame 0 Mask 2	32_H	51
WUF0M_3	Wakeup Frame 0 Mask 3	33_H	51
WUF0M_4	Wakeup Frame 0 Mask 4	34_H	51
WUF0M_5	Wakeup Frame 0 Mask 5	35_H	51
WUF0M_6	Wakeup Frame 0 Mask 6	36_H	51
WUF0M_7	Wakeup Frame 0 Mask 7	37_H	51
WUF0M_8	Wakeup Frame 0 Mask 8	38_H	51
WUF0M_9	Wakeup Frame 0 Mask 9	39_H	51
WUF0M_10	Wakeup Frame 0 Mask 10	$3A_H$	51
WUF0M_11	Wakeup Frame 0 Mask 11	$3B_H$	51
WUF0M_12	Wakeup Frame 0 Mask 12	$3C_H$	51
WUF0M_13	Wakeup Frame 0 Mask 13	$3D_H$	51
WUF0M_14	Wakeup Frame 0 Mask 14	$3E_H$	51
WUF0M_15	Wakeup Frame 0 Mask 15	$3F_H$	51
WUF0O_0	Wakeup Frame 0 Offset	40_H	51
WUF0CRCL	Wakeup Frame 0 CRC Low	41_H	52
WUF0CRCH	Wakeup Frame 0 CRC High	42_H	52
Res13	Reserved 13	43_H	33
Res14	Reserved 14	44_H	33
Res15	Reserved 15	45_H	33

Table 64 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
Res16	Reserved 16	46_H	33
Res17	Reserved 17	47_H	33
WUF1M_0	Wakeup Frame 1 Mask	48_H	53
WUF1M_1	Wakeup Frame 1 Mask 1	49_H	53
WUF1M_2	Wakeup Frame 1 Mask 2	$4A_H$	53
WUF1M_3	Wakeup Frame 1 Mask 3	$4B_H$	53
WUF1M_4	Wakeup Frame 1 Mask 4	$4C_H$	53
WUF1M_5	Wakeup Frame 1 Mask 5	$4D_H$	53
WUF1M_6	Wakeup Frame 1 Mask 6	$4E_H$	53
WUF1M_7	Wakeup Frame 1 Mask 7	$4F_H$	53
WUF1M_8	Wakeup Frame 1 Mask 8	50_H	53
WUF1M_9	Wakeup Frame 1 Mask 9	51_H	53
WUF1M_10	Wakeup Frame 1 Mask 10	52_H	53
WUF1M_12	Wakeup Frame 1 Mask 12	54_H	53
WUF1M_13	Wakeup Frame 1 Mask 13	55_H	53
WUF1M_11	Wakeup Frame 1 Mask 11	56_H	53
WUF1M_14	Wakeup Frame 1 Mask 14	56_H	53
WUF1M_15	Wakeup Frame 1 Mask 15	57_H	53
WUF1O	Wakeup Frame 1 Offset	58_H	53
WUF1CRCL	Wakeup Frame 1 CRC Low	59_H	55
WUF1CRCH	Wakeup Frame 1 CRC High	$5A_H$	55
Res18	Reserved 18	$5B_H$	33
Res19	Reserved 19	$5C_H$	33
Res20	Reserved 20	$5D_H$	33
Res21	Reserved 21	$5E_H$	33
Res22	Reserved 22	$5F_H$	33
WUF2M	Wakeup Frame 2 Mask	60_H	56
WUF2M_1	Wakeup Frame 2 Mask 1	61_H	56
WUF2M_2	Wakeup Frame 2 Mask 2	62_H	56
WUF2M_3	Wakeup Frame 2 Mask 3	63_H	56
WUF2M_4	Wakeup Frame 2 Mask 4	64_H	56
WUF2M_5	Wakeup Frame 2 Mask 5	65_H	56
WUF2M_6	Wakeup Frame 2 Mask 6	66_H	56
WUF2M_7	Wakeup Frame 2 Mask 7	67_H	56
WUF2M_8	Wakeup Frame 2 Mask 8	68_H	56
WUF2M_9	Wakeup Frame 2 Mask 9	69_H	56
WUF2M_10	Wakeup Frame 2 Mask 10	$6A_H$	56
WUF2M_11	Wakeup Frame 2 Mask 11	$6B_H$	56
WUF2M_12	Wakeup Frame 2 Mask 12	$6C_H$	56
WUF2M_13	Wakeup Frame 2 Mask 13	$6D_H$	56
WUF2M_14	Wakeup Frame 2 Mask 14	$6E_H$	56

Table 64 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
WUF2M_15	Wakeup Frame 2 Mask 15	$6F_H$	56
WUF2O	Wakeup Frame 2 Offset	70_H	56
WUF2CRCL	Wakeup Frame 2 CRC Low	71_H	58
WUF2CRCH	Wakeup Frame 2 CRC High	72_H	58
Res23	Reserved 23	73_H	33
Res24	Reserved 24	74_H	33
Res25	Reserved 25	75_H	33
Res26	Reserved 26	76_H	34
Res27	Reserved 27	77_H	34
WUC	Wakeup Control	78_H	59
Res28	Reserved 28	79_H	34
WUS	Wakeup Status	$7A_H$	60
IPHYC	Internal PHY Control	$7B_H$	60
GPIO54C	GPIO[5:4] Control	$7C_H$	61
Res29	Reserved 29	$7D_H$	34
GPIO10C	GPIO[1:0] Control	$7E_H$	62
GPIO32C	GPIO[3:2] Control	$7F_H$	63
Test	TEST	80_H	64
TM	Test Mode	81_H	64

The register is addressed wordwise.

Table 65 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is readable and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)

Table 65 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Interrupt high, self clearing	ihsc	Differentiates the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiates the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiates the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiates the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

Table 66 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

6.1.1 System Registers

Ethernet Control 0

EC0 **Offset** **Reset Value**
Ethernet Control 0 **00_H** **09_H**

7	6	5	4	3	2	1	0
TXE	**RXE**	**RXFCE**	**WOE**	**RXSA**	**SBO**	**RXMA**	**RXCS**
rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TXE	7	rw	**Ethernet Transmission Enable**
RXE	6	rw	**Ethernet Receive Enable**
RXFCE	5	rw	**Receive Pause Frame Enable**
WOE	4	rw	**Wake-on-LAN Mode Enable**
RXSA	3	rw	**Status Append at the End of Received Packet Enable**

Field	Bits	Type	Description
SBO	2	rw	**Stop Back Off** 0_B **CNOT**, Back-off counter isn't affected by carrier 1_B **CST**, Back-off counter stops when carrier is active and resumes when carrier drops
RXMA	1	rw	**Receive All Multicast Packet**
RXCS	0	rw	**Include CRC in Receive Packet**

Ethernet Control 1

EC1 **Offset** **Reset Value**

Ethernet Control 1 **01_H** **00_H**

7	6	5	4	3	2	1	0
Res		**FD**	**10M**	**RM**	**MII**	Res	
ro		rw	rw	rw	r	ro	

Field	Bits	Type	Description
Res	7:6	ro	**Reserved**
FD	5	rw	**Full Dublex** 0_B **HDM**, Half-duplex mode 1_B **FDM**, Full-duplex mode
10M	4	rw	**10mode** 0_B **10Base**, 10Base-T mode 1_B **100Base**, 100Base-T mode
RM	3	rw	**Reset MAC** After write 1, HW will clear this bit after MAC reset.
MII	2	r	**MII Mode** 0_B **MIIM**, MII mode
Res	1:0	ro	**Reserved**

Ethernet Control 2

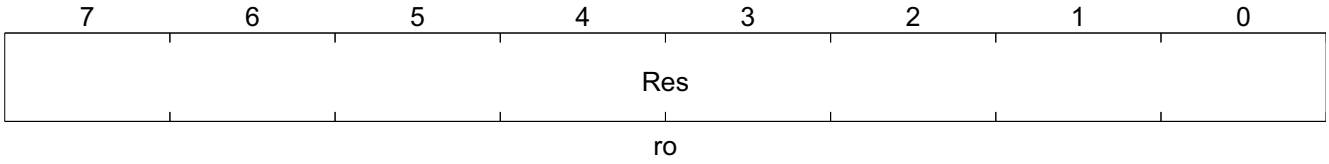
EC2	Offset	Reset Value
Ethernet Control 2	02_H	00_H

7	6	5	4	3	2	1	0
MEPL	Res	**LEEPRS**	**EEPRW**	**LB**	**PROM**	**RXBP**	**EP3RC**
rw	ro	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MEPL	7	rw	**Max Ethernet Packet Length** 0_B **1528B**, 1528 bytes 1_B **1638B**, 1638 bytes, Default is 0
Res	6	ro	**Reserved**
LEEPRS	5	rw	**Load EEPROM Start** When this bit is written with 1, HW will start to load EEPROM.
EEPRW	4	rw	**EEPROM Write Enable/disable** 0_B **WEDC**, EEPROM writes enable/disable command 1_B **WC**, EEPROM writes command
LB	3	rw	**MAC Loop Back Mode Enable**
PROM	2	rw	**Promiscuous** 0_B **RPP**, Receives packets which pass the address filter 1_B **RAP**, Receives any packet
RXBP	1	rw	**Receive Bad Packets** 0_B **FABP**, Filters all bad packet 1_B **RBPP**, Receives bad packets which pass the address filter
EP3RC	0	rw	**EP3 Read Cleared** 0_B **AEP3**, Access EP3, no effect to those registers. 1_B **OEP3**, Once EP3 is accessed, those registers (2B-2F, 7A) will be cleared.

Reserved 0

Res0	Offset	Reset Value
Reserved 0	03_H	00_H



Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

Similar Registers

Table 67 Reserved Registers

Register Short Name	Register Long Name	Offset Address	Page Number
Res1	Reserved 1	04_H	
Res2	Reserved 2	05_H	
Res3	Reserved 3	06_H	
Res4	Reserved 4	07_H	
Res5	Reserved 5	16_H	
Res6	Reserved 6	17_H	
Res7	Reserved 7	$1C_H$	
Res8	Reserved 8	$1D_H$	
Res9	Reserved 9	$1E_H$	
Res10	Reserved 10	$1F_H$	
Res11	Reserved 11	24_H	
Res12	Reserved 12	29_H	
Res13	Reserved 13	43_H	
Res14	Reserved 14	44_H	
Res15	Reserved 15	45_H	
Res16	Reserved 16	46_H	
Res17	Reserved 17	47_H	
Res18	Reserved 18	$5B_H$	
Res19	Reserved 19	$5C_H$	
Res20	Reserved 20	$5D_H$	
Res21	Reserved 21	$5E_H$	
Res22	Reserved 22	$5F_H$	
Res23	Reserved 23	73_H	
Res24	Reserved 24	74_H	
Res25	Reserved 25	75_H	

Table 67 Reserved Registers (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
Res26	Reserved 26	76_H	
Res27	Reserved 27	77_H	
Res28	Reserved 28	79_H	
Res29	Reserved 29	$7D_H$	
Res30_Res155	Reserved 30~Reserved 155	$82\sim FF_H$	

Multicast Address 0

MA0	Offset	Reset Value
Multicast Address 0	**08_H**	**00_H**

7	6	5	4	3	2	1	0
MAB0							
rw							

Field	Bits	Type	Description
MAB0	7:0	rw	**Multicast 0** Multicast address byte [7:0]

Multicast Address 1

MA1	Offset	Reset Value
Multicast Address 1	**09_H**	**00_H**

7	6	5	4	3	2	1	0
MAB1							
rw							

Field	Bits	Type	Description
MAB1	7:0	rw	**Multicast 1** Multicast address byte [15:8]

Multicast Address 2

MA2	Offset	Reset Value
Multicast Address 2	$0A_H$	00_H

7	6	5	4	3	2	1	0
MAB2							
rw							

Field	Bits	Type	Description
MAB2	7:0	rw	**Multicast 2** Multicast address byte [23:16]

Multicast Address 3

MA3	Offset	Reset Value
Multicast Address 3	$0B_H$	00_H

7	6	5	4	3	2	1	0
MAB3							
rw							

Field	Bits	Type	Description
MAB3	7:0	rw	**Multicast 3** Multicast address byte [31:24]

Multicast Address 4

MA4	Offset	Reset Value
Multicast Address 4	$0C_H$	00_H

7	6	5	4	3	2	1	0
MAB4							
rw							

Field	Bits	Type	Description
MAB4	7:0	rw	**Multicast 4** Multicast address byte [39:32]

Multicast Address 5

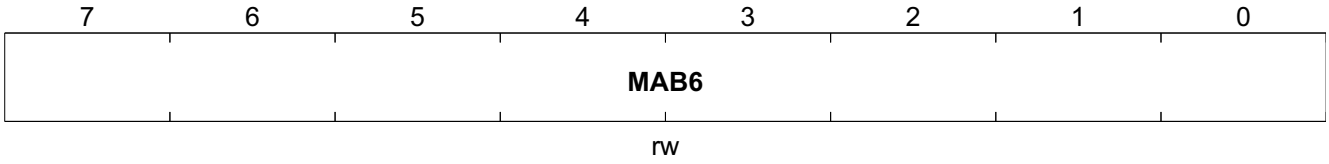
MA5	Offset	Reset Value
Multicast Address 5	$0D_H$	00_H

7	6	5	4	3	2	1	0
MAB5							
rw							

Field	Bits	Type	Description
MAB5	7:0	rw	**Multicast 5** Multicast address byte [47:40]

Multicast Address 6

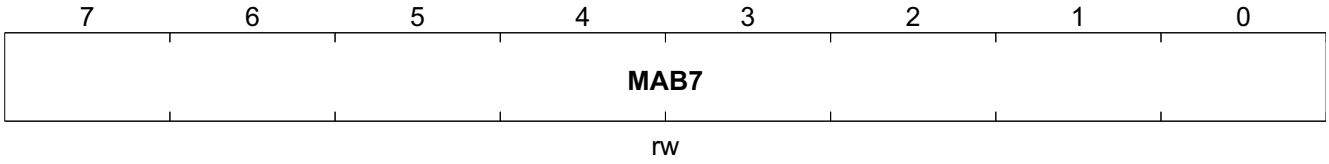
MA6	Offset	Reset Value
Multicast Address 6	$0E_H$	00_H



Field	Bits	Type	Description
MAB6	7:0	rw	**Multicast 6** Multicast address byte [55:48]

Multicast Address 7

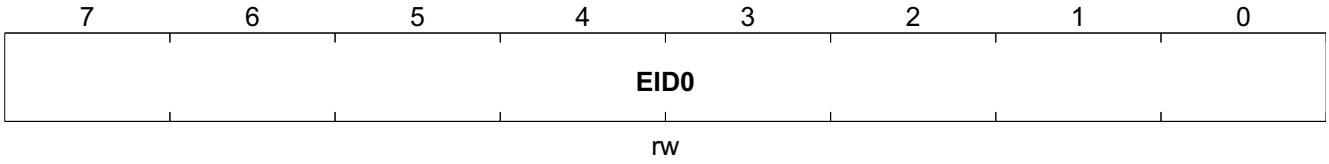
MA7	Offset	Reset Value
Multicast Address 7	$0F_H$	00_H



Field	Bits	Type	Description
MAB7	7:0	rw	**Multicast 7** Multicast address byte [63:56]

Ethernet ID 0

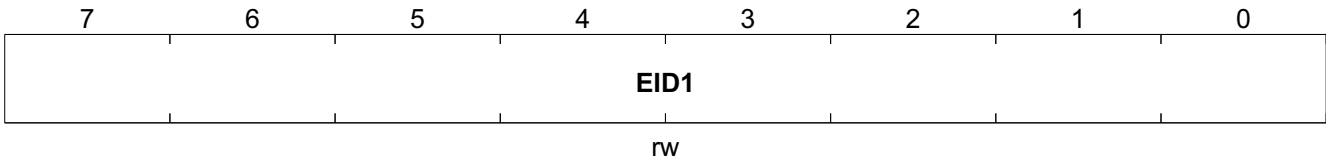
EID0 **Offset** **Reset Value**
Ethernet ID 0 **10_H** **00_H**



Field	Bits	Type	Description
EID0	7:0	rw	**Ethernet ID 0** The 1st byte of Ethernet ID is automatically loaded from EEPROM after HW reset.

Ethernet ID 1

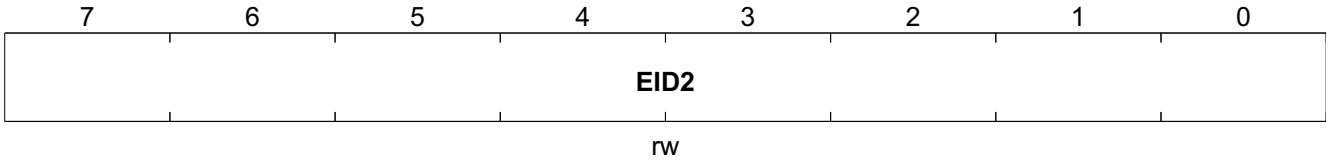
EID1 **Offset** **Reset Value**
Ethernet ID 1 **11_H** **00_H**



Field	Bits	Type	Description
EID1	7:0	rw	**Ethernet ID 1** The 2nd byte of Ethernet ID.

Ethernet ID 2

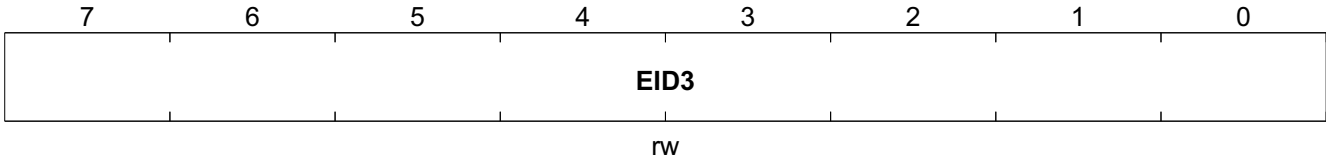
EID2	Offset	Reset Value
Ethernet ID 2	12_H	00_H



Field	Bits	Type	Description
EID2	7:0	rw	**Ethernet ID 2** The 3rd byte of Ethernet ID.

Ethernet ID 3

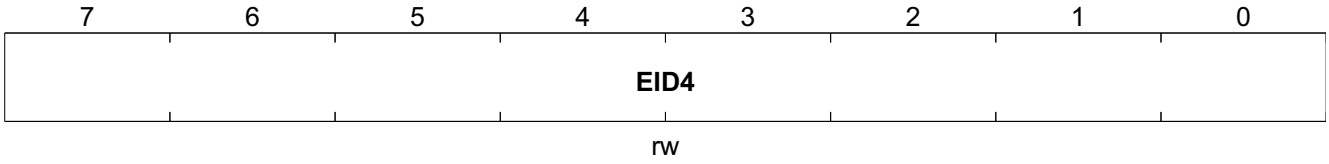
EID3	Offset	Reset Value
Ethernet ID 3	13_H	00_H



Field	Bits	Type	Description
EID3	7:0	rw	**Ethernet ID 3** The 4th byte of Ethernet ID.

Ethernet ID 4

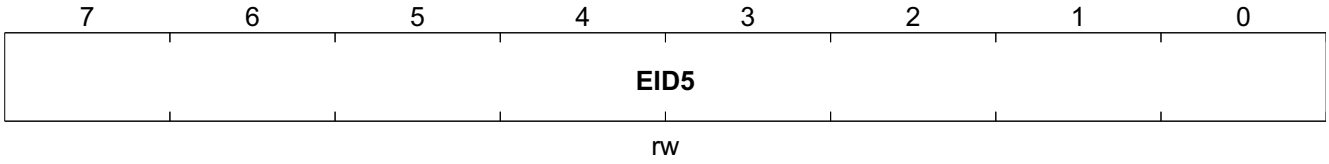
EID4	Offset	Reset Value
Ethernet ID 4	14_H	00_H



Field	Bits	Type	Description
EID4	7:0	rw	**Ethernet ID 4** The 5th byte of Ethernet ID.

Ethernet ID 5

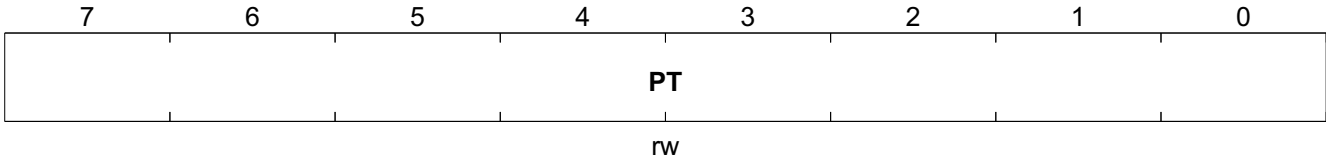
EID5	Offset	Reset Value
Ethernet ID 5	15_H	00_H



Field	Bits	Type	Description
EID5	7:0	rw	**Ethernet ID 5** The 6th byte of Ethernet ID.

Pause Timer

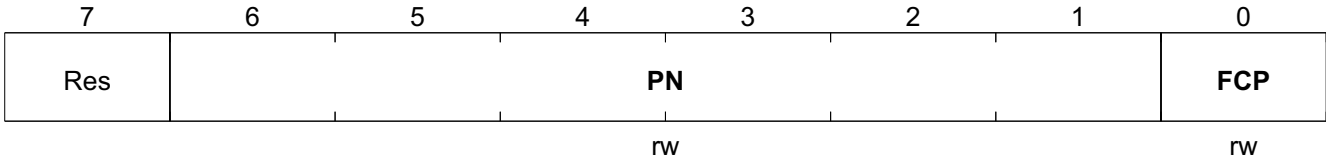
PT	Offset	Reset Value
Pause Timer	18_H	00_H



Field	Bits	Type	Description
PT	7:0	rw	**Pause Timer** The [11:4] of pause time in the PAUSE frame.

Receive Packet Number Based Flow Control

RPNBFC	Offset	Reset Value
Receive Packet Number Based Flow Control	$1A_H$	00_H



Field	Bits	Type	Description
PN	6:1	rw	**Packet Number** This field specifies the threshold for transmitting the PAUSE frame. As the received packet number is more than or equal to this field, the PAUSE frame is sent automatically by HW.
FCP	0	rw	**Flow Control Packet** 1_B **RPN**, Enables pause frame transmission based on received packet number

Occupied Receive FIFO Based Flow Control

ORFBFC	Offset	Reset Value
Occupied Receive FIFO Based Flow Control	$1B_H$	00_H

7	6	5	4	3	2	1	0
Res	RXS						FCRXS
	rw						rw

Field	Bits	Type	Description
RXS	6:1	rw	**RX Size** This field specifies the Kbyte threshold for transmitting the PAUSE frame. As the received FIFO is occupied than or equal to this field, the PAUSE frame is sent automatically by HW. If this field = 2, as receive FIFO is occupied more than or equal to 2 Kbyte, the PAUSE frame is transmitted.
FCRXS	0	rw	**Flow Control RX Size** 1_B **RFS**, Enables pause frame transmission based on occupied received FIFO size

EP1 Control

EP1C	Offset	Reset Value
EP1 Control	$1C_H$	04_H

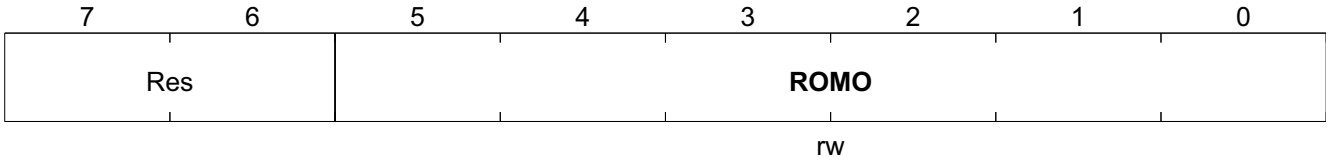
7	6	5	4	3	2	1	0
EP1S0E	FID		FI				
rw	rw		rw				

Field	Bits	Type	Description
EP1S0E	7	rw	**EP1 Send** 0_B **DEP1**, Disables EP1 send 1-byte 00 function 1_B **EEP1**, Enables EP1 send 1-byte 00 when more than frame_ interval's NAK is received
FID	6:5	rw	**Frame Interval Detail** This value is the detailed scale of frame interval, it is from 0ms to 3ms. 00_B , for more than 0 plus frame_interval ms NAK, EP1 sends 1-byte 00 01_B , for more than 1 plus frame_interval ms NAK, EP1 sends 1-byte 00 11_B , for more than 3 plus frame_interval ms NAK, EP1 sends 1-byte 00

Field	Bits	Type	Description
FI	4:0	rw	**Frame Interval** This value multiply with 4 is the frame interval, it is from 4ms to 124ms 00001_B, for more than 4 ms NAK, EP1 sends 1-byte 00 00010_B, for more than 8 ms NAK, EP1 sends 1-byte 00 11111_B, for more than 124 ms NAK, EP1 sends 1-byte 00

EEPROM Offset

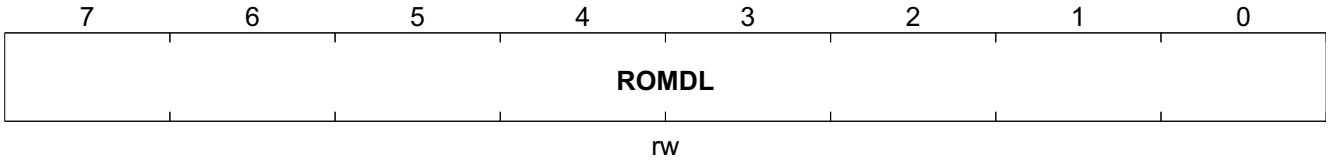
EEPROMO	Offset	Reset Value
EEPROM Offset	**20_H**	**00_H**



Field	Bits	Type	Description
ROMO	5:0	rw	**ROM Offset** SW sets this register when access to EEPROM.

EEPROM Data Low

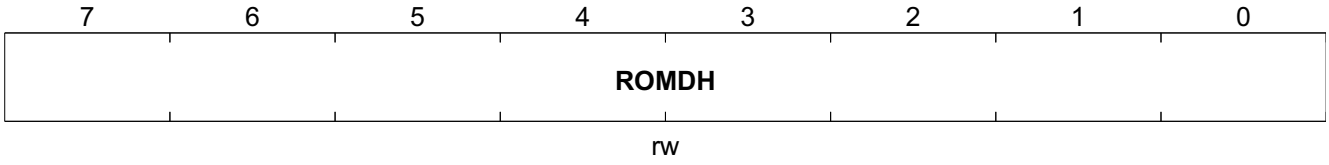
EEPROMDL	Offset	Reset Value
EEPROM Data Low	**21_H**	**00_H**



Field	Bits	Type	Description
ROMDL	7:0	rw	**ROM Data Low** EEPROM Write: The data set in this register will be written to EEPROM EEPROM Read: The data red from EEPROM will be stored in this register

EEPROM Data High

EEPROMDH	Offset	Reset Value
EEPROM Data High	**22_H**	**00_H**



Field	Bits	Type	Description
ROMDH	7:0	rw	**ROM Data High** EEPROM Write: The data set in this register will be written to EEPROM EEPROM Read: The data read from EEPROM will be stored in this register

EEPROM Access Control

EEPROMAC	Offset	Reset Value
EEPROM Access Control	23_H	00_H

7	6	5	4	3	2	1	0
Res					DO	RDE	WRE
					rw	rw	rw

Field	Bits	Type	Description
DO	2	rw	**Done** Set by HW to indicate successful completion of EEPROM access. Clear by SW when initiate a new access to EEPROM
RDE	1	rw	**Read Access to EEPROM** Set by SW to initiate a read access to EEPROM. SW sets this bit after it well setting the rom_offset.
WRE	0	rw	**Write Access to EEPROM** Set by SW to initiate a write access to EEPROM. SW set this bit after it well setting the rom_offset, romdata_lo and romdata_hi.

PHY Address

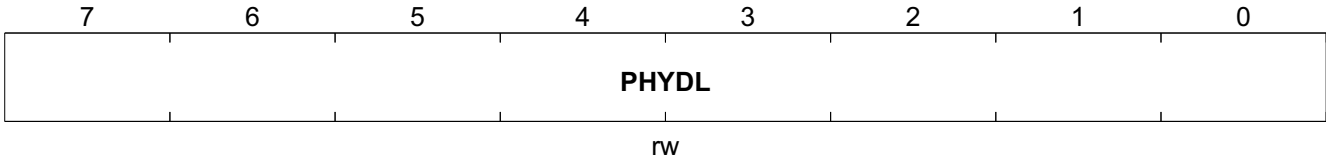
PHYA	Offset	Reset Value
PHY Address	25_H	00_H

7	6	5	4	3	2	1	0
Res			PHYA				
			rw				

Field	Bits	Type	Description
PHYA	4:0	rw	**MII PHY Address**

PHY Data Low

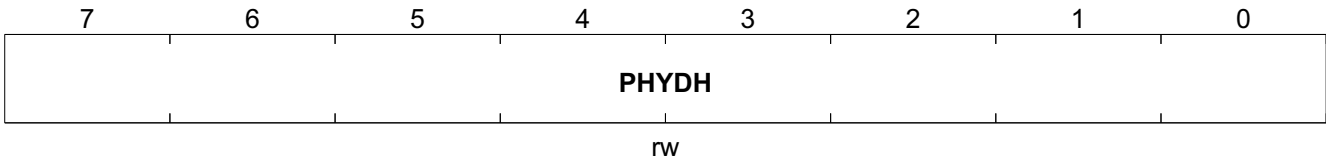
PHYDL	Offset	Reset Value
PHY Data Low	26_H	00_H



Field	Bits	Type	Description
PHYDL	7:0	rw	**PHY Data Low** SW set this register when write to PHY register. HW set this register when read data from PHY register.

PHY Data High

PHYDH	Offset	Reset Value
PHY Data High	27_H	00_H



Field	Bits	Type	Description
PHYDH	7:0	rw	**PHY Data High** SW set this register when write to PHY register. HW set this register when read data from PHY register.

PHY Access Control

PHYAC	Offset	Reset Value
PHY Access Control	28_H	00_H

7	6	5	4	3	2	1	0
DO	RDPHY	WRPHY	PHYRA				
rw	rw	rw	rw				

Field	Bits	Type	Description
DO	7	rw	**Done** Set by HW to indicate successful completion of PHY access. Clear by SW when initiate a new access to PHY.
RDPHY	6	rw	**Read Access to PHY Register** Set by SW to initiate a read access to PHY register. SW set this bit after it well setting the phy_addr and phyreg_addr.
WRPHY	5	rw	**Write Access to PHY Register** Set by SW to initiate a write access to PHY register. SW set this bit after it well setting the phy_addr, phyreg_addr and phyreg_data.
PHYRA	4:0	rw	**PHY Register Address**

USB Bus Status

USBBS	Offset	Reset Value
USB Bus Status	$2A_H$	00_H

7	6	5	4	3	2	1	0
Res						USBR	USBS
						rw	rw

Field	Bits	Type	Description
USBR	1	rw	**USB Bus in Resume State** Set by HW to indicate usb bus in resumed state. Clear by SW read this register.
USBS	0	rw	**USB Bus in Suspend State** Set by HW to indicate usb bus in suspended state. Clear by SW read this register.

Transmit Status 1

TS1 **Offset** **Reset Value**

Transmit Status 1 **$2B_H$** **00_H**

7	6	5	4	3	2	1	0
TXUE	**EC**	**LC**	**NC**	**CL**	**JTO**	Res	
r	r	r	r	r	r		

Field	Bits	Type	Description
TXUE	7	r	**TX Underrun Error** Set by HW to indicate tx underrun error. Clear by SW read this register or after EP3 is accessed.
EC	6	r	**Excessive Collision** Set by HW to indicate excessive collision. Clear by SW read this register or after EP3 is accessed.
LC	5	r	**Late Collision Error** Set by HW to indicate late collision error. Clear this register by SW Read or after EP3 is accessed.
NC	4	r	**No Carrier** Set by HW to indicate no carrier. Clear this register by SW Read or after EP3 is accessed.
CL	3	r	**Carrier Loss** Set by HW to indicate carrier loss. Clear this register by SW Read or after EP3 is accessed.
JTO	2	r	**Jabber Time Out** Set by HW to indicate jabber time out. Clear this register by SW Read or after EP3 is accessed.

Transmit Status 2

TS2	Offset	Reset Value
Transmit Status 2	$2C_H$	00_H

7	6	5	4	3	2	1	0
TXFF	**TXFE**	Res		**TXPC**			
r	r			r			

Field	Bits	Type	Description
TXFF	7	r	**TX Fifo Full** Set by HW to indicate tx fifo full. Clear this register by SW Read or after EP3 is accessed.
TXFE	6	r	**TX Fifo Empty** Set by HW to indicate tx fifo empty. Clear this register by SW Read or after EP3 is accessed.
TXPC	3:0	r	**TX Packet Count** Set by HW to indicate Ethernet transmit packet counts every interrupt EP polling. If more than 15 packets have been transmitted, this value will stay as 15. Clear by SW read or after EP3 is accessed.

Receive Status

RS	Offset	Reset Value
Receive Status	$2D_H$	00_H

7	6	5	4	3	2	1	0
Res						**RXP**	**RXO**
						r	r

Field	Bits	Type	Description
RXP	1	r	**RX Pause** Set by HW to indicate a PAUSE frame is received. Clear this register by SW Read or after EP3 is accessed.
RXO	0	r	**RX Overflow** Set by HW to indicate external SRAM overflow. Clear this register by SW Read or after EP3 is accessed.

Receive Lost Packet Count High

RLPCH — **Receive Lost Packet Count High**

Offset $2E_H$

Reset Value 00_H

7	6	5	4	3	2	1	0
RPL	RXLPC						
r	r						

Field	Bits	Type	Description
RPL	7	r	**Received Packet Lost**
RXLPC	6:0	r	**RX Lost Packet Counts** The [14:8] of lost packet counts due to receive FIFO overflow. Clear this register by SW Read or after EP3 is accessed.

Receive Lost Packet Count Low

RLPCL — **Receive Lost Packet Count Low**

Offset $2F_H$

Reset Value 00_H

7	6	5	4	3	2	1	0
RXLPC							
r							

Field	Bits	Type	Description
RXLPC	7:0	r	**RX Lost Packet Counts** The [7:0] of lost packet counts due to receive FIFO overflow. Clear this register by SW Read or after EP3 is accessed.

Wakeup Frame 0 Mask

WUF0M_0 — **Wakeup Frame 0 Mask**

Offset 30_H

Reset Value 00_H

7	6	5	4	3	2	1	0
F0M							
rw							

Field	Bits	Type	Description
F0M	7:0	rw	**The 128 Mask Bits for Frame 0**

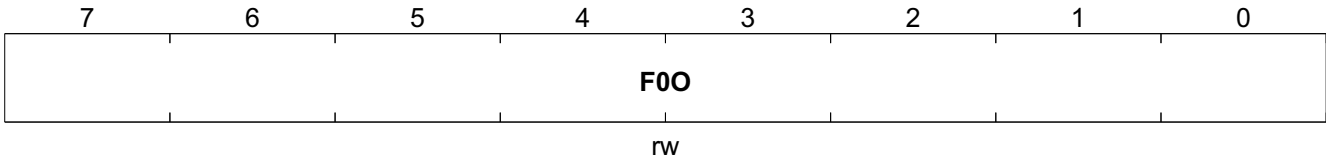
Similar Registers

Table 68 Wakeup Frame 0 Mask Registers

Register Short Name	Register Long Name	Offset Address	Page Number
WUF0M_1	Wakeup Frame 0 Mask 1	31_H	
WUF0M_2	Wakeup Frame 0 Mask 2	32_H	
WUF0M_3	Wakeup Frame 0 Mask 3	33_H	
WUF0M_4	Wakeup Frame 0 Mask 4	34_H	
WUF0M_5	Wakeup Frame 0 Mask 5	35_H	
WUF0M_6	Wakeup Frame 0 Mask 6	36_H	
WUF0M_7	Wakeup Frame 0 Mask 7	37_H	
WUF0M_8	Wakeup Frame 0 Mask 8	38_H	
WUF0M_9	Wakeup Frame 0 Mask 9	39_H	
WUF0M_10	Wakeup Frame 0 Mask 10	$3A_H$	
WUF0M_11	Wakeup Frame 0 Mask 11	$3B_H$	
WUF0M_12	Wakeup Frame 0 Mask 12	$3C_H$	
WUF0M_13	Wakeup Frame 0 Mask 13	$3D_H$	
WUF0M_14	Wakeup Frame 0 Mask 14	$3E_H$	
WUF0M_15	Wakeup Frame 0 Mask 15	$3F_H$	

Wakeup Frame 0 Offset

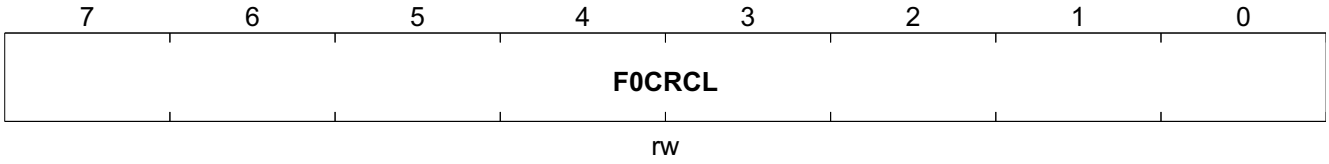
WUF0O_0	Offset	Reset Value
Wakeup Frame 0 Offset	**40_H**	**00_H**



Field	Bits	Type	Description
F0O	7:0	rw	**Offset for Wakeup Frame 0**

Wakeup Frame 0 CRC Low

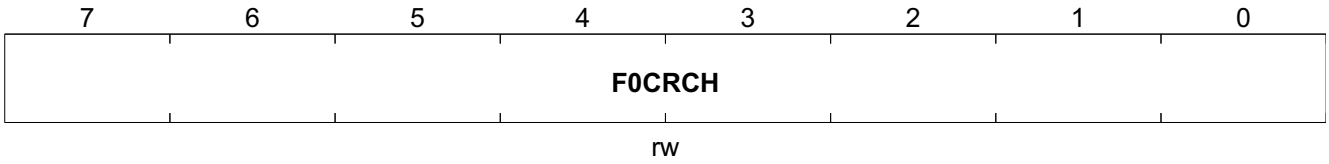
WUF0CRCL	Offset	Reset Value
Wakeup Frame 0 CRC Low	41_H	00_H



Field	Bits	Type	Description
F0CRCL	7:0	rw	**The Low Byte of CRC16 Match for Frame 0**

Wakeup Frame 0 CRC High

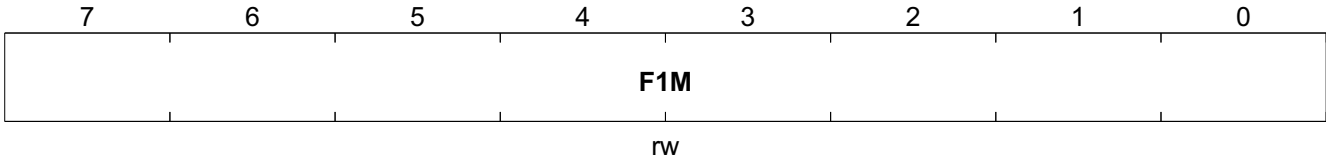
WUF0CRCH	Offset	Reset Value
Wakeup Frame 0 CRC High	42_H	00_H



Field	Bits	Type	Description
F0CRCH	7:0	rw	**The High Byte of CRC16 Match for Frame 0**

Wakeup Frame 1 Mask

WUF1M_0	Offset	Reset Value
Wakeup Frame 1 Mask	48_H	00_H



Field	Bits	Type	Description
F1M	7:0	rw	**The 128 Mask Bits for Frame 1**

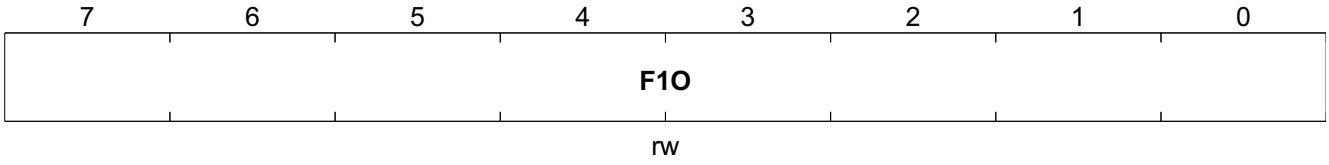
Similar Registers

Table 69 Wakeup Frame 1 Mask Registers

Register Short Name	Register Long Name	Offset Address	Page Number
WUF1M_1	Wakeup Frame 1 Mask 1	49_H	
WUF1M_2	Wakeup Frame 1 Mask 2	$4A_H$	
WUF1M_3	Wakeup Frame 1 Mask 3	$4B_H$	
WUF1M_4	Wakeup Frame 1 Mask 4	$4C_H$	
WUF1M_5	Wakeup Frame 1 Mask 5	$4D_H$	
WUF1M_6	Wakeup Frame 1 Mask 6	$4E_H$	
WUF1M_7	Wakeup Frame 1 Mask 7	$4F_H$	
WUF1M_8	Wakeup Frame 1 Mask 8	50_H	
WUF1M_9	Wakeup Frame 1 Mask 9	51_H	
WUF1M_10	Wakeup Frame 1 Mask 10	52_H	
WUF1M_11	Wakeup Frame 1 Mask 11	56_H	
WUF1M_12	Wakeup Frame 1 Mask 12	54_H	
WUF1M_13	Wakeup Frame 1 Mask 13	55_H	
WUF1M_14	Wakeup Frame 1 Mask 14	56_H	
WUF1M_15	Wakeup Frame 1 Mask 15	57_H	

Wakeup Frame 1 Offset

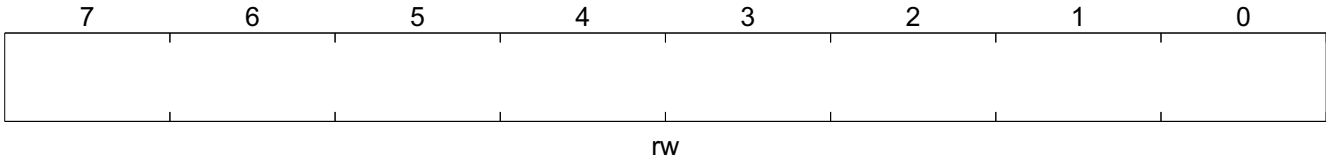
WUF1O	Offset	Reset Value
Wakeup Frame 1 Offset	58_H	00_H



Field	Bits	Type	Description
F1O	7:0	rw	**Offset for Wakeup Frame 1**

Wakeup Frame 1 CRC Low

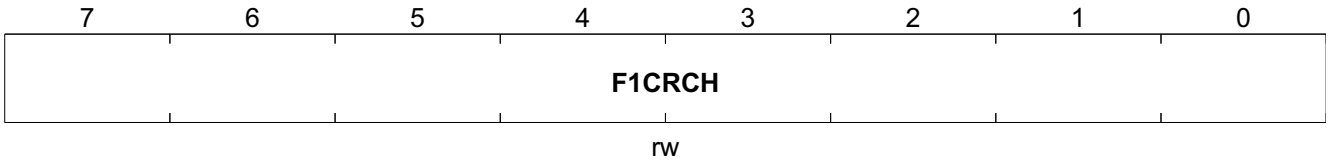
WUF1CRCL	Offset	Reset Value
Wakeup Frame 1 CRC Low	59_H	00_H



Field	Bits	Type	Description
	7:0	rw	**The Low Byte of CRC16 Match for Frame 1**

Wakeup Frame 1 CRC High

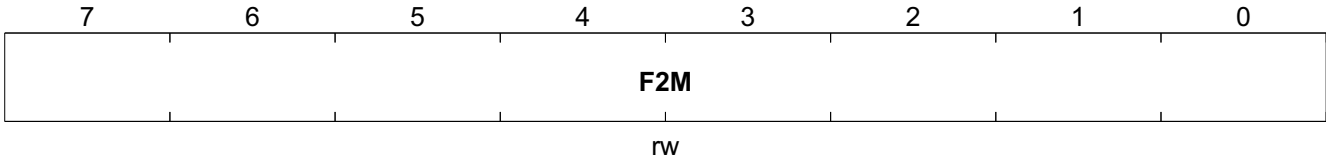
WUF1CRCH	Offset	Reset Value
Wakeup Frame 1 CRC High	$5A_H$	00_H



Field	Bits	Type	Description
F1CRCH	7:0	rw	**The High Byte of CRC16 Match for Frame 1**

Wakeup Frame 2 Mask

WUF2M	Offset	Reset Value
Wakeup Frame 2 Mask	60_H	00_H



Field	Bits	Type	Description
F2M	7:0	rw	**The 128 Mask Bits for Frame 2**

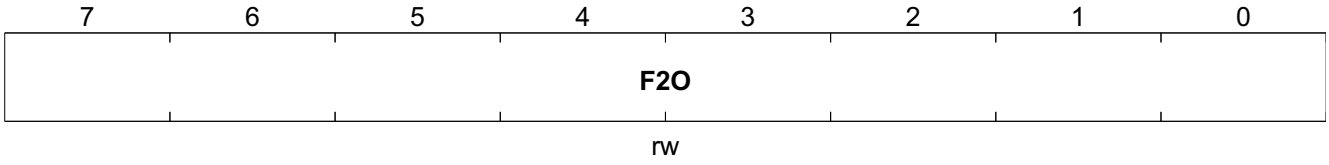
Similar Registers

Table 70 Wakeup Frame 2 Mask Registers

Register Short Name	Register Long Name	Offset Address	Page Number
WUF2M_1	Wakeup Frame 2 Mask 1	61_H	
WUF2M_2	Wakeup Frame 2 Mask 2	62_H	
WUF2M_3	Wakeup Frame 2 Mask 3	63_H	
WUF2M_4	Wakeup Frame 2 Mask 4	64_H	
WUF2M_5	Wakeup Frame 2 Mask 5	65_H	
WUF2M_6	Wakeup Frame 2 Mask 6	66_H	
WUF2M_7	Wakeup Frame 2 Mask 7	67_H	
WUF2M_8	Wakeup Frame 2 Mask 8	68_H	
WUF2M_9	Wakeup Frame 2 Mask 9	69_H	
WUF2M_10	Wakeup Frame 2 Mask 10	$6A_H$	
WUF2M_11	Wakeup Frame 2 Mask 11	$6B_H$	
WUF2M_12	Wakeup Frame 2 Mask 12	$6C_H$	
WUF2M_13	Wakeup Frame 2 Mask 13	$6D_H$	
WUF2M_14	Wakeup Frame 2 Mask 14	$6E_H$	
WUF2M_15	Wakeup Frame 2 Mask 15	$6F_H$	

Wakeup Frame 2 Offset

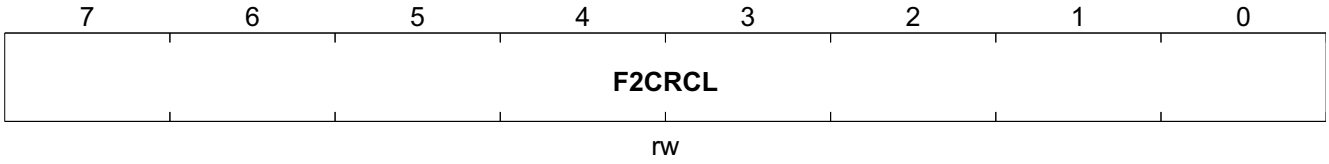
WUF2O	Offset	Reset Value
Wakeup Frame 2 Offset	70_H	00_H



Field	Bits	Type	Description
F2O	7:0	rw	**Offset for Wakeup Frame 2**

Wakeup Frame 2 CRC Low

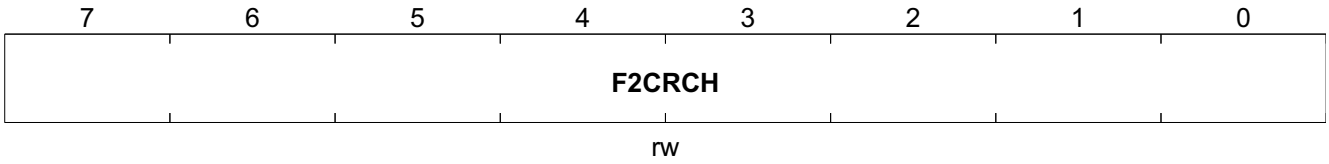
WUF2CRCL	Offset	Reset Value
Wakeup Frame 2 CRC Low	71_H	00_H



Field	Bits	Type	Description
F2CRCL	7:0	rw	**The Low Byte of CRC16 Match for Frame 2**

Wakeup Frame 2 CRC High

WUF2CRCH	Offset	Reset Value
Wakeup Frame 2 CRC High	72_H	00_H



Field	Bits	Type	Description
F2CRCH	7:0	rw	**The High Byte of CRC16 Match for Frame 2**

Wakeup Control

WUC	Offset	Reset Value
Wakeup Control	78_H	04_H

7	6	5	4	3	2	1	0
EMP	**ELS**	**EWF0**	**WUF1**	**WUF2**	**CRC16**	Res	
rw	rw	rw	rw	rw	rw		

Field	Bits	Type	Description
EMP	7	rw	**Enable Magic Packet** Set by SW to enable magic packet wakeup function. 1_B **EMP**, Enables magic packet wakeup function
ELS	6	rw	**Enable Link Status** Set by SW to enable link status wakeup function. 1_B **ELS**, Enables link status wakeup function
EWF0	5	rw	**Enable Wakeup Frame 0** Set by SW to enable wakeup frame0 wakeup function 1_B **EWF0**, Enables wakeup frame0 wakeup function
WUF1	4	rw	**Enable Wakeup Frame 1** Set by SW to enable wakeup frame1 wakeup function 1_B **EWF1**, Enables wakeup frame1 wakeup function
WUF2	3	rw	**Enable Wakeup Frame 2** Set by SW to enable wakeup frame2 wakeup function 1_B **EWF2**, Enables wakeup frame2 wakeup function
CRC16	2	rw	**CRC-16 Initial Type** 0_B **CRC16**, CRC-16 initial contents = 0000_H 1_B **CRC16**, CRC-16 initial contents = $ffff_H$

Wakeup Status

WUS	Offset	Reset Value
Wakeup Status	$7A_H$	00_H

7	6	5	4	3	2	1	0
RXMP	**LW**	**RXWF**	Res				**LS**
r	r	r					r

Field	Bits	Type	Description
RXMP	7	r	**Receives a Magic Packet** Set by HW when receive a magic packet. Clear by SW read this register. 1_B **RMP**, Means ADM8513/X receives a magic packet
LW	6	r	**Receives a Link Status Change** Set by HW when link status change.Clear by SW read this register. 1_B **RLS**, Means ADM8513/X receives a link status change
RXWF	5	r	**Receives a Wakeup Frame** Set by HW when receive a wakeup frame.Clear by SW read this register. 1_B **RWF**, Means ADM8513/X receives a wakeup frame
LS	0	r	**Indicate the Current Link Status** link_sts 0_B **LOFF**, Link off 1_B **LON**, Link on

Internal PHY Control

IPHYC	Offset	Reset Value
Internal PHY Control	$7B_H$	00_H

7	6	5	4	3	2	1	0
Res						**EPHY**	**PHYR**
						rw	rw

Field	Bits	Type	Description
EPHY	1	rw	**Enable PHY** 0_B **DIN**, Disables internal 10/100 PHY 1_B **EIN**, Enables internal 10/100 PHY

Field	Bits	Type	Description
PHYR	0	rw	**Internal PHY Reset** The internal PHY is reset when this bit is written with 1 and stops reset when this bit is written with 0. 1_B **RIPHY**, Reset internal PHY

GPIO[5:4] Control

GPIO54C **Offset** **Reset Value**

GPIO[5:4] Control **$7C_H$** **00_H**

7	6	5	4	3	2	1	0
Res		**G5OE**	**G5OV**	**G5IV**	**G4OE**	**G4OV**	**G4IV**
		rw	rw	r	rw	rw	r

Field	Bits	Type	Description
G5OE	5	rw	**GPIO5 Output Enable** 0_B **IN**, GPIO5 is used for input 1_B **OUT**, GPIO5 is used for output
G5OV	4	rw	**GPIO5 Output Value** When GPIO5 is used for output, this value is driven to GPIO5 pin.
G5IV	3	r	**GPIO5 Input Value** When GPIO5 is used for input, this field reflects the status of GPIO5. Default is pulled-down.
G4OE	2	rw	**GPIO4 Output Enable** 0_B **IN**, GPIO4 is used for input 1_B **OUT**, GPIO4 is used for output
G4OV	1	rw	**GPIO4 Output Value** When GPIO4 is used for output, this value is driven to GPIO4 pin.
G4IV	0	r	**GPIO4 Input Value** When GPIO4 is used for input, this field reflects the status of GPIO4. Default is pulled-down.

GPIO[1:0] Control

GPIO10C	Offset	Reset Value
GPIO[1:0] Control	$7E_H$	00_H

7	6	5	4	3	2	1	0
Res		G1OE	G1OV	G1IV	G1OE	G0OV	G0IV
		rw	rw	r	rw	rw	r

Field	Bits	Type	Description
G1OE	5	rw	**GPIO1 Output Enable** 0_B **IN**, GPIO1 is used for input 1_B **OUT**, GPIO1 is used for output
G1OV	4	rw	**GPIO1 Output Value** When GPIO1 is used for output, this value is driven to GPIO1 pin. Set by SW.
G1IV	3	r	**GPIO1 Input Value** When GPIO1 is used for input, this field reflects the status of GPIO1. Set by HW.
G1OE	2	rw	**GPIO0 Output Enable** 0_B **IN**, GPIO0 is used for input 1_B **OUT**, GPIO0 is used for output
G0OV	1	rw	**GPIO0 Output Value** When GPIO0 is used for output, this value is driven to GPIO0 pin. Set by SW.
G0IV	0	r	**GPIO0 Input Value** When GPIO0 is used for input, this field reflects the status of GPIO0. Set by HW.

GPIO[3:2] Control

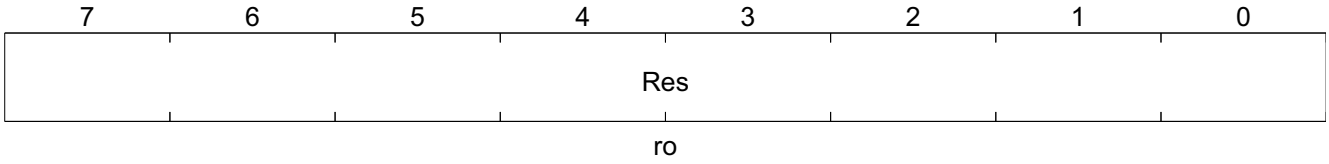
GPIO32C	Offset	Reset Value
GPIO[3:2] Control	$7F_H$	00_H

7	6	5	4	3	2	1	0
Res		G3OE	G3OV	G3IV	G2OE	G2OV	G2IV
		rw	rw	r	rw	rw	r

Field	Bits	Type	Description
G3OE	5	rw	**GPIO3 Output Enable** 0_B **IN**, GPIO3 is used for input 1_B **OUT**, GPIO3 is used for output
G3OV	4	rw	**GPIO3 Output Value** When GPIO3 is used for output, this value is driven to GPIO3 pin. Set by SW.
G3IV	3	r	**GPIO3 Input Value** When GPIO3 is used for input, this field reflects the status of GPIO3. Set by HW.
G2OE	2	rw	**GPIO2 Output Enable** 0_B **IN**, GPIO2 is used for input 1_B **OUT**, GPIO2 is used for output
G2OV	1	rw	**GPIO2 Output Value** When GPIO2 is used for output, this value is driven to GPIO2 pin. Set by SW.
G2IV	0	r	**GPIO2 Input Value** When GPIO2 is used for input, this field reflects the status of GPIO2. Set by HW.

TEST

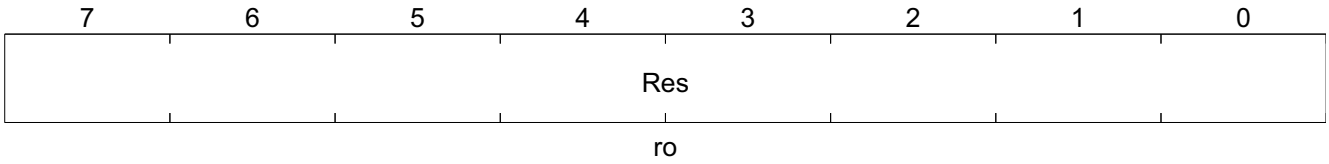
Test **Offset** **Reset Value**
TEST **80_H** **00_H**



Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

Test Mode

TM **Offset** **Reset Value**
Test Mode **81_H** **00_H**



Field	Bits	Type	Description
Res	7:0	ro	**Reserved**

6.2 PHY Registers Description

Table 71 Registers Address SpaceRegisters Address Space

Module	Base Address	End Address	Note
System Registers	$0000\ 0000_H$	$0000\ 0006_H$	

Table 72 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
CTL	Control	0_H	**67**
STA	Status	1_H	**68**
PHYI1	PHY Identifier 1	2_H	**70**
PHYI2	PHY Identifier 2	3_H	**70**
ANA	Auto-Negotiation Advertisement	4_H	**71**

Table 72 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
ANLPA	Auto-Negotiation Link Partner Ability	5_H	72
ANE	Auto-Negotiation Expansion	6_H	72

The register is addressed wordwise.

Table 73 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is readable and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is readable and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is readable and writable by SW.

Table 74 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

6.2.1 PHY Registers

Control

CTL	Offset	Reset Value
Control	0_H	1000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	**LP**	**SS**	**ANE**	**PD**	**ISO**	**RA**	**DM**	**CT**	Res						
rwsc	rw	rw	rw	rw	rw	rwsc	rw	ro							

Field	Bits	Type	Description
RST	15	rwsc	**Reset** 0_B **NO**, Normal operation 1_B **PR**, PHY Reset
LP	14	rw	**Loopback** 0_B **DL**, Disable loopback 1_B **EL**, Enable loopback
SS	13	rw	**Speed Selection** 0_B **10M**, 10 Mbit/s 1_B **100M**, 100 Mbit/s
ANE	12	rw	**Autonegotiation Enable** 0_B **DAN**, Disable auto-neg 1_B **EAN**, Enable auto-neg
PD	11	rw	**Power Down** 0_B **NO**, Normal operation 1_B **PD**, Power Down
ISO	10	rw	**Isolate** 0_B **NO**, normal operation 1_B **IPHY**, isolate PHY from MII
RA	9	rwsc	**Restart Autonegotiation** 1_B **RAN**, Restart Auto-neg
DM	8	rw	**Duplex Mode** 0_B **HA**, Half 1_B **FU**, Full
CT	7	ro	**Collision Test** Not implemented

SC

Self Clearing

Reset

Reset this port only. This will cause the following:

1. Restart the auto-negotiation process.

2. Reset the registers to their default values. Note that this does not affect registers 20, 22, 30 or 31. These registers are not reset by this bit to allow test configurations to be written and then not affected by resetting the port.
   Note: No reset is performed to analogue sections of the port. There is also no physical reset to any internal clock synthesisers or the local clock recovery oscillator which will continue to run throughout the reset period. However since the port is restarted and autoneg re-run the process of locking the frequency of the local oscillator (slave) to the reference oscillator (master) will be repeated as it is at the start of any link initialization process.

LoopbackLoop back of transmit data to receive via a path as closed to the wire as possible. When set inhibits actual transmission on the wire.

Speed Selection Forces speed of Phy only when auto-negotiation is disabled. The default state of this bit will be determined by a power-up configuration pin in this case. Otherwise it defaults to 1.

Auto-neg Enable Defaults to pin programmed value. When cleared allows forcing of speed and duplex settings. When set (after being cleared) causes re-start of auto-neg process. Pin programming at power-up allows it to come up disabled and for software to write the desired capability before allowing the first negotiation to commence.

Restart Negotiation Only has effect when auto-negotiating. Restarts state machine.

Power Down Has no effect in this device. Test mode power down modes may be implemented in other specific modules.

IsolatePuts RMII receive signals into high impedance state and ignores transmit signals.

Duplex Mode When bit12 is cleared (i.e. autoneg disabled), this bit forces full duplex (bit = 1) or half duplex (bit = 0).

Collision Test Always 0 because collision signal is not implemented.

Status

STA	**Offset**	**Reset Value**
Status	**1_H**	**7849_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
100T4	**100FD**	**100HD**	**10FD**	**10HD**	**100TFD**	**100THD**	Res		**MFPS**	**ANC**	**RF**	**ANA**	**LS**	**JD**	**EC**
ro	ro	ro	ro	ro	ro	ro			ro	ro	ro, lh	ro	ro, ll	ro, lh	ro

Field	Bits	Type	Description
100T4	15	ro	**100 BASE T4** Not supported
100FD	14	ro	**100BASE-X Full Duplex** 0_B **100FDN**, PHY is not 100BASE-X full duplex capable 1_B **100FD**, PHY is 100BASE-X full duplex capable
100HD	13	ro	**100BASE-X Half Duplex** 0_B **100HDN**, PHY is not 100BASE-X half duplex capable 1_B **100HD**, PHY is 100BASE-X half duplex capable
10FD	12	ro	**10 Mbit/s Full Duplex** 0_B **10FDN**, PHY is not 10 Mbit/s Full duplex capable 1_B **10FD**, PHY is 10 Mbit/s Full duplex capable

Field	Bits	Type	Description
10HD	11	ro	**10 Mbit/s Half Duplex** 0_B **10HDN**, PHY is not 10 Mbit/s Half duplex capable 1_B **10HD**, PHY is 10 Mbit/s Half duplex capable
100TFD	10	ro	**100BASE-T2 Full Duplex** Not Supported
100THD	9	ro	**100BASE-T2 Half Duplex** Not Supported
MFPS	6	ro	**MF Preamble Suppression** 0_B **MFPSN**, PHY cannot accept management frames with preamble suppression 1_B **MFPS**, PHY can accept management frames with preamble suppression
ANC	5	ro	**Auto-neg Complete** 0_B **ANI**, Auto-neg incomplete 1_B **ANC**, Auto-neg completed
RF	4	ro, lh	**Remote Fault** 0_B **RFN**, No remote fault detected 1_B **RF**, Remote fault detected
ANA	3	ro	**Auto-neg Ability** 0_B **ANN**, PHY cannot auto-negotiate 1_B **AN**, PHY can auto-negotiate
LS	2	ro, ll	**Link Status** 0_B **LD**, Link is down 1_B **LU**, Link is up
JD	1	ro, lh	**Jabber Detect** 1_B **JCD**, Jabber condition detected
EC	0	ro	**Extended Capability** 0_B **BSC**, Basic register set capabilities only 1_B **EC**, Extended register capabilities

*Note: **Jabber Detect** Only used in 10Base-T mode. Read as 0 in 100Base-TX mode.*

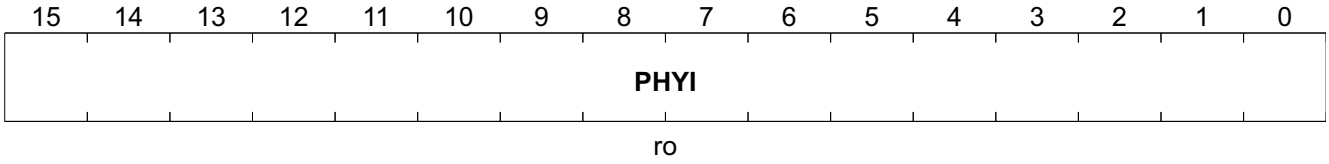
PHY Identifier 2 and 3

Each PHY has an identifier, which is assigned to the device.

The identifier contains a total of 32 bits, which consists of the following: 22 bits of a 24 bit organizationally unique identifier (OUI) for the manufacturer; a 6-bit manufacturer's model number; a 4-bit manufacturer's revision number. For an explanation of how the OUI maps to the register, please refer to IEEE 802-1990 clause 5.1

PHY Identifier 1

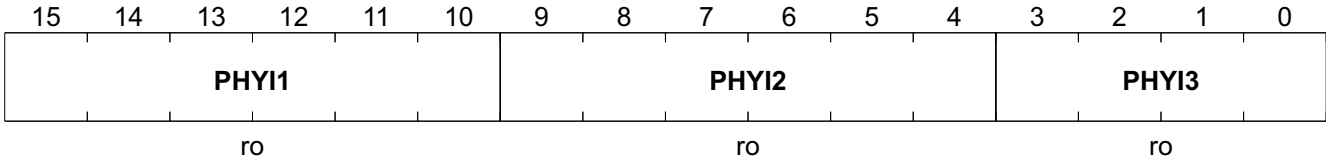
PHYI1	Offset	Reset Value
PHY Identifier 1	2_H	$001D_H$



Field	Bits	Type	Description
PHYI	15:0	ro	**PHY Identifier[31-16]** OUI (bits 3-18)

PHY Identifier 2

PHYI2	Offset	Reset Value
PHY Identifier 2	3_H	2411_H



Field	Bits	Type	Description
PHYI1	15:10	ro	**PHY Identifier[15-10]** OUI (bits 19-24)
PHYI2	9:4	ro	**PHY Identifier[9-4]** Manufacturer's Model Number (bits 5-0)
PHYI3	3:0	ro	**PHY Identifier[3-0]** Revision Number (bits 3-0);Register 3, bit 0 is LS bit of PHY Identifier

Note: This uses the OUI of Infineon-ADMtek, device type of 1 and rev 0.

Auto-Negotiation Advertisement

ANA	Offset	Reset Value
Auto-Negotiation Advertisement	4_H	0001_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Res	**RF**	**NI**		**PAU**	**NI**	**100FD**	**100HD**	**10FD**	**10HD**	**SF**				
rw		rw	ro		rw	ro	rw	rw	rw	rw			ro		

Field	Bits	Type	Description
NP	15	rw	**Next Page** 0_B **NNP**, Device not set to use Next Page 1_B **NP**, Device set to use Next Page
RF	13	rw	**Remote Fault** 0_B **NFD**, No fault detected 1_B **RF**, Local remote fault sent to link partner
NI	12:11	ro	**Not Implemented** Technology ability bits A7-A6
PAU	10	rw	**Pause** Technology ability bit A5
NI	9	ro	**Not Implemented** Technology ability bit A4
100FD	8	rw	**100BASE-TX Full Duplex** Technology ability bit A3 0_B **100NFD**, Unit is not capable of Full Duplex 1_B **100FD**, Unit is capable of Full Duplex
100HD	7	rw	**100BASE-TX Half Duplex** Technology ability bit A2 0_B **100NHD**, Unit is not capable of Half Duplex 100BASE-TX 1_B **100HD**, Unit is capable of Half Duplex
10FD	6	rw	**10BASE-T Full Duplex** Technology ability bit A1 0_B **10NFD**, Unit is not capable of Full Duplex 10BASE-T 1_B **10FD**, Unit is capable of Full Duplex 10BASE-T
10HD	5	rw	**10BASE-T Half Duplex** Technology ability bit A0 0_B **10NHD**, Unit is not capable of Half Duplex 10BASE-T 1_B **10HD**, Unit is capable of Half Duplex 10BASE-T
SF	4:0	ro	**Selector Field** Identifies type of message being sent. Currently only one value is defined.

Auto-Negotiation Link Partner Ability

The register is used to view the advertised capabilities of the link partner once auto negotiation is complete. The contents of this register should not be relied upon unless register 1 bit 5 is set (auto negotiation complete). After negotiation this register should contain a copy of the link partner's register 4. All bits are therefore defined in the same way as for register 4.All bits are readable only.This register is used for Base Page code word only.Base Page Register Format

ANLPA	Offset	Reset Value
Auto-Negotiation Link Partner Ability	5_H	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	**ACK**	**RF**	**TA**								**SF**				
ro	ro	ro	ro								ro				

Field	Bits	Type	Description
NP	15	ro	**Next Page** 0_B , Base Page is requested 1_B , Link Partner is requesting Next Page function
ACK	14	ro	**Acknowledge** Link Partner acknowledgement bit
RF	13	ro	**Remote Fault** Link Partner is indicating a fault
TA	12:5	ro	**Technology Ability** Link Partner technology ability field.
SF	4:0	ro	**Selector Field** Link Partner selector field

Auto-Negotiation Expansion

ANE	Offset	Reset Value
Auto-Negotiation Expansion	6_H	0004_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res											**PDF**	**LPNP**	**NPA**	**PR**	**LPAN**
											ro, lh	ro	ro	ro, lh	ro

Field	Bits	Type	Description
PDF	4	ro, lh	**Parallel Detection Fault** 0_B **NFD**, No fault detected 1_B **FD**, Local Device Parallel Detection Fault

Field	Bits	Type	Description
LPNP	3	ro	**Link Partner Next Page Able** 0_B **NNP**, Link Partner is not Next Page Able 1_B **NP**, Link Partner is Next Page Able
NPA	2	ro	**Next Page Able** 0_B , Local device is not Next Page Able 1_B , Local device is Next Page Able
PR	1	ro, lh	**Page Received** 0_B **NPR**, A New Page has not been received 1_B **PR**, A New Page has been received
LPAN	0	ro	**Link Partner Auto Negotiation Able** 0_B **NAN**, Link Partner is not Auto negotiation able 1_B **AN**, Link Partner is Auto negotiation able

7 Electrical Characteristics

7.1 Absolute Maximum Ratings

Table 75 Absolute Maximum Rating

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	–	–	4.6	V	–
DC Input Voltage	V_{IN}	–	–	6	V	–
DC Output Voltage	V_{OUT}	–	–	4.6	V	–
Power Consumption	P_C	–	–	126	mA	@ Idle State
		–	–	7	mA	@ Suspend Mode
		–	–	142	mA	@ 10M Full Duplex Mode
		–	–	152	mA	@ 100M Full Duplex Mode
Storage Temperature	T_{STG}	-65	–	150	°C	–
Operation Temperature	T_{AMB}	-40	–	125	W	–
ESD Rating	V_{ESD}	–	–	2000	V	–

7.2 Operating Condition

Table 76 Operating Condition

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply Voltage	V_{DD}	3.0	–	3.6	V	–
Supply Current	I_{DD}	–	–	150	mA	–

7.3 DC Specifications

7.3.1 USB Interface DC Specification

Table 77 USB Interface DC Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	2.0	–	–	V	–
Input Low Voltage	V_{IL}	–	–	0.8	V	–
Differential Input Sensitivity	V_{DI}	0.2	–	–	V	–

Table 77 USB Interface DC Specification (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Differential Common Mode Range	V_{CM}	0.8	–	2.5	V	–
Output High Voltage	V_{CH}	2.8	–	3.6	V	–
Output Low Voltage	V_{OL}	0.0	–	0.3	V	–
Output Signal Crossover Voltage	V_{CRS}	1.3	–	2.0	V	–

8 EEPROM Interface DC Specification

8.1 Recommended Operating Conditions

Table 78 EEPROM Interface DC Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	1.8	–	5.5	V	–
Input Low Voltage	V_{IL}	-0.5	–	1.0	V	–
Input Leakage Current	I_I	± 1	–	± 1000	nA	V_{IN} 3.3V or 0 V
Output High Voltage	V_{OH}	2.4	–	–	V	–
Output Low Voltage	V_{OL}	–	–	0.4	V	–
Input Pin Capacitance	C_{IN}	–	–	5.66	pF	–

8.2 GPIO Interface DC Specification

Table 79 GPIO Interface DC Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input High Voltage	V_{IH}	1.8	–	5.5	V	–
Input Low Voltage	V_{IL}	-0.5	–	1.0	V	–
Input Leakage Current	I_I	± 1	–	± 1000	nA	V_{IN} 3.3 V or 0 V
Output High Voltage	V_{OH}	2.4	–	–	V	–
Output Low Voltage	V_{OL}	–	–	0.4	V	–
Input Pin Capacitance	C_{IN}	–	–	5.64	pF	–

9 Timing

9.1 Reset Timing

ADM8513/X can be reset either by hardware, software or USB reset.

- A hardware reset is accomplished by asserting the RST# pin after powering up the device. It should have a duration of at least 100 ms to ensure the external 12 MHz and crystal is in stable and correct frequency. All registers will be reset to default values.
- A software reset is accomplished by setting the reset bit (bit 4) of the Ethernet Control Register (address 01_H). This software reset will reset all registers to default values.
- When ADM8513/X sees an SE0 on USB bus for more than 2.5 s. This USB reset will reset all registers to default values

9.2 USB Interface Timing

Table 80 GPIO Interface DC Specification

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise Time	T_{FR}	4	–	20	ns	C_L=50 pF
Fall Time	T_{FF}	4	–	20	ns	C_L=50 pF
Rise and fall time matching	T_{FRFF}	90	–	111.11	%	$T_{FRFF} = T_{FR} / T_{FF}$

9.3 EEPROM Interface Timing

Table 81 EEPROM Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Clock Frequency	t_{EESK}	0	–	1	MHz	–
EECS Setup Time to EESK	t_{EECSS}	0.2	–	–	µs	–
EECS Hold Time from EESK	t_{EECSH}	0	–	–	ns	–
EEDO Hold Time from EESK	t_{EEDOH}	70	–	–	ns	–
EEDO Output Delay to “1” or “0”	t_{EEDOP}	–	–	2	µs	–
EEDI Setup Time to EESK	t_{EEDIS}	0.4	–	–	µs	–
EEDI Hold Time from EESK	t_{EEDIH}	0.4	–	–	µs	–

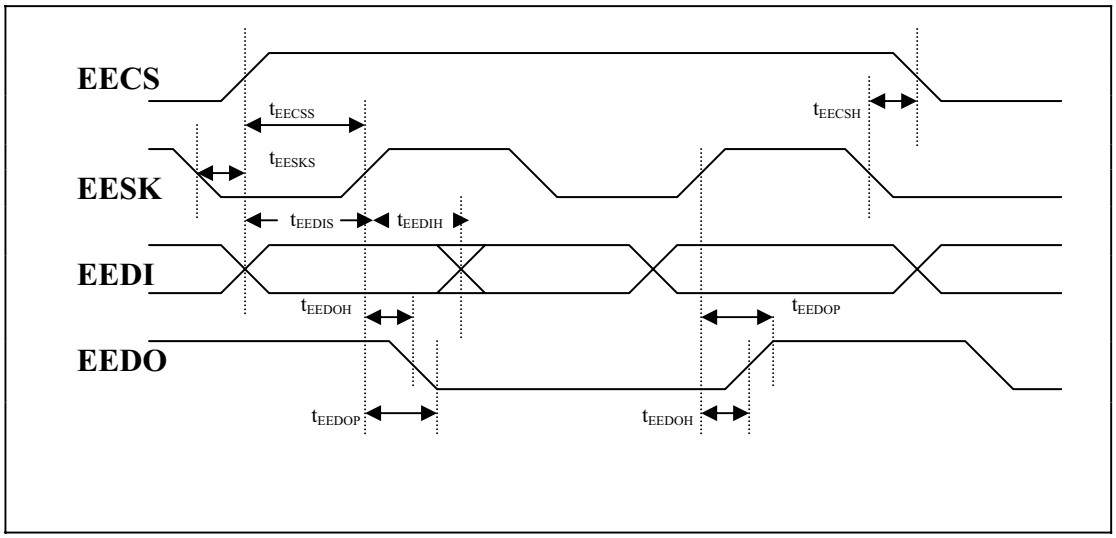


Figure 5 EEPROM Interface Timing

10 EEPROM Interface & Example

If the EEPROM contents from offset 0 to offset 5 is “FF_FF_FF_FF_FF_FF”, the EEPROM isn't programmed correctly. The default values for every field are used instead of loading from EEPROM.

Table 82 EEPROM Interface

Offset(Byte)	Field	Description
00	node_id0	The 1st byte of Ethernet node ID.
01	node_id1	The 2st byte of Ethernet node ID.
02	node_id2	The 3st byte of Ethernet node ID.
03	node_id3	The 4st byte of Ethernet node ID.
04	node_id4	The 5st byte of Ethernet node ID.
05	node_id5	The 6st byte of Ethernet node ID.
06-07	Reserved	
08	Max_Pwr	The maximum USB power consumption.
09	Ep3_Interval	The polling interval for endpoint 3. If this value is 0, EP3 is disabled.
0A[0]	Reserved	
0A[1]	USB_Sel	0A[1] = 1: select internal USB transceiver.
0A[4:2]	PHY Mode	0A[4:2]= 000
0B[0]	Reserved	
0B[5:1]	Reserved	
0B[7:6]	LED Mode	Refer to Pin assignment
0C	Languageid_lo	The low byte of language ID.
0D	Languageid_hi	The high byte of language ID.
0E-0F	Reserved	
10	Manuid_lo	The low byte of manufacture ID.
11	Manuid_hi	The high byte of manufacture ID.

Table 82 EEPROM Interface (cont'd)

Offset(Byte)	Field	Description
12	ProID_lo	The low byte of product ID.
13	ProID_hi	The high byte of product ID.
14	Manu_str_len	The length for manufacture string.
15	Manu_str_offset	The word offset address of manufacture string.
16	Pro_str_len	The length for product string.
17	Pro_str_offset	The word offset address of product string.
18	Seri_str_len	The length for serial number string.
19	Seri_str_offset	The word offset address of serial number string.

10.1 Example

offset(byte) Value

0000_H: 00, 00 E8 00 02 2C 00 00,
0008_H: 50 01 02 00 09 04 00 00
0010_H: A6 07 13 85 0E 10 2A 20
0018_H: 0A 38 00 00 00 00 00 00
0020_H: 0E 03 41 00 44 00 4D 00
0028_H: 74 00 65 00 6B 00 00 00
0030_H: 1E 00 55 00 53 00 42 00
0038_H: 20 00 31 00 30 00 2F 00
0040_H: 2A 03 55 00 53 00 42 00
0048_H: -20 00 54 00 6F 00 20 00
0050_H: 4C 00 41 00 4E 00 20 00
0058_H: 43 00 6F 00 6E 00 76 00
0060_H: 65 00 72 00 74 00 65 00
0068_H: 72 00 00 00 00 00 00 00
0070_H: 0A 03 30 00 30 00 30 00
0078_H: 31 00 00 00 00 00 00 00

Table 83 EEPROM Example

Offset(Byte)	Value	Description
00-05	00_00_E8_10 _46_02	NIC node ID
08	50	maximum power 160mA
09	01	interrupt endpoint 3 polling interval 1ms
0A	02	isochronous endpoint disables, selects internal USB transceiver Uses internal Ethernet PHY, Wakes on Lan en
0C-0D	0904	Language ID 0409
10-11	A607	manufacture ID 07A6
12-13	8513	product ID 8513
14	0E	manufacture string length 0E bytes
15	10	manufacture string starts from word offset 10h, thus byte offset 20_H.

Table 83 EEPROM Example (cont'd)

Offset(Byte)	Value	Description
16	1E	product string length 1E bytes
17	18	product string starts from word offset 18h, thus byte offset 30_H.
18	0A	serial number string length 0A bytes
19	38	serial number string starts from word offset 38h, thus byte offset 70_H.
20-2E	0E 03 41 00 44 00 4D 00 74 00 65 00 6B 00	0E:descriptor size 14 bytes 03: string descriptor 41.....: UNICODE encoded string
30-4E	1E 03 55 00 53 00 42 00 20 00.....	1E:descriptor size 30 bytes 03: string descriptor 55.....: UNICODE encoded string
50-5A	0A 03 30 00 30 00 30 00 31 00	0A: descriptor size 10 bytes 03: string descriptor 30.....: UNICODE encoded string

11 Package

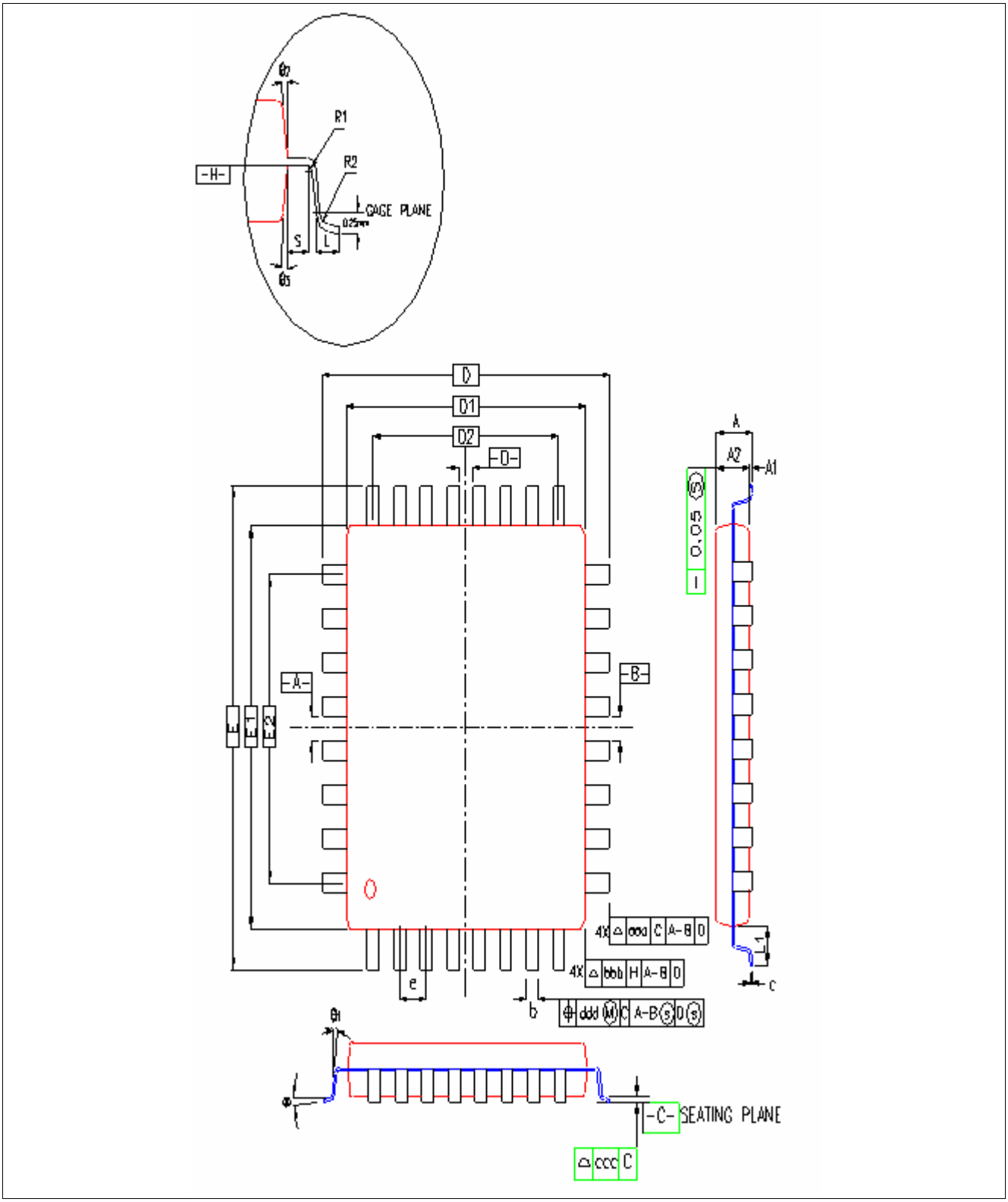


Figure 6 Package

Note: This diagram has a 32pin. But, the relative parameters presents 48pin package data. So, please ignore the pin number and regard the diagram as 48pin. Make an example: Parameter “E” (9mm) means the distance between the two opposite sides. Parameter "e" (0.8mm) means the distance between two adjacent pins. D&E1 means body size.

Table 84 Dimensions for 48 Pin LQFP Package

Symbol	Millimeter (mm)			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	–	–	1.60	–	–	0.063
A_1	0.05	–	0.15	0.002	–	0.006
A_2	1.35	1.40	1.45	0.053	0.005	0.057
D		9.00 BSC.			0.354 BSC.	
D_1		7.00 BSC			0.276 BSC.	
E		9.00 BSC			0.354 BSC.	
E_1		7.00 BSC			0.276 BSC.	
R_2	0.08	–	0.20	0.003	–	0.008
R_1	0.08	–	–	0.003	–	–
Θ	0°	3.5°	7°	0°	3.5°	7°
$Θ_1$	0°	–	–	0°	–	–
$Θ_2$	11°	12°	13°	11°	12°	13°
$Θ_3$	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00 Ref.			0.039 Ref.	
S	0.20	–	–	0.008	–	–
32L						
b	0.30	0.35	0.45	0.0012	0.0014	0.018
e		0.80 BSC.			0.031 BSC.	
D_2		5.60			0.220	
E_2		5.60			0.220	
Tolerance of Form and Position						
aaa		0.20			0.008	
bbb		0.20			0.008	
ccc		0.10			0.003	
ddd		0.20			0.008	
34L						
b	0.17	0.20	0.27	0.007	0.008	0.011
e		0.50 BSC.			0.020 BSC.	
D_2		5.00			0.197	
E_2		5.00			0.197	
Tolerance of Form and Position						
aaa		0.20			0.008	
bbb		0.20			0.008	
ccc		0.08			0.003	
ddd		0.08			0.003	
48L						
b	0.17	0.20	0.27	0.007	0.008	0.011

Table 84 Dimensions for 48 Pin LQFP Package (cont'd)

Symbol	Millimeter (mm)	Inch
e	0.50 BSC.	0.020 BSC.
D_2	5.50	0.217
E_2	5.50	0.217
Tolerance of Form and Position		
aaa	0.20	0.008
bbb	0.20	0.008
ccc	0.08	0.003
ddd	0.08	0.003

12 Appendix Layout Guide

Placement:

- At USB side, place ADM8513/X and USB connector as close as possible.
- At Ethernet side, place ADM8513/X, transformer and RJ45 as close as possible.
- The crystal or OSC device should be closed to ADM8513/X and away from the following items
  - Any analog signal
  - PCB edge
  - Any other high frequency components and their associated traces.

If you can't avoid those designs, please add a Resistor between Crystal (or OSC) and ADM8513/X chip clk48_I pin as figure show:

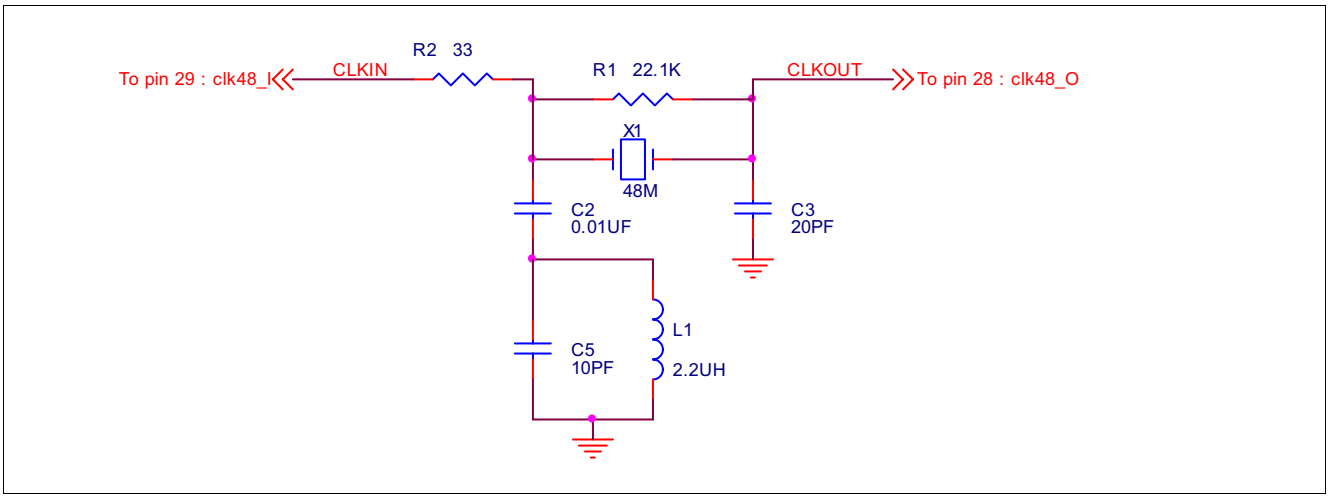


Figure 7 Placement 1

- Place the filtering capacitor as closed as possible at the Vcc pin of ADM8513/X and its trace must be short and wide.

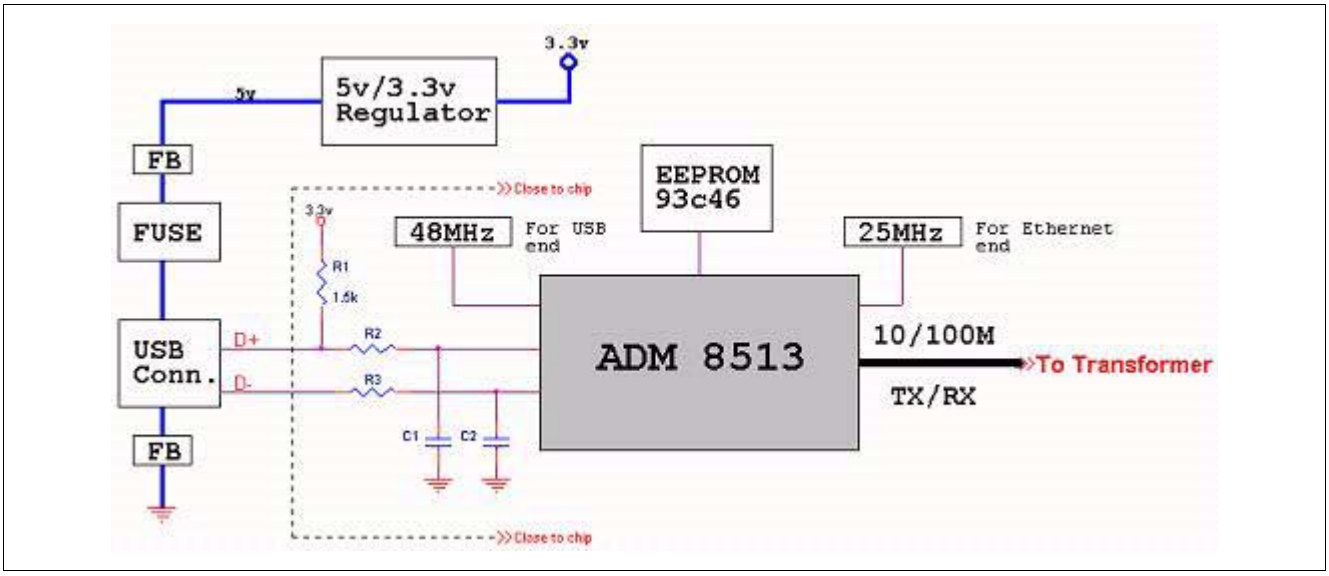


Figure 8 Placement 2

Trace routing

- Keep USB differential pair data signal D+ and D-:
  - Trace width should be as wide as possible.
  - Make D+ and D- traces route at the same signal plane and not pass through the other plane.
  - Inhibit crossover on D+ and D-
  - The termination resistance (R2,R3) and decoupling capacitors (C1,C2) should be closed to ADM8513/X.
  - D+ and D- Signal trace length should be equal and as short as possible.
- Arrangement Tx and Rx trace
  - Tx+/- and Rx+/- trace avoid right angle and round angle >90 degree, suggested.
  - Trace width must be wide and should be wider than 8 mils.
  - Signal trace length between Tx+/- differential pairs should be crossed and have equal length.The total length should be no longer than 2 cm. The same requirement applies to Rx+/- also.
  - Make Tx and Rx trace route at the same signal plane and not pass through the other plane.
  - Every differential pairs as cross as possible, but no less than 8 mils and space should be almost equal.
  - Keep space large between Tx and Rx differential pairs, even separated ground planes underneath Tx and Rx signal pairs.
  - Away from clock and power traces.
  - If Tx routed trace must cross, the trace can be swapped between chip and transformer, and transformer to RJ45,too.

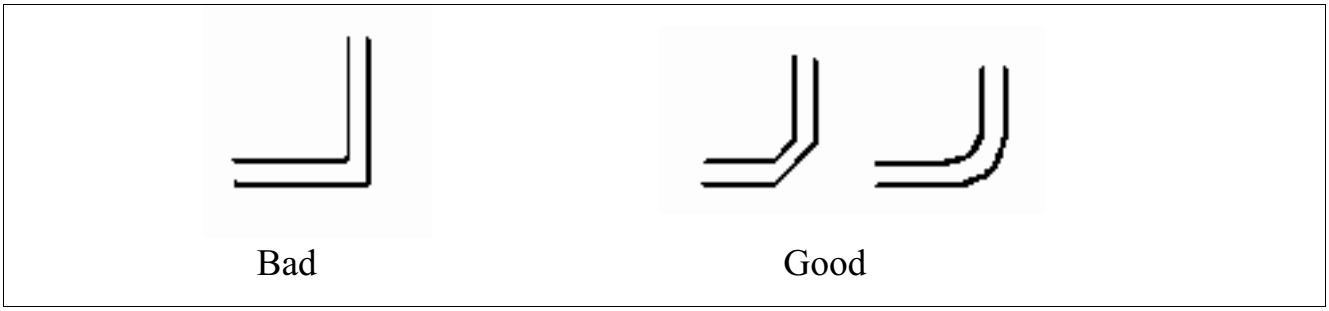


Figure 9 Trace Routing 1

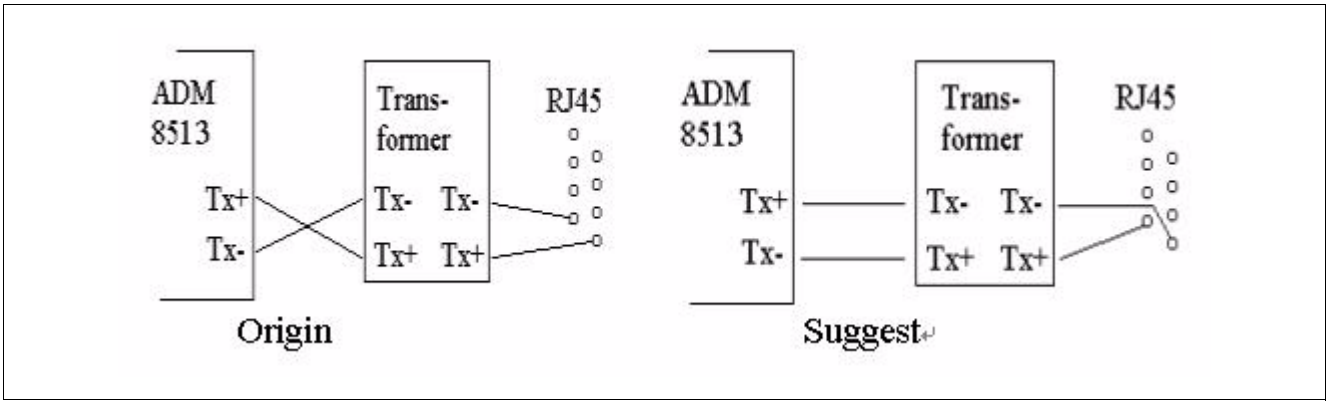


Figure 10 Trace Routing 2

- Digital signal should be away from analog signal and Vcc traces. If you can't avoid this situation, analog signal or Vcc trace should cross over 90 degree at other plane.

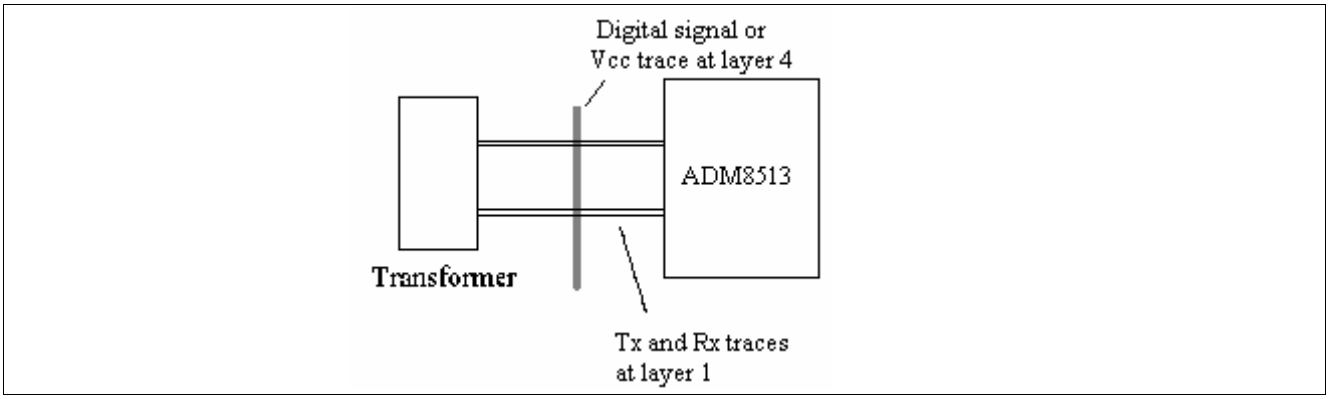


Figure 11 Trace Routing 3

- Vcc trace should be short and prefer route in the format of the plane a special for GND.

Power and Ground

- All of the Vcc pin should have a 0.1uF SMD capacitors which placed with it. To be effective, the capacitors should be placed as close as possible at the pin.
- The chassis ground plane connected to the USB B type and network connector chassis should be isolated from the signal plane with 0.1uF capacitors or bead to prevent any radiation from leaking and resulting in EMI failure.
- Right angle is recommend when partition Vcc as well as GND planes.
- Avoid Vcc and ground planes placing directly under the transformer.See the Figure as below.

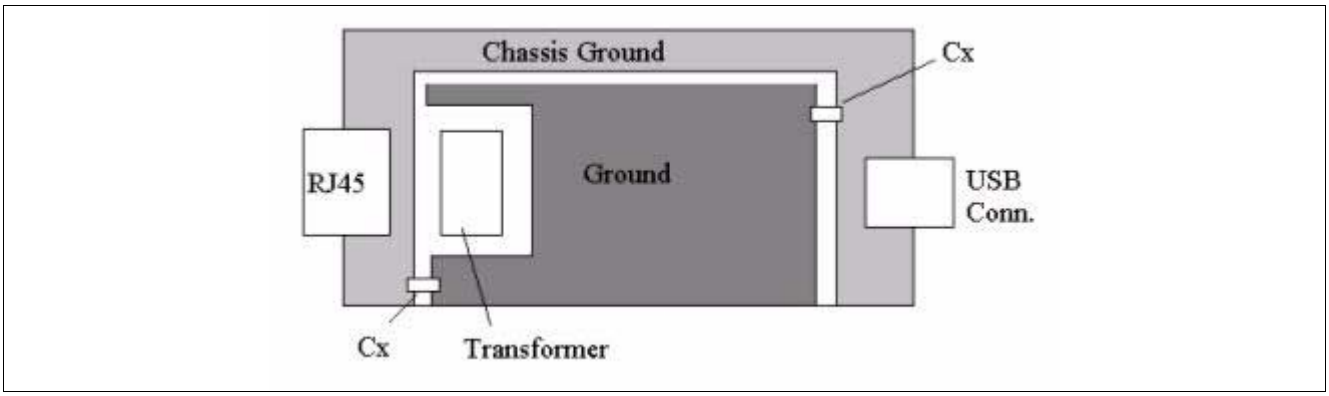


Figure 12 Power and Ground 1

- If you use a captive cable (plus the shield wire) it may require additional filtering for EMI test pass and the length of unshielded cable should be limited to 3cm or less.

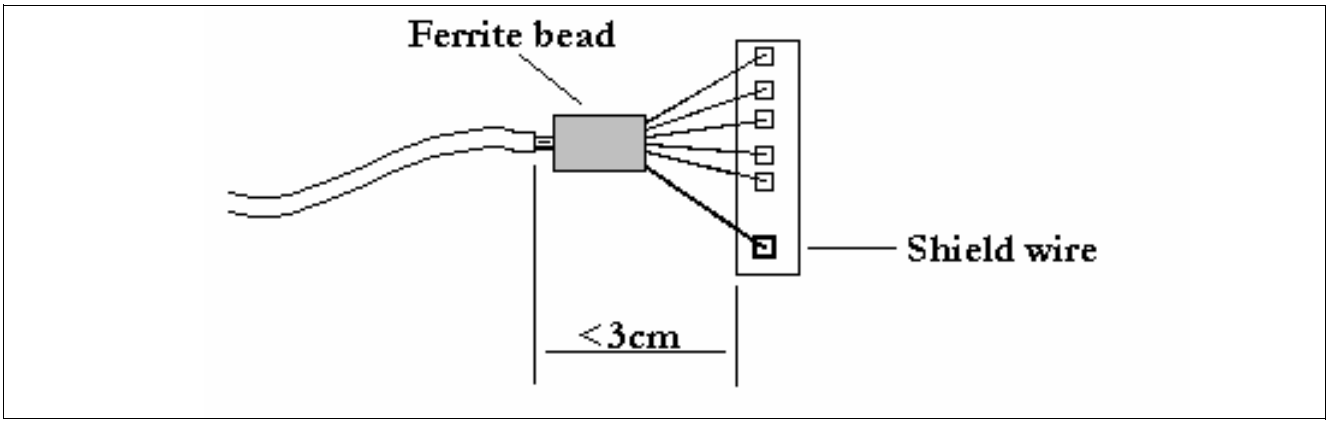


Figure 13 Power and Ground 2

- Please connect 10K Ohm Ribb resistance gnd, pin40(GndRef) and pin37(GndR) first then use signal via to Gnd (Specially for 2 layers board design).

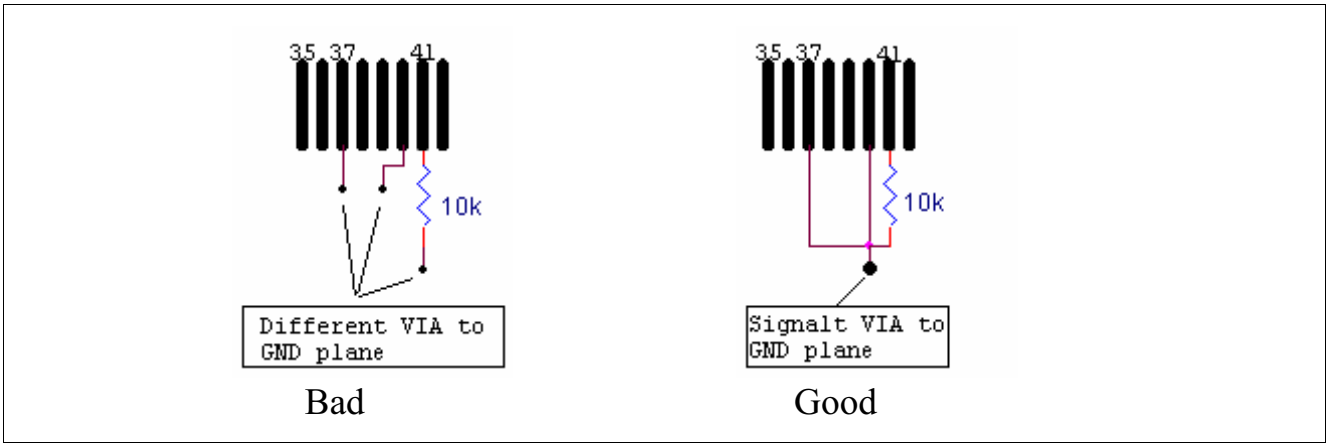


Figure 14 Power and Ground 3

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