Customer Information Notification

202107020I : PCA9635 Datasheet Send at Least 18 Clock Cycles + STOP Condition onto I2C Bus

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Issue Date: Aug 02, 2021 **Effective date:Aug 03, 2021**

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Management summary

Updated sections 4.0 "Ordering Information", 7.5 "Power-On Reset (POR)" and 8.4 "I2C-bus SDA line stuck low recovery mechanism" of the Datasheet, to ensure the users send at least 18 clock cycles + STOP condition onto 12C bus if it detects SDA line stuck low.

Change Category

[ ]Wafer Fab Process	[ ]Assembly Process	[ ]Product Marking	[ ]Test Process	[ ]Design
[ ]Wafer Fab Materials	[ ]Assembly Materials	[ ]Mechanical Specification	[ ]Test Equipment	[X]Errata
[ ]Wafer Fab Location	[ ]Assembly Location	[ ]Packing/Shipping/Labeling	[ ]Test Location	[ ]Electrical spec./Test coverage
[ ]Firmware	[ ]Other			

PCN Overview

Description

Updated the following Datasheet sections:

4.0 Ordering Information:
Added PCA9635PW/Q900 (AEC-Q100 compliant)

7.5 Power-on reset
Added the following paragraph:
PCA9635 requires the I2C master device always sends START condition to communicate with PCA9635 after POR (Power-on-Reset) is completed. After the initial START condition than either START or repeated START are acceptable.

8.4 I2C-bus SDA line stuck low recovery mechanism
PCA9635 requires I2C master device sends at least 18 clock cycles + STOP condition onto I2C bus if it detects SDA line stuck low by any I2C slave device on the bus vs the normal 9 or more clock cycles due to the register set sequence.

Reason

The intend of these updates is to ensure that the customers send at least 18 clock cycles + STOP condition onto I2C bus if it detects SDA line stuck low by any I2C slave device on the bus vs the normal 9 or more clock cycles due to the register set sequence.

Identification of Affected Products

Product identification does not change

Anticipated Impact on Form, Fit, Function, Reliability or Quality

Customer must send at least 18 clock cycles + STOP condition onto I2C bus if it detects SDA line stuck low by any I2C slave device on the bus vs the normal 9 or more clock cycles due to the register set sequence.

Data Sheet Revision

No impact to existing datasheet

Disposition of Old Products

Existing inventory will be shipped until depleted

Remarks

Customer reported the devices can't recognize the component through I2C when sending 9 clock I2C waveform onto I2C bus, as the SDA line is stuck at low level. This issue appears when addresses 0x13 (0010 011x) and 0x17 (0010 111x) are set.

NXP Evaluation: Failure came to light based on Customer Application Usage. As a due diligence NXP performed an extensive evaluation on 20 returned devices and implemented a new TP which to production on 9-Jan-2020.

A Root Cause Statement was provided, plus a Workaround Firmware Fix for the customer to insert 18 clock cycles plus a stop command before any other activity on I2C bus.

New Test Screen Implementation: TPE developed a new test pattern that screened all customer returns. The new TP was implemented to production on 9-Jan-2020. NXP to revert back to original TP once end customer implement the workaround fix.

Contact and Support

For all inquiries regarding the ePCN tool application or access issues, please contact NXP "Global Quality Support Team".

For all Quality Notification content inquiries, please contact your local NXP Sales Support team.

For specific questions on this notice or the products affected please contact our specialist directly:

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Changed Orderable Part#	12NC	Product Type	Product Description	Package Outline	Package Description	Product Status	Customer Specific Indicator	Product Line
PCA9635PW,118	935282225118	PCA9635PW	PCA9635	(T)SSOP28	SOT361-1	RFS	No	BLC6